# UM1585
# User manual

## EVALSP1310CPU
## evaluation board, hardware revision 1

## Introduction

This document applies to hardware revision 1 evaluation boards.

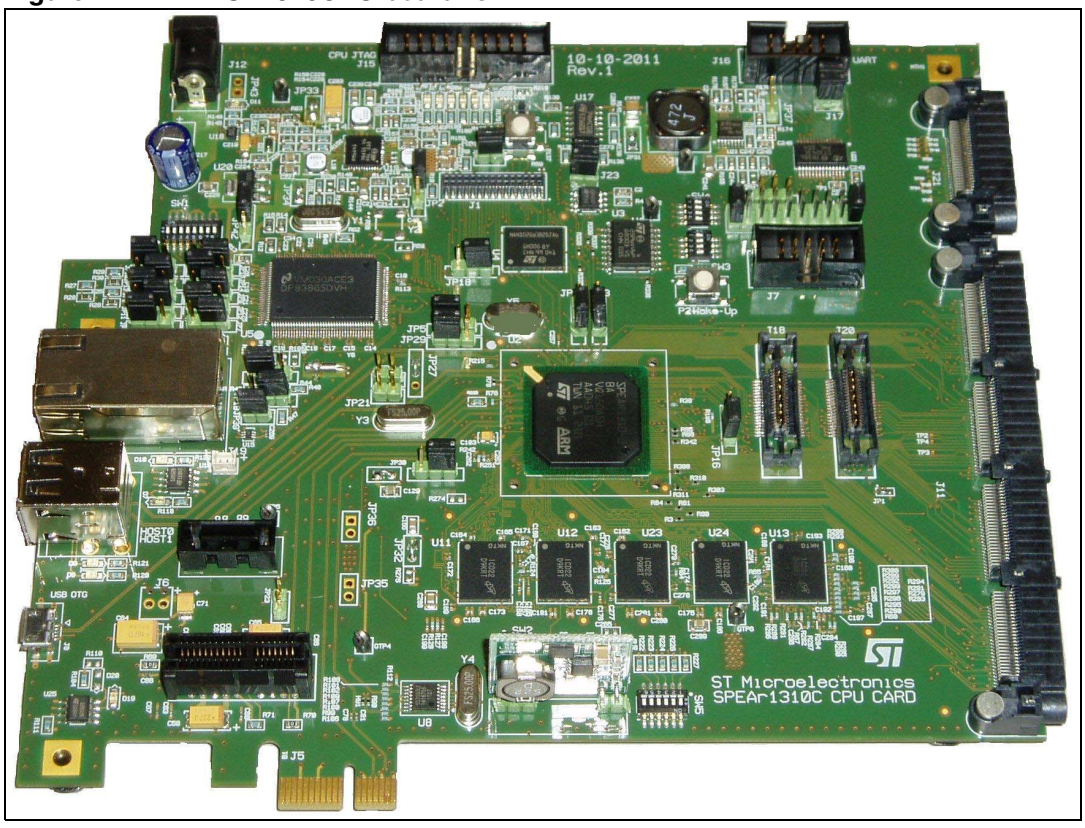
This evaluation board is intended to be used to:

- enable quick evaluation and debugging of software for the SPEAr1310 rev.C embedded MPU family
- act as a learning tool for rapid familiarity with the features of the SPEAr1310 rev.C
- provide a reference design to use as a starting point for the development of a final application board

The EVALSP1310CPU board is equipped with interfaces to the high speed peripherals embedded in SPEAr1310 rev. C devices.

Through an expansion connector it is possible to plug in dedicated expansion boards (EVALBASEXP) and/or FPGA boards (EVALSP13xxFPGA) for developing customer-specific IPs.

**Figure 1. EVALSP1310CPU board rev. 1**



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# 1 Kit contents

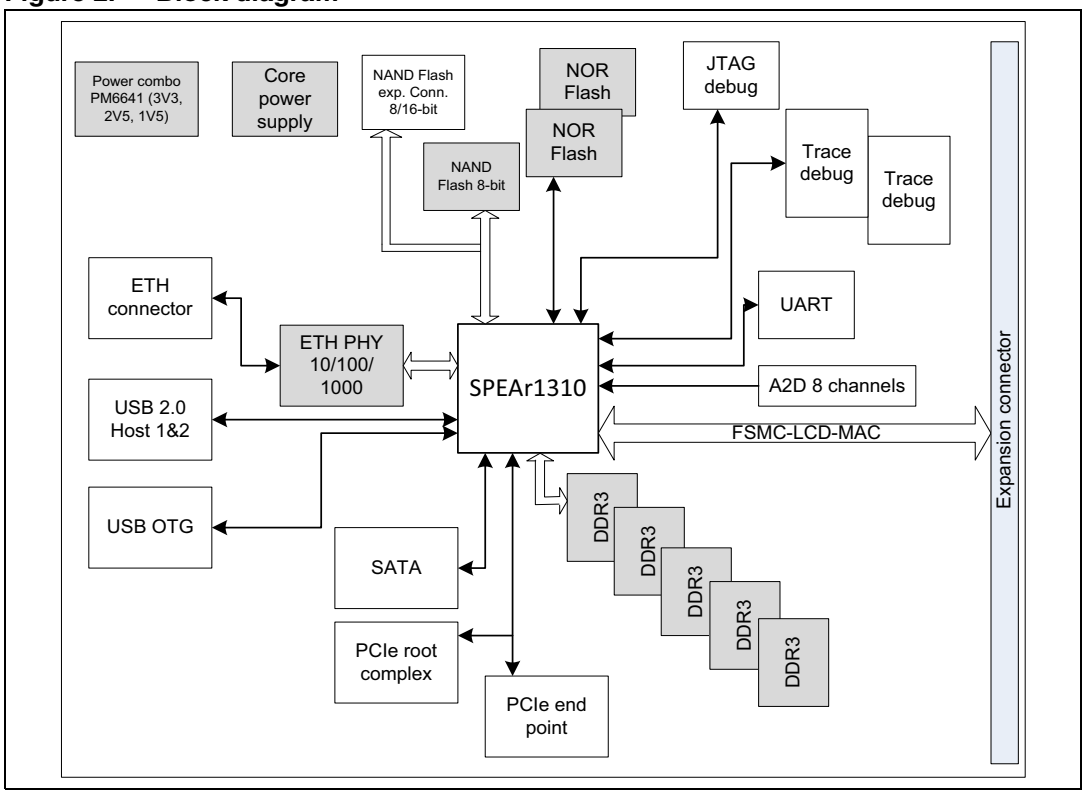
- EVALSP1310CPU board
- AC adapter (output voltage 5 V 2A)
- 2 power adapter plugs (USA/Europe)

# 2 Features and block diagram

## 2.1 Board features

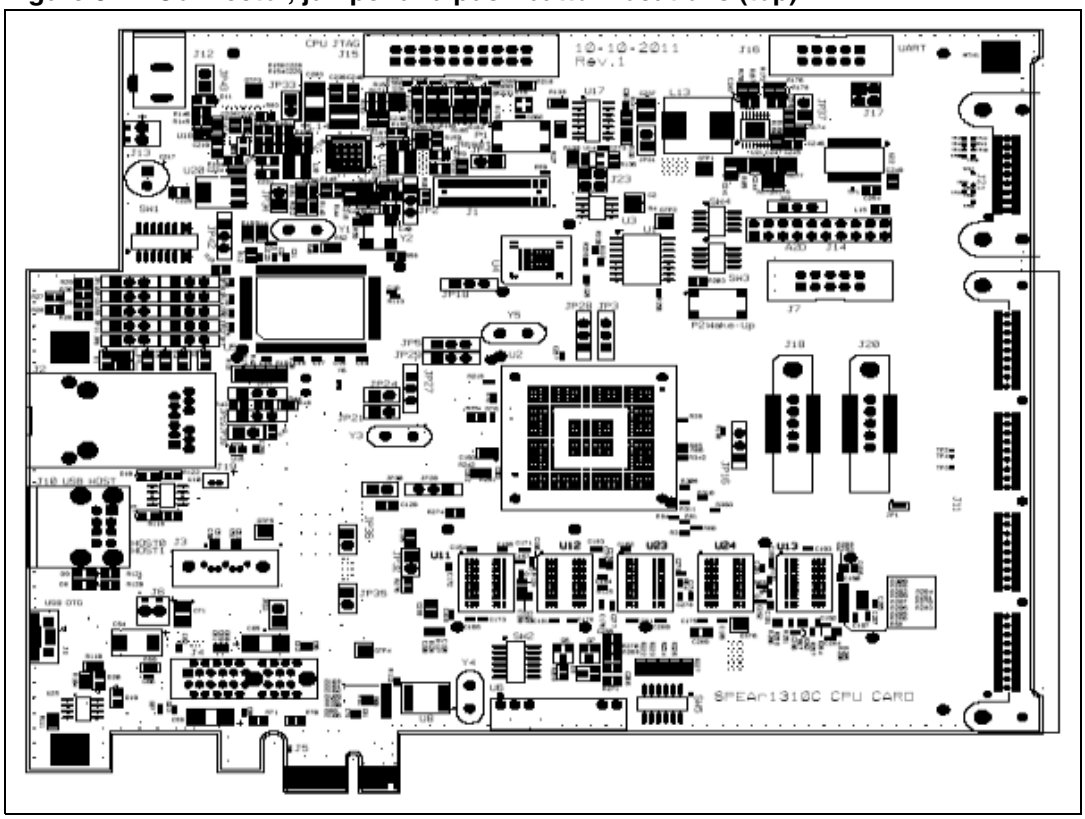
- SPEAr1310 SoC CPU
- Dedicated 16/32-bit trace port (program trace)
- Five DDR3 chips (32-bit width plus ECC), 1 GB
- Serial NOR Flash, 8 MB
- Serial NOR Flash 512 KB
- 8-bit NAND Flash, 256 MB
- 16-bit NAND Flash expansion connector
- Two USB 2.0 full speed Host ports
- One OTG 2.0 high speed port (Micro USB-AB)
- One 10/100/1000 Ethernet port
- One SATA connector
- One PCIe X1 Endpoint
- One PCIe X1 Root Complex connector
- One Serial port (up to 115 Kbaud)
- Debug ports (CPU JTAG & CoreSight)
- 8 ADC channels (10 bit, 1 Msamples/s)
- Expansion connector

**Figure 2. Block diagram**



## 2.2 Connectors, jumpers and pushbuttons

**Figure 3. Connector, jumper and push button locations (top)**



# 3 Getting started

**Caution:** This board contains electrostatic-sensitive devices

The EVALSP1310CPU board is shipped in protective anti-static packaging. Do not submit the board to high electrostatic potentials, and follow good practices for working with static sensitive devices.

- Wear an anti-static wristband. Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- Zero potential. Always touch a grounded conducting material before handling the board, and periodically while handling it.
- Use an anti-static mat. When configuring the board, place it on an anti-static mat to reduce the possibility of ESD damage.
- Handle only the edges. Handle the board by its edges only, and avoid touching board components.

## 3.1 Connecting

1. Connect a serial cable adapter (RS232 on J16) to a host PC (see Primary Serial cable setting).
2. On a host PC running Windows or Linux, start the Terminal program.
3. Connect the AC adapter to a power outlet.
4. Power on the board (plug the AC adapter jack into J12). A sequence of boot messages displays, followed by the Linux console prompt.

Software user manuals are available on request; contact your local ST representative.

## 3.2 Booting

The EVALSP1310CPU board can boot a Linux kernel pre-installed in the serial NOR Flash.

At power on, the serial port outputs a brief header message with some uBoot information (uBoot version, SDK version, and some internal hardware information). At this point, you can choose to:

- Stop the system directly in uBoot

  To do this, press the spacebar on the host computer keyboard before the boot delay time expires (default is 3 seconds).
- Boot Linux

  The system logs you in automatically as super user, and the Linux shell prompt displays on the screen.

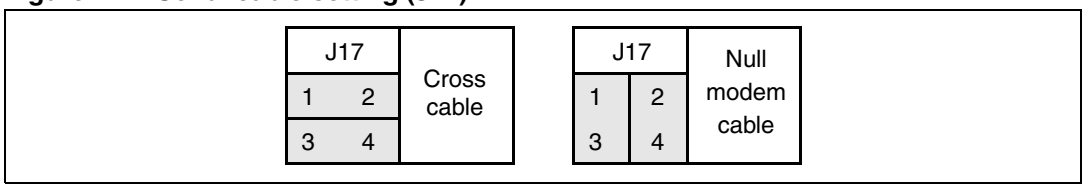
## 3.3 Serial interface

A serial interface, which can typically be used to connect an operating system monitor console, is available on the J16 connector.

It is possible to simulate a cross cable by changing the position of the J17 jumpers as shown below.

Refer to the schematic drawing (contact your local ST representative for availability), for the pin-out of the connectors.

**Figure 4. Serial cable setting (J17)**




## 3.4 Reset switch

A manual reset switch (P1) is available on the top side of the board.

# 4 Block descriptions

## 4.1 General power supply

The power supply block generates all the required voltages from a 5 V external AC/DC. The generated voltages are:

- 5 V obtained from an over voltage protection device with thermal shutdown
- 1.2 V, generated from 5 V with a step-down switching regulator
- 1.5 V, 2.5 V, and 3.3 V generated from 5 V with a multi-output switching regulator
- 12 V generated from 5 V with a set-up converter
- 1.8 V generated from 3.3 V with a low drop voltage regulator

**Table 1. Common power rails**

| Name | Use | Jumper for current measurement |
|---|---|---|
| +5V | J13: Alternate power input connector<br>J11: Expansion connector | |
| VDD1V2 | SPEAr core (SPEAr_VDD1V2)<br>SPEAr DDR3 interface (SPEAr_DDR3_1V2) | JP31<br>JP30 |
| VDD1V5 | DDR3 chips<br>SPEAr DDR I/O (SPEAr_DDR3_1V5)<br>SPEAr RTC (RTC_VDD1V5) | -<br>JP32<br>JP39 |
| VDD1V8 | GigaPhy chip<br>SPEAr 1.8 V NAND8 Flash (JP3: Close 2&3 for 1.8 V)<br>NAND Flash chip (Close 2&3 of JP2 for 1.8V)<br>NAND expansion connector (Close2&3 of JP3) | -<br>JP3(2-3) |
| VDD2V5 | SPEAr_OTP antifuses (JP1: Close 1&2 to supply)<br>SPEAr GMII interface(JP16: Close 2&3 for 2.5V)<br>SPEAr PCIe (JP24 close and JP5: Close 2&3 for ext power)<br>SPEAr A2D_PLLs_VDD2V5<br>SPEAr USB_VDD2V5<br>A2D connector<br>Ethernet RJ45 (J2)<br>Giga PHY (JP42 close 2&3) | JP33<br>JP1(1-2)<br>JP16(2-3) |
| VDD3V3 | SPEAr (SPEAr_VDD3V3)<br>PCIe Clock Source<br>JTAG MIPHY connector<br>Giga PHY (JP42 close 1&2)<br>Serial NOR Flash<br>NAND Flash chip (Close 1&2 of JP2 for 3.3V)<br>NAND expansion connector (Close1&2 of JP3)<br>CPU JTAG & trace connectors | JP34 |

Table 1. Common power rails (continued)

| Name | Use | Jumper for current measurement |
|---|---|---|
| VDD3V3_HOST | PCIe x1 connectors | |
| +12V_HOST | PCIe x1 connectors | |

### 4.1.1 Power LEDs

Table 2. Power LEDs

| Ref. Des. | Description |
|---|---|
| D11 red | 5 volt fault: undervoltage or overvoltage on +5V |
| D13 green | 5 volt: +5V |
| D12 green | 1.2 volt: VDD1V2 |
| D14 green | 1.5 volt: VDD1V5 |
| D17green | 1.8 volt: VDD1V8 |
| D16 green | 2.5 volt: VDD2V5 |
| D15 green | 3.3 volt: VDD3V3 |

A low-power supervisory device monitors the power supplies and generates a reset signal.

## 4.2 Dynamic memory subsystem

Five Micron DDR3 chips (MT41J256M8) are used: four for data (32-bit width), and one for ECC.

Total size available is 4 chips x 32 Mb x 8 x 8 banks = 1 Gbyte.

## 4.3 Static memory subsystem

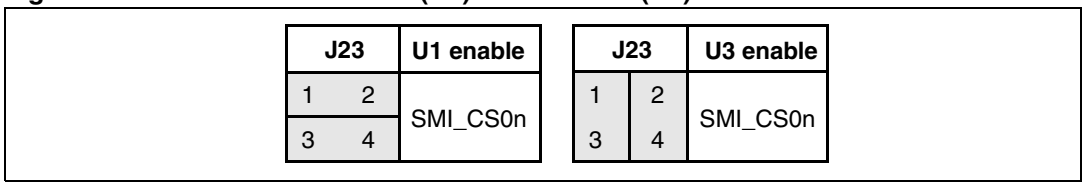
### 4.3.1 Serial Flash

The following components are connected to the SMI interface:

- M25P64 (U1) ST serial Flash device: memory size = 8 MB
- M25P40 (U3) ST serial Flash device: memory size = 512 KB (optional, the device is not installed on the board)

To enable M25P64 or M25P40, use SMI_CS0 with the J23 jumpers set as shown in *Figure 5*.

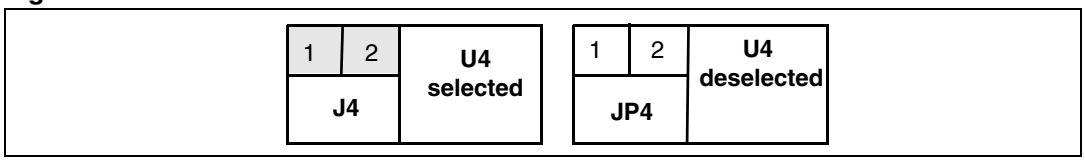
**Figure 5. Serial Flash M25P64 (U1) and M25P40 (U3) enable**




### 4.3.2 NAND Flash

This block is based on ST NAND Flash NAND02GW3B (U4) (64 MB; bus width = x8). If required, this chip can be replaced and another can be used. To do this, deselect the on-board Flash by removing jumper JP4, and connect an adapter board to J1.

**Figure 6. NAND Flash selection**




### 4.3.3 NAND Flash expansion

A 30-pin expansion connector (J1) enables the use of different Flash devices. When used, remove jumper JP4.

**Table 3. J1 NAND expansion connector pin assignment**

| Pin number | Signal |
|---|---|
| 1, 3, 29 | NAND_VDD |
| 2, 4, 28, 30 | GND |
| 5 ... 20 | NFIO0 ... NFIO15 |
| 21 | NFnCE |
| 22 | NFALE |
| 23 | NFCLE |
| 24 | NFRnB |
| 25 | NFnRE |

Table 3. J1 NAND expansion connector pin assignment (continued)

| | |
|---|---|
| 26 | NFnWP |
| 27 | NFnWE |

On the expansion connectors it is possible, through JP2, to select NAND_VDD between 3.3 V and 1.8 V to test different voltage devices. The NAND FLASH SPEAr I/O voltage has to be aligned with the Flash device voltage. Use JP2, JP3 and Strapping option SW4.1 to set the correct voltage.

Figure 7. NAND Flash device voltage selector

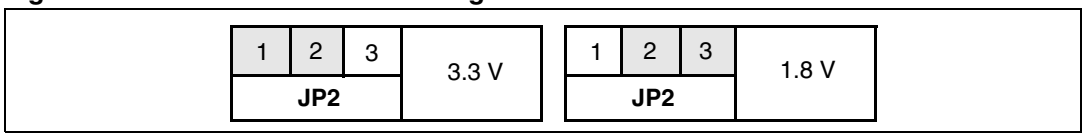
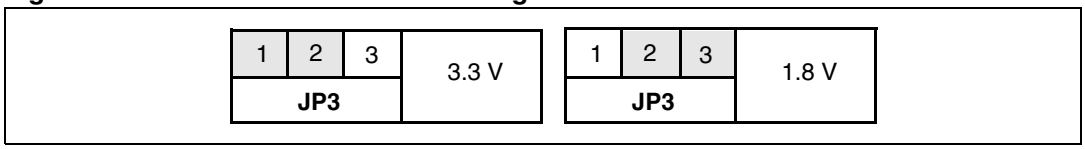



Figure 8. SPEAr NAND Flash I/O voltage selector



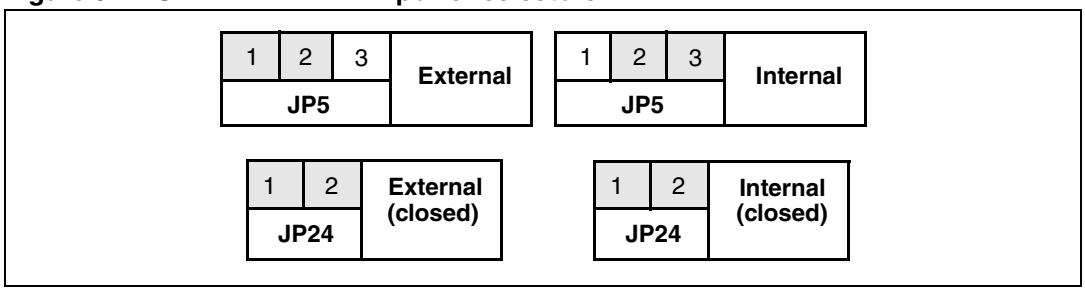

## 4.4 PCIe/SATA

The SPEAr1310 rev. C device has up to 3 PCIe or 3 SATA interfaces. The EVALSP1310CPU board provides the following configuration: one standard SATA and two PCIe Gen2 lanes.

The lane (PHY1) is used as a PCIe endpoint. In the default setting, the PCIe endpoint is not available. To make the PCIe endpoint available it is necessary to change the settings of the board removing the 0 ohm resistors, R90 and R91 and installing 0 ohm resistors, R92 and R93. The lane PHY0 is used as SATA and on board there is a standard connector (J3).

SPEAr MIPHY PLL can be powered by an internal regulator or can use external power. JP24 has to be configured according to the JP5 setting.

Figure 9. SPEAr MIPHY PLL power selectors




### 4.4.1 PCIe clock

The PCIe clock is generated by ICS557-03 (differential clock generator). This device can generate 2 different clock frequencies. This depends on the settings of bits S2 to S0.

Table 4. PCIe clock settings (default settings)

| S2 (SW2-3) | S1(SW2-2) | S0 (SW2-1) | Spread % | Spread type | Output frequency |
|---|---|---|---|---|---|
| 0 | 0 | 0 | -0.5 | Down | 100 |
| 0 | 0 | 1 | -1.0 | Down | 100 |
| 0 | 1 | 0 | -1.5 | Down | 100 |
| 0 | 1 | 1 | No spread | Not applicable | 100 |
| 1 | 0 | 0 | -0.5 | Down | 200 |
| 1 | 0 | 1 | -1.0 | Down | 200 |
| 1 | 1 | 0 | -1.5 | Down | 200 |
| 1 | 1 | 1 | No spread | Not applicable | 200 |

The output frequency must be set at 100 MHz. On the EVALSP1310CPU board, the default settings is S2 ... S0 = 0.

## 4.5 Ethernet subsystem

This subsystem is based on the Ethernet GMII PHY DP83865 (U5) and a connector that also includes all the required magnetics. Several configuration jumpers are present and also several LEDs to display the line status/activity.

### 4.5.1 Configuration jumpers and switches

Table 5. Switch 1 configuration

| Pin | Description (default settings) |
|---|---|
| 1 | Phy address bit 1 (0 - ON) |
| 2 | Phy address bit 2 (1 - OFF) |
| 3 | Phy address bit 3 (0 - ON) |
| 4 | Phy address bit 4 (0 - ON) |
| 5 | **MULTIPLE NODE ENABLE**: This pin determines if the PHY advertises Master (multiple nodes) or Slave (single node) priority during 1000BASE-T Auto-Negotiation.<br>1: multiple node priority (switch or hub)<br>0: single node priority (NIC) (0 - ON) |
| 6 | **AUTO MDIX ENABLE**: This pin controls the automatic pair swap (Auto-MDIX) of the MDI/MDIX interface.<br>1: pair swap mode enabled<br>0: Auto-MDIX disabled, and part defaulted into the mode preset by the MAN_MDIX_STRAP pin. (0 - ON) |
| 7 | **CLOCK TO MAC ENABLE**:<br>1: CLK_TO_MAC clock output enabled<br>0: CLK_TO_MAC disabled (1 - OFF) |
| 8 | Not used |

*Note: When DIP switch SWx-x is in the ON position, the bit value is 0. When the DIP switch is in the OFF position, the bit value is 1.*

**Table 6. Jumper configurations**

| Default Settings | | | | | | Description |
|---|---|---|---|---|---|---|
| On | | | Off | | | |
| JP6 | | | JP11 | | | Phy address bit 0 |
| 1 | 2 | 3 | 1 | 2 | 3 | |
| JP7 | | | JP12 | | | Auto negotiation enable bit |
| 1 | 2 | 3 | 1 | 2 | 3 | |
| JP8 | | | JP13 | | | Full duplex select bit |
| 1 | 2 | 3 | 1 | 2 | 3 | |
| JP9 | | | JP14 | | | Speed select bit 1 (see *Table 3: J1 NAND expansion connector pin assignment* and *Table 4: PCIe clock settings (default settings)*) |
| 1 | 2 | 3 | 1 | 2 | 3 | |
| JP10 | | | JP15 | | | Speed select bit 1 (see *Table 3: J1 NAND expansion connector pin assignment* and *Table 4: PCIe clock settings (default settings)*) |
| 1 | 2 | 3 | 1 | 2 | 3 | |

SPEAr GMII I/F VDD could be 3.3 V or 2.5 V. It is possible test this functionality by moving two jumpers: one for SPEAr pads and one for the external DP83865 (U5).

The two jumpers must also be aligned with strapping option SW4.2.

**Figure 10. SPEAr GMII I/F voltage selector**

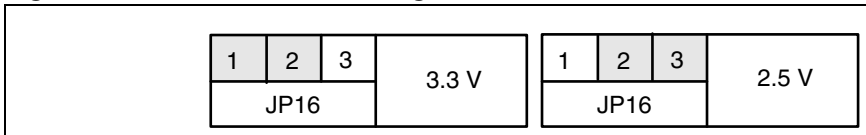
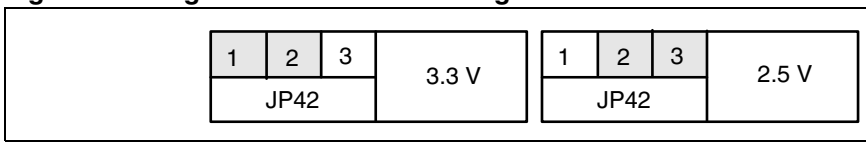
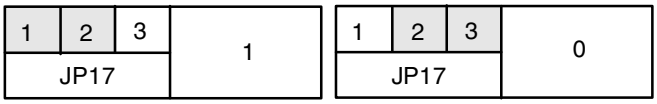



**Figure 11. Gigabit PHY Ethernet voltage selector**




Three JP are used as DP83865 (U5) strapping option: JP17, JP18 and JP19.

**Figure 12. DP83865 clock output selector**




0 = Clock to MAC output is 25 MHz
1= Clock to MAC output is 125 MHz

**Table 7. DP83865, MAC interface setting**

| JP18 (TXCLK_RGMII_SEL1) | JP19 (CRS_RGMII_SEL0) | MAC Interface |
|---|---|---|
| 0 | 0 | GMII |
| 0 | 1 | GMII |
| 1 | 0 | RGMII HP |
| 1 | 1 | RGMII 3COM |

*Note: EVALSP1310CPU BOARD was designed for GMII mode only.*

SPEED SELECT STRAP: These strapping option pins have two different functions depending on whether auto-negotiation is enabled or not. See *Table 8* and *Table 9*.

**Table 8. Auto-negotiation disabled**

| Speed[1] | Speed[0] | Speed enabled |
|---|---|---|
| 1 | 1 | Reserved |
| 1 | 0 | 1000BASE-T |
| 0 | 1 | 100BASE-T |
| 0 | 0 | 10BASE-T |

**Table 9. Auto-negotiation enabled**

| Speed[1] | Speed[0] | Speed enabled |
|---|---|---|
| 1 | 1 | 1000BASE-T, 10BASE-T |
| 1 | 0 | 1000BASE-T |
| 0 | 1 | 1000BASE-T, 100BASE-T |
| 0 | 0 | 1000BASE-T, 100BASE-T, 10BASE-T |

### 4.5.2 Ethernet LEDs

**Table 10. Ethernet LEDs**

| Reference | Description |
|---|---|
| D1<br>Yellow | **DUPLEX STATUS:** The LED is lit when the PHY is in Full Duplex operation after the link is established. |
| D2<br>Yellow | **1000M SPEED AND GOOD LINK LED**: The LED output indicates that the PHY has established a good link at 1000 Mbps.<br>In 1000BASE-T mode, the link is established as a result of training, Auto-Negotiation completed, valid 1000BASE-T link established and reliable reception of signals transmitted from a remote PHY is received. |
| D3<br>Yellow | **100M SPEED AND GOOD LINK LED**: The LED output indicates that the PHY has established a good link at 100 Mbps.<br>In 100BASE-T mode, the link is established as a result of an input receive amplitude compliant with TP-PMD specifications which will result in internal generation of Signal Detect. LINK100_LED will assert after the internal Signal Detect has remained asserted for a minimum of 500 µs. LINK100_LED will de-assert immediately following the de-assertion of the internal Signal Detect. |
| D4<br>Yellow | **10M GOOD LINK LED**: In the standard 5-LED display mode, this LED output indicates that the PHY has established a good link at 10 Mbps. |
| D5<br>Yellow | **ACTIVITY LED**: The LED output indicates the occurrence of either idle error or packet transfer. |

# 5 USB 2.0 subsystem

## 5.1 Host ports

The board has two host ports that are fully compliant with the USB 2.0 specification (two controllers with one port each). This means that the two hosts can work in concurrent mode with the maximum possible bandwidth. Each host has also full control of the VBUS supplied by the ST2052 or STMP2252MTR power switch that also provides over current protection in case of a short circuit in the USB cable. The ports are equipped with LEDs showing the power status of each port (the green LED indicates the presence of VBUS and the red one the current limiter status).

## 5.2 Host LEDs

**USB host LEDs**

**Table 11. USB host LEDs**

| Reference | Description |
|---|---|
| D7<br>Red | **USB HOST1 OVERCURRENT**: Abnormal current flowing on USB HOST 1 port |
| D8<br>Green | **USB HOST1 VBUS**: VBUS present on USB HOST port 1 |
| D9<br>Green | **USB HOST1 VBUS**: VBUS present on USB HOST port 2 |
| D10<br>Red | **USB HOST2 OVERCURRENT**: Abnormal current flowing on USB HOST 2 port |

## 5.3 OTG USB

One OTG micro USB-AB connector is present on the board.

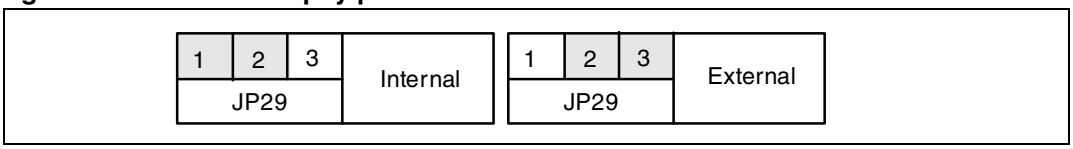
**Table 12. OTG micro USB-AB LEDs**

| Reference | Description |
|---|---|
| D20 Red | **USB OTG OVERCURRENT**: Abnormal current flowing on OTG USB |
| D19 Green | **USB OTG VBUS**: VBUS present on OTG USB |

### 5.3.1 SPEAr USB interface power

SPEAr USB phy (2.5 V) could be powered by an internal regulator or use external power.

**Figure 13. SPEAr USB phy power selector**



# 6 A/D Interface

Eight analog input lines are provided on the J14 strip connector.

**Table 13. J14 (20) ADC connector A2D**

| Pin number | Signal |
|---|---|
| 1 | ADC_VREFP |
| 2 | ADC_VDD2V5 |
| 3 ... 17 (odd only) | AIN0 ... AIN7 |
| 4 ... 20 (even only) | AGND |
| 19 | ADC_VREFN |

The connector also allows you to determine the conversion range by setting the conversion limits on pins J14.19 (lower limit) and J14.1 (upper limit). The default setting is to have pins 1-2 and 19-20 shorted by jumpers, which sets the conversion range to the maximum value of 0 to 2.5 V, with a granularity of 2.44 mV.

Removing the two jumpers and providing different values on pins 1 and 19 makes it possible to reduce the range, increasing the granularity. For example, an input of 1 V on J14.19 and 2 V on J14.1 provides a range of 1 to 2 V, in steps of less than 1 mV.

In any case, ensure the following relationships between the pins:

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0 V | ≤ | J14.19 | ≤ | J14 17 .. 3 | ≤ | J14.1 | ≤ | +2.5 V |
| AGND | ≤ | Vref_n | ≤ | ADC_In channels | ≤ | Vref_p | ≤ | AVDD |

# 7 RTC (battery connector)

To avoid losing data even if the main power supply is switched off, the Real Time Clock can be powered with a 3 V external battery (J19).

# 8 Expansion connectors

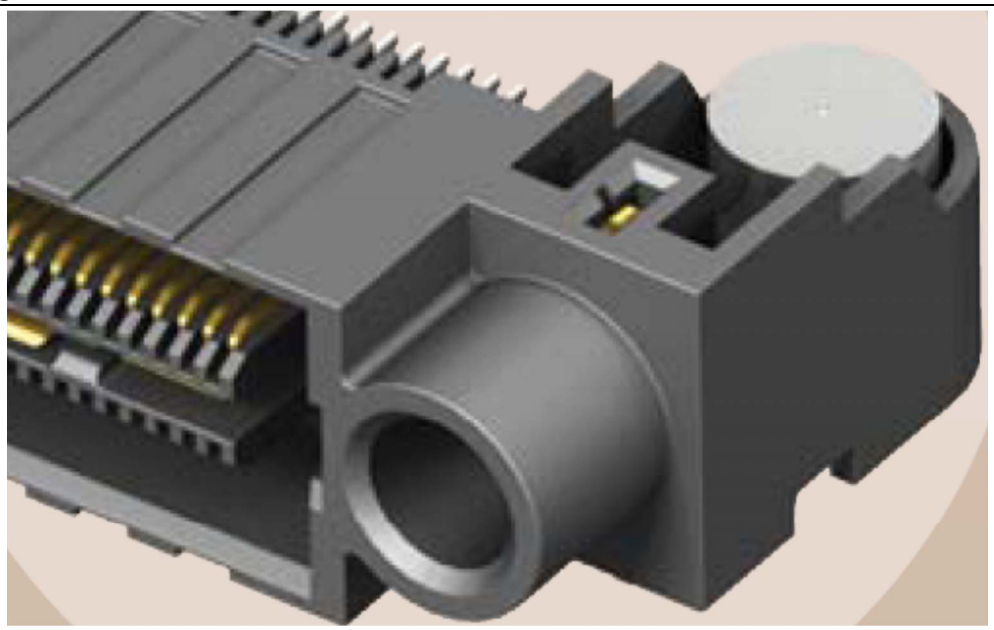
Expansion connectors J11 and J21 are provided to enable the use of an additional board.

Both connectors are Samtec High Speed Board-to-Board connectors Q2 Right angle.

- J11, P/N QFS-104-01-SL-D-RA, mates with QMS-104-01-SL-D-RA
- J21, P/N QFS-026-01-SL-D-RA, mates with QMS-026-01-SL-D-RA

The signals available on the expansion connector are shown in Expansion connector functions.

**Figure 14. Samtec connector**



*Note: EXPI mode enabled/disabled (refer to Table 21 to configure EXPI mode).*

**Table 14. Expansion connector functions - EXPI mode enabled**

| Pin | Description |
|---|---|
| 4 | PLL_CLK1 ... 3 |
| 8 | No function |
| 33 | MCI expansion 8 ... 15 |
| 2 | NOR parallel Flash (1) |
| 5 | SMI exp CS |
| 4 | Second LCD |
| 30 | Keypad expansion to 9x9 |
| 10 | GPIO |
| | UART modem expansion |

**Table 14. Expansion connector functions - EXPI mode enabled (continued)**

| Pin | Description |
|---|---|
| 1 | Timers |
| 1 | I2S |

1. Usable only with the addition of 15 FSMC signals. To make the 15 FSMC signals available, load resistors R314 through R328, and remove jumper JP4.

**Table 15. Expansion connector functions - EXPI mode not enabled**

| Pin | Description |
|---|---|
| 4 | Keyboard 2x2<br>NAND Flash CE & WPRT |
| 8 | Keyboard expansion to 6x6<br>NAND Flash expansion 8 ... 15 |
| 33 | MCI (memory card interface) |
| 2 | I2C |
| 5 | I2S |
| 4 | SPI |
| 30 | LCD |
| 10 | GPIO |
| 1 | FPGA done (input) |
| 1 | Reset |
| 4 | ADC |
| 2 | MAC I/F |

# 9 Debug interface

The following debug interfaces are provided:

- **The CPU JTAG interface:** this can be used for "static" debug, meaning that it is possible to set a breakpoint and, when the system stops, to verify the contents of the memory and/or registers and modify them if needed.

**Table 16. J15 JTAG connector pin-out**

| Pin number | Signal |
|---|---|
| 1, 2 | VDD3V3 |
| 4 ... 20 | GND |
| 3 | nTRST |
| 5 | TDI |
| 7 | TMS |
| 9 | TCK |
| 13 | TDO |
| 15 | Powergood |
| 11,17,19 | NC |

- **The PCIe JTAG interface**: (reserved)
- **The CPU coresight interface.** (Trace 16 or 32) This can be used for "dynamic" debug. The coresight block embedded in the SPEAr1310 chip sends all the information about the AHB transactions during code execution to the external trace box and the external box stores this information in a local buffer. This makes it possible to stop the CPU activity in order to analyze the program flow. For example, if a particular data abort occurs, you can set a breakpoint on the data abort location and then, when the breakpoint is reached you can analyze the trace buffer. With this information, it becomes a simple task to identify the event that produced the problem.

**Table 17. Debug mode selection**

| Switch5 | | | Description |
|---|---|---|---|
| 3 | 2 | 1 | |
| 0 | 0 | 0 | No debug features available |
| 0 | 0 | 1 | The ARM JTAG is connected to J15 |
| 0 | 1 | 0 | ARM Trace 16bit bus available on J18 and J20 |
| 0 | 1 | 1 | ARM Trace 32bit bus available on J18 and J20 |

# 10 Strapping options

General purpose I/Os are present on the board. They are connected to DIP switches to allow the user to select/deselect them.

Immediately after reset phase, the SPEAr can be configured by means of the GPIO_A0 ... A3 strapping options.

2 µs after reset, pins can be used with GPIO features.

*Note: Important: To use pins as input, the external pin driver must be in tri-state for the duration of the reset phase plus 2 µs.*

**Table 18. Switch 3 (SW3) configuration**

| Pin | Description (default settings) |
|---|---|
| 1 | GPIO_A0 (OFF) (See *Table 20: Software boot options* for description) |
| 2 | GPIO_A1 (ON) (See *Table 20: Software boot options* for description) |
| 3 | GPIO_A2 (ON) (See *Table 20: Software boot options* for description) |
| 4 | GPIO_A3 (ON) (See *Table 20: Software boot options* for description) |
| 8 | Not used |

*Note: When DIP switch SWx-x is in the ON position, the bit value is 0. When the DIP switch is in the OFF position, the bit value is 1.*

**Table 19. Switch 4 (SW4) configuration**

| Pin | Description (default settings) |
|---|---|
| 1 | NAND Flash interface voltage (OFF)<br>OFF = 3.3 volt<br>ON = 1.8 volt |
| 2 | GMII interface 2.5 V (OFF)<br>OFF = 3.3 V<br>ON = 2.5 V |
| 3 | PCI level (to allow a PCI implementation in the SPEAr13x RAS) (OFF)<br>OFF = Normal level<br>ON = PCI level for PL_GPIO[86÷99] [6÷53] |
| 4 | Not used |

**Table 20. Software boot options**

| Boot Type | SW3-4 GPIO_A3 | SW3-3 GPIO_A2 | SW3-2 GPIO_A1 | SW3-1 GPIO_A0 |
|---|---|---|---|---|
| Bypass internal bootROM and jump to code in serial NOR Flash (SMI interface) | 0 | 0 | 0 | 0 |
| Boot from external serial NOR Flash (SMI).If the code not valid, boot from USB is forced. | 0 | 0 | 0 | 1 |

**Table 20. Software boot options (continued)**

| Boot Type | SW3-4 GPIO_A3 | SW3-3 GPIO_A2 | SW3-2 GPIO_A1 | SW3-1 GPIO_A0 |
|---|---|---|---|---|
| Boot from external serial NAND Flash (FSMC). If the code is invalid, boot from USB is forced. | 0 | 0 | 1 | 0 |
| Boot from external serial NOR Flash (FSMC). If the code is invalid, boot from USB is forced. | 0 | 0 | 1 | 1 |
| Boot from I2C (device address). If the code is invalid, boot from USB is forced. | 0 | 1 | 0 | 0 |
| Boot from UART<br>(115 baud, no parity, 8 data bits, 1 stop bit)<br>*Note: Not available on engineering sample devices (ES marking)* | 0 | 1 | 0 | 1 |
| Boot from PCIe device | 0 | 1 | 1 | 0 |
| Reserved | 0 | 1 | 1 | 1 |
| Boot from USB device. (VID PID) | 1 | 0 | 0 | 0 |

# 11 Test modes

At reset, the SPEAr device can be configured in different modes through SW5.

In EXPI mode, the PL_GPIO0 ... 100 pins are mapped to the internal bus signals.

**Table 21. Test modes**

| Boot Type | SW5-4 TEST3 | SW5-3 TEST2 | SW5-2 TEST1 | SW5-1 TEST0 |
|---|---|---|---|---|
| Functional: normal mode | 0 | 0 | 0 | 0 |
| CPU JTAG debug | 0 | 0 | 0 | 1 |
| CPU Trace 16 bits | 0 | 0 | 1 | 0 |
| CPU Trace 32 bits | 0 | 0 | 1 | 1 |
| EXPI mode | 0 | 1 | 0 | 0 |
| EXPI and CPU JTAG debug | 0 | 1 | 0 | 1 |
| EXPI and CPU Trace 16 bits | 0 | 1 | 1 | 0 |
| EXPI and CPU Trace 32 bits | 0 | 1 | 1 | 1 |
| Reserved configurations | 1 | x | x | x |

# 12 LEDs

Several LEDs are present on the board. They display the following status information:

**Table 22. Status LEDs**

| LED | Color | Status displayed |
|---|---|---|
| D1 | Yellow | GIG PHY Duplex |
| D2 | Yellow | GIG PHY link1000 |
| D3 | Yellow | GIG PHY Link100 |
| D4 | Yellow | GIG PHY Link10 |
| D5 | Yellow | GIG PHY Activity |
| D7 | Red | Host1 Overcurrent |
| D8 | Green | USB Host1 5V |
| D9 | Green | USB Host2 5V |
| D10 | Red | USB Host2 Overcurrent |
| D11 | Red | Overvoltage or undervoltage protection activated (STBP120 pin 3) |
| D12 | Green | VDD1V2 |
| D13 | Green | +5V |
| D14 | Green | VDD1V5 |
| D15 | Green | VDD3V3 |
| D16 | Green | VDD2V5 |
| D17 | Green | VDD1V8 |

# 13 Jumper descriptions

The board has the following jumpers for settings or measurements:

**Table 23. List of board jumpers**

| Jumper | Description |
|---|---|
| J23 (4) | M25P64 (U1) nCS select (default 1-2 closed: 3-4 closed) |
| JP1 (3) | SAFHV antifuse (OTP) cell power supply VDD2V5 (default closed 1-2) |
| JP2 (3) | NAND FLASH VDD (default 1-2 closed = 3.3 V) |
| JP3 (3) | NAND FLASH SPEAr I/O (default 1-2 closed = 3.3 V) |
| JP4 (2) | On-board NAND FLASH (U4) closed = enabled |
| JP5 (3) | MIPHY (U5) VDD_IO (default 1-2 closed = 3.3 V) |
| JP6 - JP11 (3+3) | GIGA PHY STRAP13 |
| JP7 - JP12 (3+3) | GIGA PHY STRAP10 |
| JP8 - JP13 (3+3) | GIGA PHY STRAP9 |
| JP9 - JP14 (3+3) | GIGA PHY STRAP8 |
| JP10 - JP15 (3+3) | GIGA PHY STRAP7 |
| JP16 (3) | SPEAr GMII I/F VDD (default 1-2 closed = 3.3 V) |
| JP17 (3) | GMII_COL. (default 1-2 closed = pull up) |
| JP18 (3) | MII_TXCLK_SEL1 (default 2-3 closed) |
| JP19 (3) | CRS_RGMII_SEL0 (default 2-3 closed) |
| JP23 (2) | Power OFF LM2731 (U7) (default open) |
| JP24 (2) | Connect SPEAr_VDD2V5 to MIPHY_VDD2V5_PLL (default open) |
| JP27 (3) | MIPHY_VDD1V2 (default 1-2 closed) |
| JP28 (3) | A2D_PLL_VDD2.5 (default 1-2 closed = internal regulator) |
| JP29 (3) | USB_VDD2V5. (default 1-2closed = internal regulator) |
| JP30 (2) | SPEAr_DDR3_1V2 (default closed) |
| JP31 (2) | SPEAr_VDD1V2 (default closed) |
| JP32 (2) | SPEAr_DDR3_1V5 (default closed) |
| JP33 (2) | SPEAr_VDD2V5 (default closed) |
| JP34 (2) | SPEAr_VDD3V3 (default closed) |
| JP37 (2) | SS_nINH, Power off L5989 (U21) (default open) |
| JP39 (2) | RTC_VDD1V5 (default closed) |
| JP42 | GIG PHY Ethernet power selection (default 1-2 closed = 3.3 V) |
| JP44 (3) | RTC Power Selection (default 1-2 closed) |

# 14 Connectors

**Table 24. List of board connectors**

| Connector | Description |
|---|---|
| J1 | CON32A NAND |
| J2 | RJ45 Ethernet connector |
| J3 | SATA connector |
| J4 | PCIe Root complex (HOST1) |
| J5 | PCIe Endpoint (Device) |
| J6 | +12 V_HOST (PCIe) |
| J7 | MIPHY JTAG Connector |
| J8 | USB Connector Micro A-B (OTG) |
| J10 | USB Connector Type A double |
| J11 | QFS-104-RA Expansion connector |
| J12 | +5 V |
| J13 | +5V |
| J14 | ADC Connector A/D |
| J15 | J15 (20) CPU JTAG |
| J16 | J16 (10) UART |
| J17 | RS232 invert RX<>TX |
| J18 | (Mictor38) Core-sight |
| J19 | Battery connector (1 positive, 2 gnd) |
| J20 | (Mictor38) Core-sight |
| J21 | QFS-026-RA Expansion connector |
| J22 | UART TX and RX probing |

# 15 Pushbuttons

P1 Reset switch (pin 3) STM811 (U16)

P2 Wakeup switch GPIO 7

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# Revision history

Table 25. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 07-Nov-2012 | 1 | Initial release. |