# UM0327
# User manual

## uPSD3300 evaluation board schematics

### Introduction

This manual gives some example schematics for a µPSD3300 evaluation board. You can use the schematics as a starting point for designing your own µPSD3300 application.

# 1 Board schematics

**Figure 1. Board connectors**

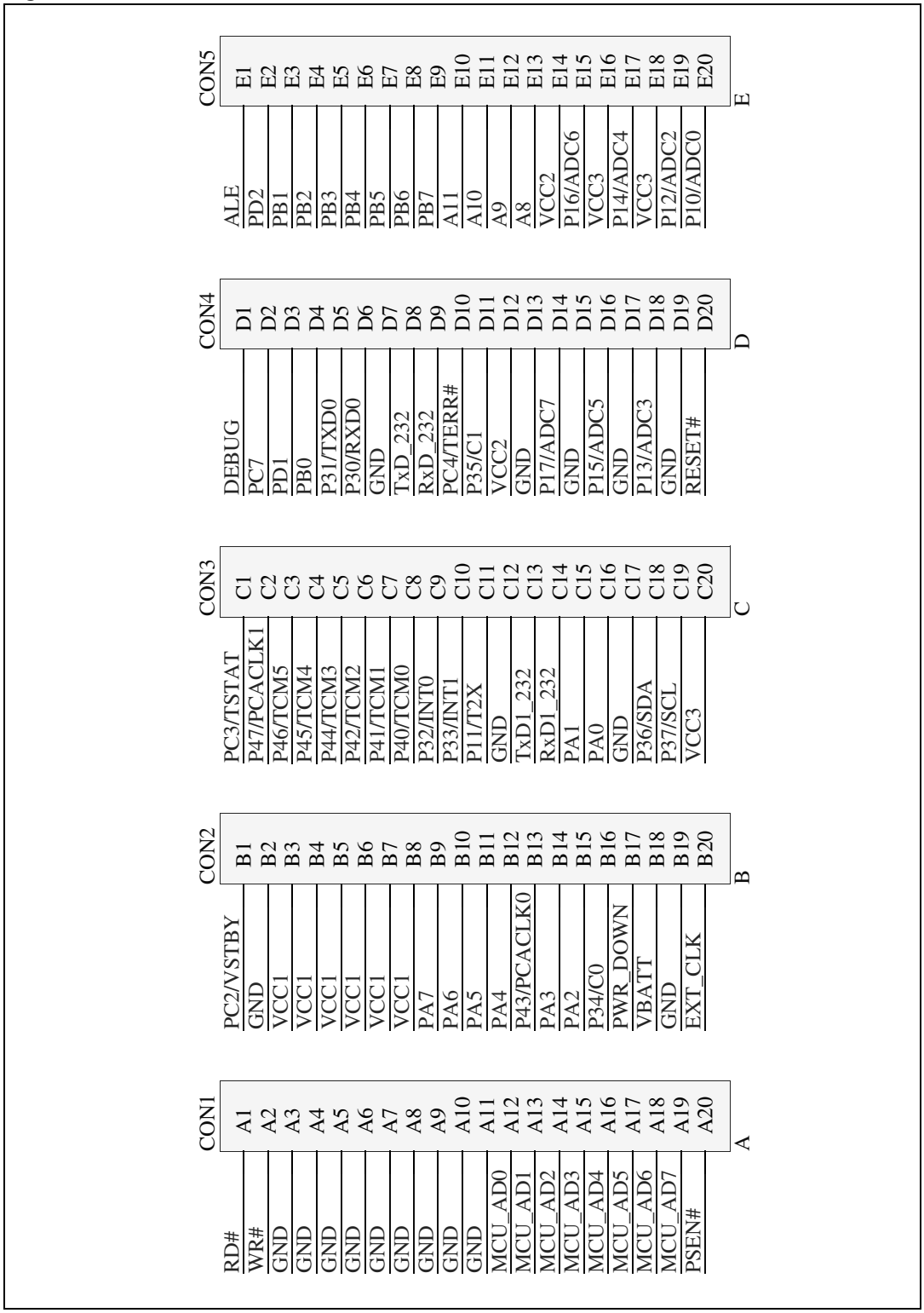


**Figure 2. JTAG interface**

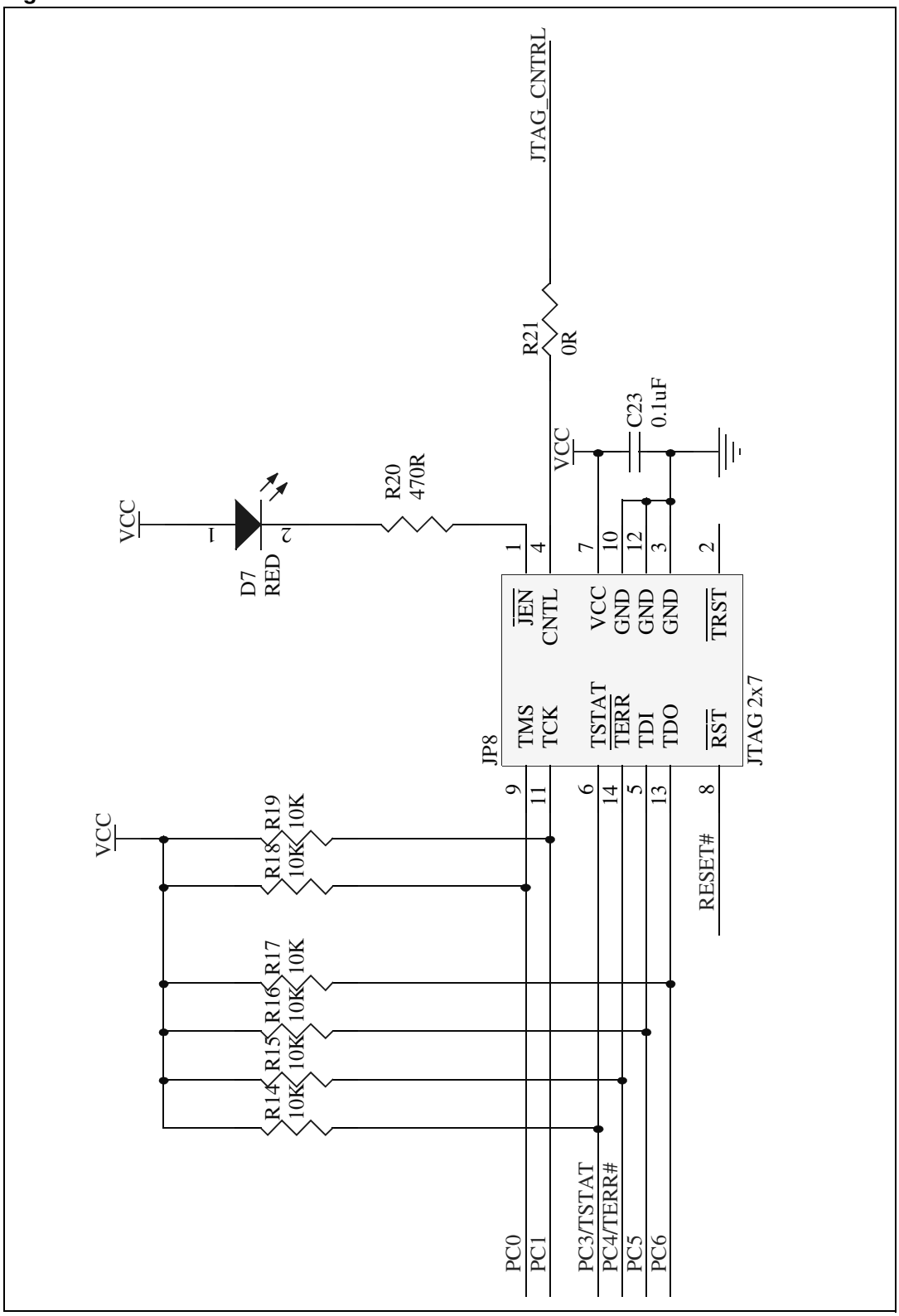


**Figure 3. MCU**

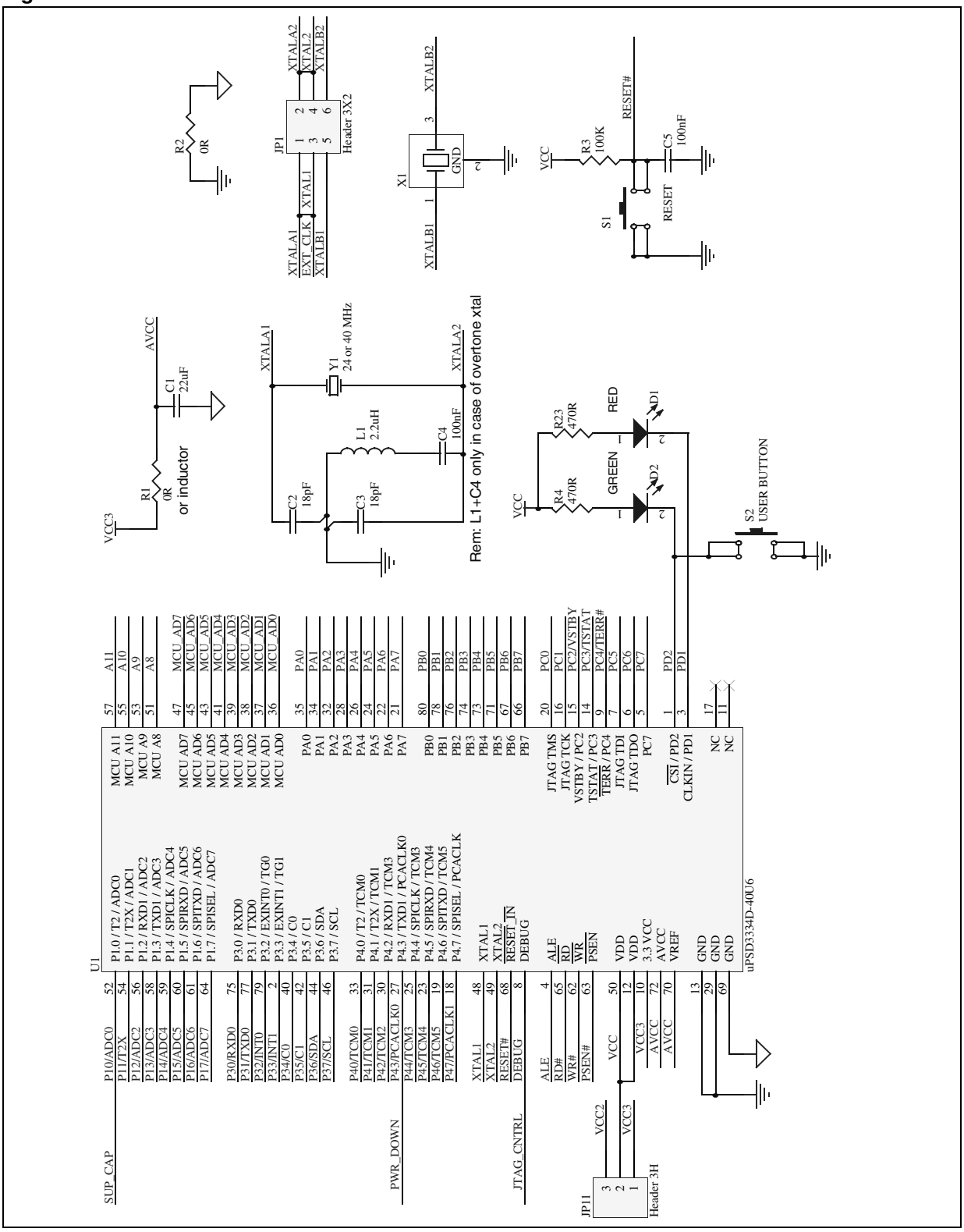

U1
uPSD3334D-40U6
SUP_CAP
PWR_DOWN
JTAG_CNTRL
P10/ADC0 52
P11/T2X 54
P12/ADC2 56
P13/ADC3 58
P14/ADC4 59
P15/ADC5 60
P16/ADC6 61
P17/ADC7 64
P30/RXD0 75
P31/TXD0 77
P32/INT0 79
P33/INT1 2
P34/C0 40
P35/C1 42
P36/SDA 44
P37/SCL 46
P40/TCM0 33
P41/TCM1 31
P42/TCM2 30
P43/PCACLK0 27
P44/TCM3 25
P45/TCM4 23
P46/TCM5 19
P47/PCACLK1 18
XTAL1 48
XTAL2 49
RESET# 68
DEBUG 8
ALE 4
RD# 65
WR# 62
PSEN# 63
VCC 50
VCC3 10
AVCC 72
AVCC 70
13
29
69
P1.0 / T2 / ADC0
P1.1 / T2X / ADC1
P1.2 / RXD1 / ADC2
P1.3 / TXD1 / ADC3
P1.4 / SPICLK / ADC4
P1.5 / SPIRXD / ADC5
P1.6 / SPITXD / ADC6
P1.7 / SPISEL / ADC7
P3.0 / RXD0
P3.1 / TXD0
P3.2 / EXINT0 / TG0
P3.3 / EXINT1 / TG1
P3.4 / C0
P3.5 / C1
P3.6 / SDA
P3.7 / SCL
P4.0 / T2 / TCM0
P4.1 / T2X / TCM1
P4.2 / RXD1 / TCM3
P4.3 / TXD1 / PCACLK0
P4.4 / SPICLK / TCM3
P4.5 / SPIRXD / TCM4
P4.6 / SPITXD / TCM5
P4.7 / SPISEL / PCACLK
XTAL1
XTAL2
RESET_IN
DEBUG
ALE
RD
WR
PSEN
VDD
VDD
3.3 VCC
AVCC
VREF
GND
GND
GND
MCU A11 57
MCU A10 55
MCU A9 53
MCU A8 51
MCU AD7 47
MCU AD6 45
MCU AD5 43
MCU AD4 41
MCU AD3 39
MCU AD2 38
MCU AD1 37
MCU AD0 36
PA0 35
PA1 34
PA2 32
PA3 28
PA4 26
PA5 24
PA6 22
PA7 21
PB0 80
PB1 78
PB2 76
PB3 74
PB4 73
PB5 71
PB6 67
PB7 66
JTAG TMS 20
JTAG TCK 16
VSTBY / PC2 15
TSTAT / PC3 14
TERR / PC4 9
JTAG TDI 7
JTAG TDO 6
PC7 5
CSI / PD2 1
CLKIN / PD1 3
NC 17
NC 11
PC0
PC1
PC2/VSTBY
PC3/TSTAT
PC4/TERR#
PC5
PC6
PC7
PD2
PD1
JP11
Header 3H
VCC2
VCC3
VCC3
R1 0R
or inductor
C1 22uF
AVCC
VCC3
XTALA1
XTALA2
Y1 24 or 40 MHz
C2 18pF
C3 18pF
L1 2.2uH
C4 100nF
Rem: L1+C4 only in case of overtone xtal
R2 0R
JP1
Header 3X2
XTALA1
EXT_CLK
XTALB1
XTAL1
XTAL2
XTALB2
X1
GND
XTALB1
XTALB2
VCC
R3 100K
RESET#
C5 100nF
S1
RESET
VCC
R4 470R
R23 470R
GREEN
RED
D1
D2
S2
USER BUTTON

**Figure 4. Power**

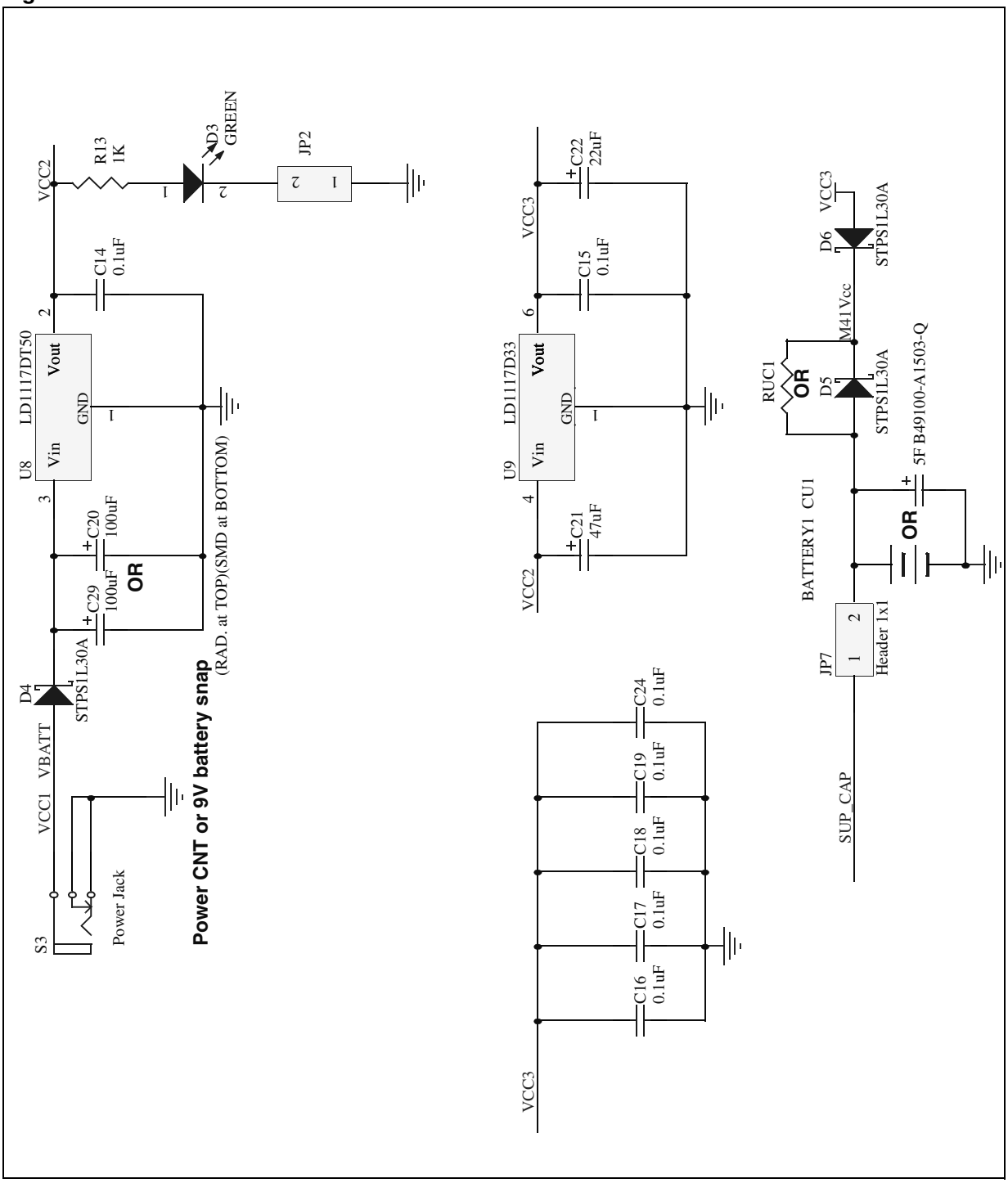


**Figure 5. NAND Flash**

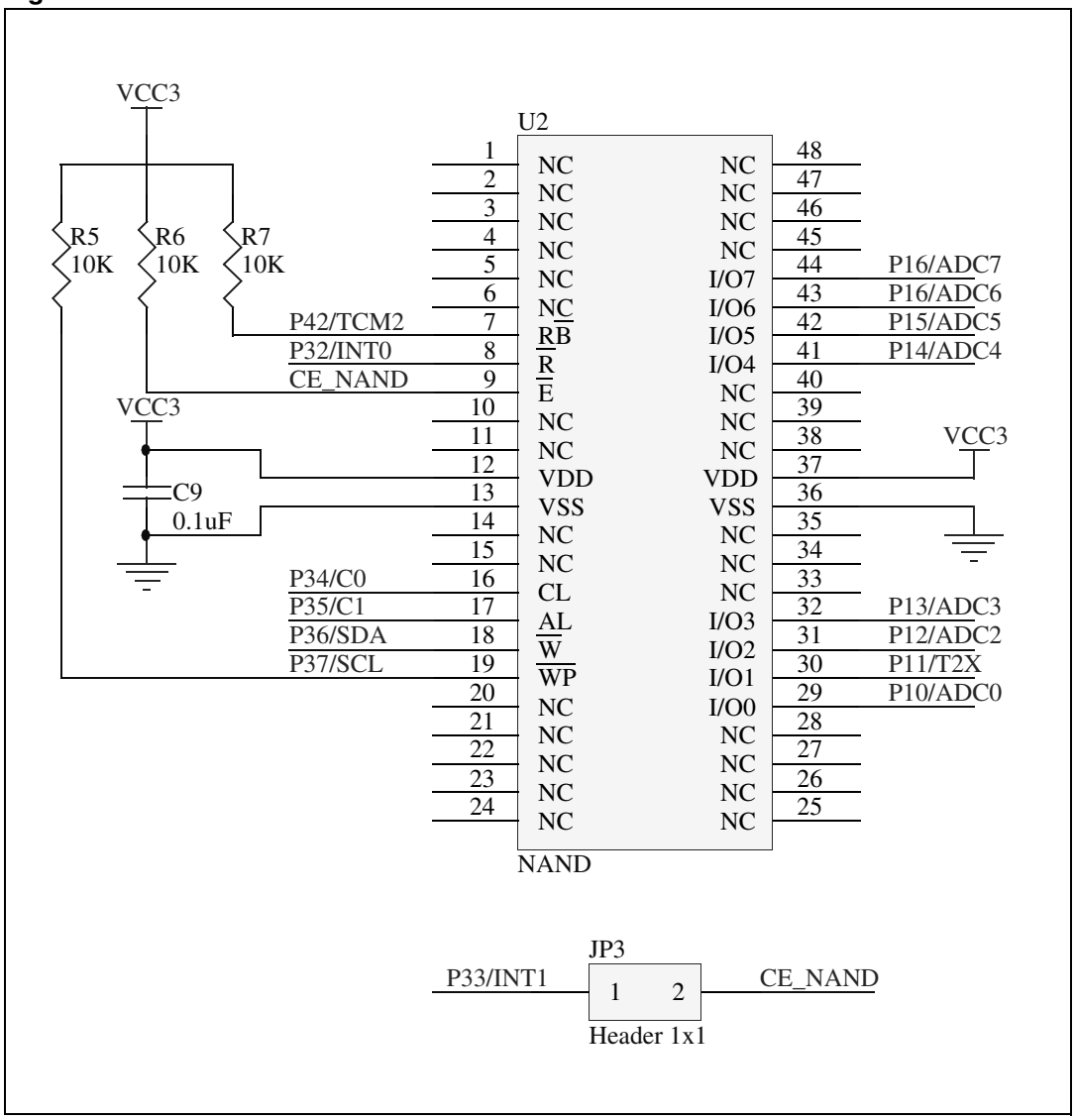


**Figure 6. SPI Flash**

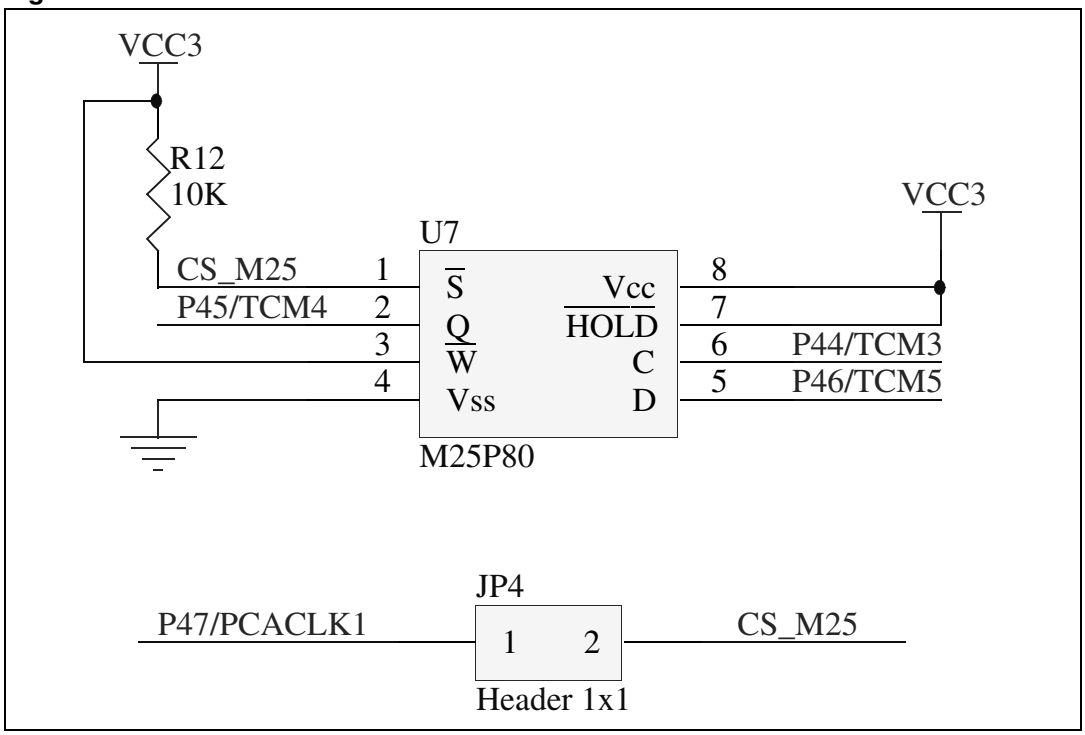


**Figure 7. RS232C IrDA**

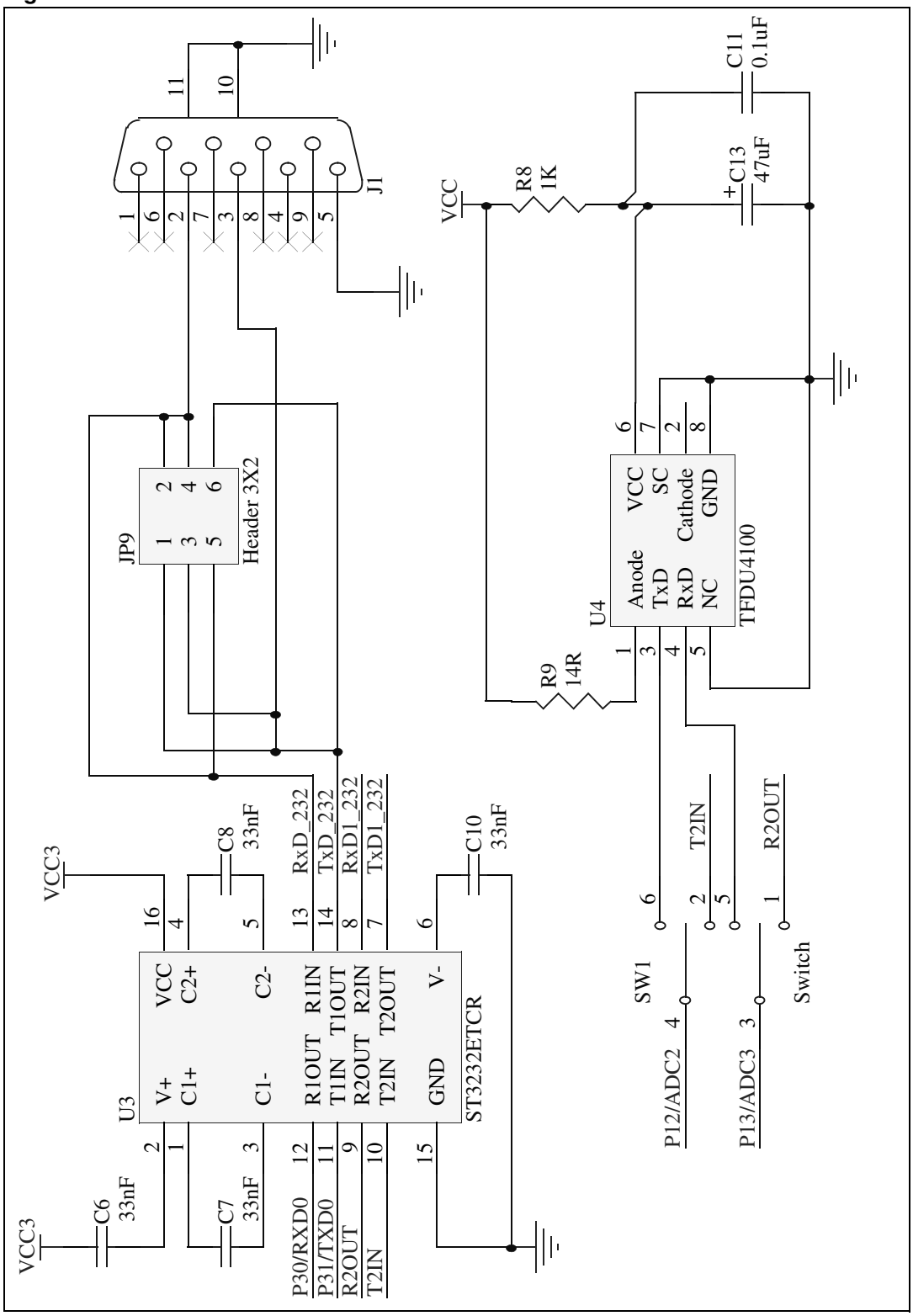
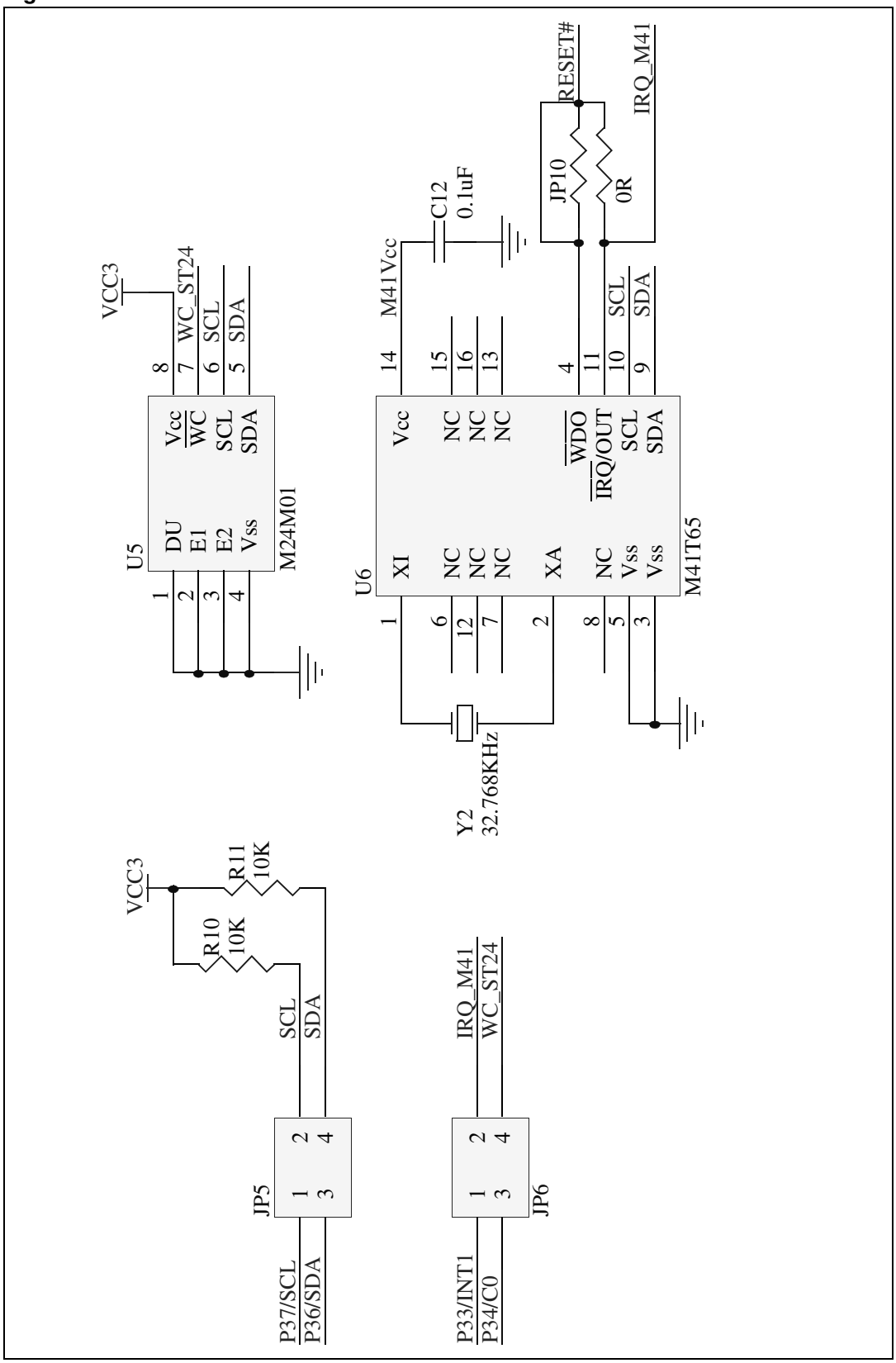


**Figure 8. I2C/RTC/EEPROM**



# 2 Revision history

**Table 1. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 30-Apr-2007 | 1 | Initial release. |
| 22-Aug-2007 | 2 | Modified presentation of schematics |

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