Article

Hardware-efficient quantum error correction via concatenated bosonic qubits

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To solve problems of practical importance[1,2], quantum computers probably need to incorporate quantum error correction, in which a logical qubit is redundantly encoded in many noisy physical qubits[3–5]. The large physical-qubit overhead associated with error correction motivates the search for more hardware-efficient approaches[6–18]. Here, using a superconducting quantum circuit[19], we realize a logical qubit memory formed from the concatenation of encoded bosonic cat qubits with an outer repetition code of distance $d = 5$ (ref. 10). A stabilizing circuit passively protects cat qubits against bit flips[20–24]. The repetition code, using ancilla transmons for syndrome measurement, corrects cat qubit phase flips. We study the performance and scaling of the logical qubit memory, finding that the phase-flip correcting repetition code operates below the threshold. The logical bit-flip error is suppressed with increasing cat qubit mean photon number, enabled by our realization of a cat-transmon noise-biased CX gate. The minimum measured logical error per cycle is on average 1.75(2)% for the distance-3 code sections, and 1.65(3)% for the distance-5 code. Despite the increased number of fault locations of the distance-5 code, the high degree of noise bias preserved during error correction enables comparable performance. These results, where the intrinsic error suppression of the bosonic encodings enables us to use a hardware-efficient outer error-correcting code, indicate that concatenated bosonic codes can be a compelling model for reaching fault-tolerant quantum computation.

For quantum computers to solve problems in materials design, quantum chemistry and cryptography, in which known speed-ups relative to classical computations are attainable, currently proposed algorithms require trillions of qubit gate operations to be applied in an error-free manner[1,2]. Despite impressive progress over the past few decades in reducing qubit error rates at the physical hardware level, the state-of-the-art remains about nine orders of magnitude away from these requirements. A path towards closing the error-rate gap is through quantum error correction (QEC)[3–5], which can exponentially suppress errors through the redundant encoding of information across many noisy physical qubits.

Recently, QEC experiments have been performed in various hardware platforms, including superconducting quantum circuits[25–28], trapped ions[29] and neutral atoms[30]. Some of these experiments are approaching[26], or have surpassed[28], the threshold at which scaling of the error-correcting code size leads to exponential improvements in the logical qubit error rate. In these experiments, the qubits are realized using a simple encoding into two levels of a physical element, leaving them susceptible to environmental noise that can cause both bit and phase-flip errors. Correcting for both types of error requires QEC codes such as the surface code[25–27], which have a relatively high overhead penalty[1].

Alternatively, we can use a layered approach to noise protection by starting from an encoded qubit that natively suppresses errors. An example is bosonic qubits, in which qubit states are encoded in the infinite-dimensional Hilbert space of a bosonic mode (a quantum harmonic oscillator) using bosonic QEC[6,31,32]. In bosonic QEC, the large oscillator Hilbert space is exploited to suppress errors. Experiments demonstrating this exploitation at the single bosonic mode level have been performed using cat codes[21–23,33–35], binomial codes[36] and GKP codes[37–39]. At the same time, various proposals have been put forward to further scale bosonic QEC by concatenating it with an outer code across multiple bosonic modes[6,8–16,18,40], leveraging the protection offered in each bosonic mode to reduce the overall resource overhead for QEC.

In this work, we demonstrate a scalable, hardware-efficient logical qubit memory built from a linear array of bosonic modes using a variant of the repetition cat code proposal in ref. 10. In particular, we stabilize noise-biased cat qubits in individual bosonic modes. Bit-flip errors of the cat qubits are natively suppressed at the physical level, and the remaining phase-flip errors are corrected by an outer repetition code. The use of a repetition code enables low overhead because of its large error rate threshold and linear scaling of code distance with physical qubit number[10,12,15]. In what follows, we describe a microfabricated superconducting quantum circuit that realizes a distance $d = 5$ repetition cat code logical qubit memory, present a noise-biased CX gate for implementing error syndrome measurements with ancilla transmons and study the logical qubit error correction performance.

Quantum device realizing a distance-5 repetition code

A schematic of our repetition code device and the corresponding superconducting circuit layout are shown in Fig. 1. The distance $d = 5$ repetition code consists of five bosonic modes that host the data qubits (blue), along with four ancilla qubits (orange). The bosonic modes,

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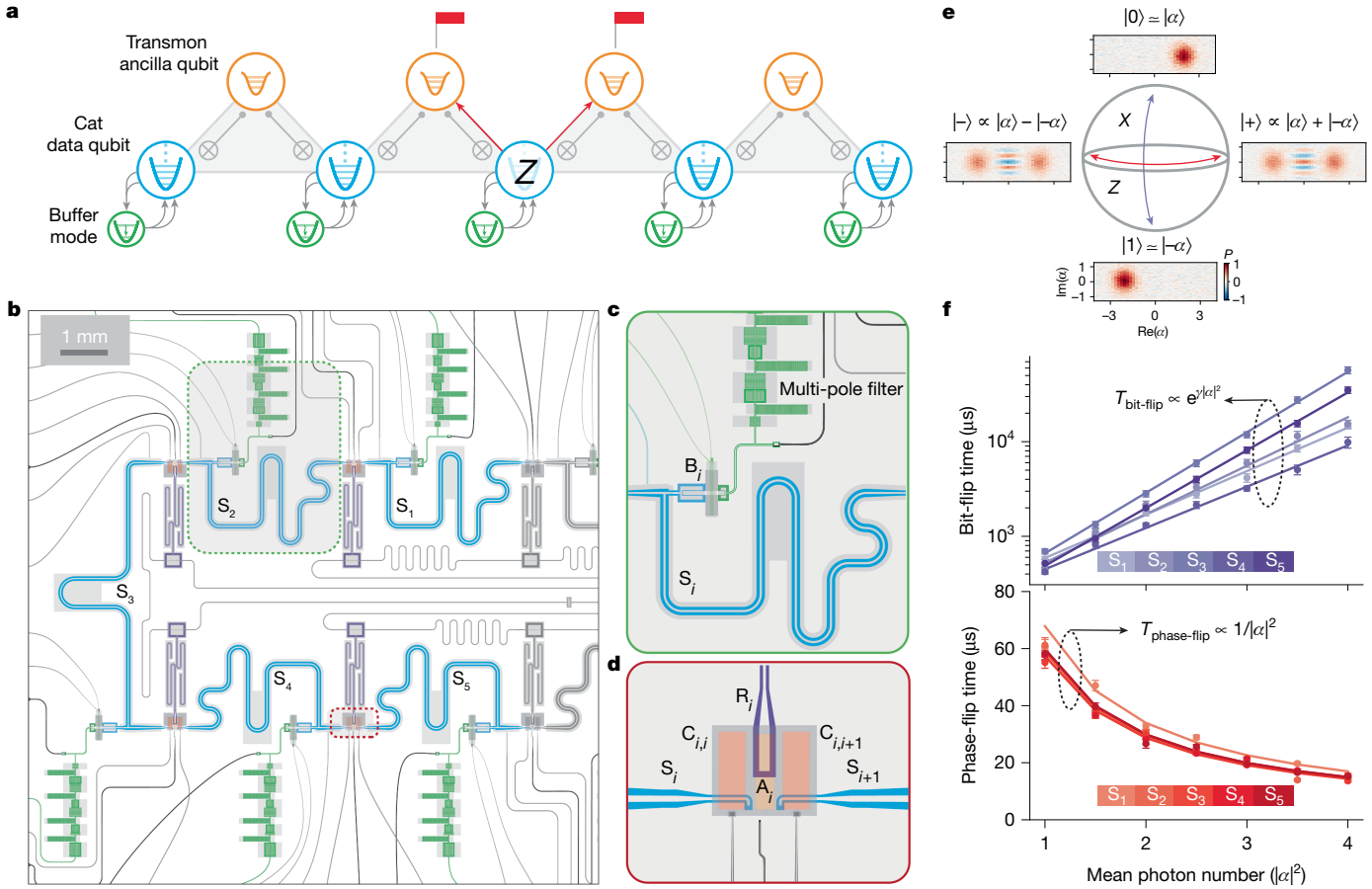

Fig. 1 | Repetition code of bosonic qubits. a, Schematic of the repetition code device. Data qubits S_1, ..., S_5 (blue) are encoded into the Hilbert space of a quantum harmonic oscillator. Each cat qubit is stabilized by a buffer mode B_1, ..., B_5 (green). The ancilla qubits A_1, ..., A_4 (orange) are transmon qubits that detect Z errors (see example with red arrows) on the data qubits by measuring repetition-code stabilizers. **b**, Circuit layout of the repetition code device using a flip-chip architecture (Supplementary Information). The five bosonic modes (S_i) are coplanar waveguide resonators. Each resonator is connected to a buffer mode (B_i). Buffer modes are damped through a multi-pole filter. Ancilla transmons (A_i) are connected to the storage modes by tunable couplers ($C_{i,j}$). Scale bar, 1 mm. **c**,**d**, Magnified circuit sections showing a storage-buffer subsystem (**c**) and an ancilla transmon coupled to its neighbouring storage modes by tunable couplers (**d**). **e**, Cat qubit encoding in a bosonic mode with experimentally measured Wigner functions of the four basis states of a cat qubit and arrows representing X and Z errors. **f**, Bit-flip and phase-flip times of the five cat qubits in our device under simultaneous two-photon dissipation. Error bars (standard error) incorporate sampling and fit error.

also referred to as storage modes, are coplanar waveguide resonators with an average T_1 time of more than 60 μs and an average T_2 time of more than 80 μs. The ancilla qubits are fixed-frequency transmons and are coupled to the storage modes by tunable-transmon couplers[41,42] that realize a tunable dispersive coupling (see ref. 24 and Supplementary Information). This dispersive interaction is used for a controlled-X operation (CX gate), with the ancilla transmon as the control and the data qubit as the target. Using the CX gates, we measure the repetition code stabilizers $\hat{X}_i\hat{X}_{i+1}$ (grey triangles), equivalent to measuring the joint photon-number parity of two neighbouring storage modes. Each ancilla qubit can be read out and reset through a readout resonator[43,44].

Each data qubit in our system is a cat qubit encoded in storage mode[20–22]. The basis states of a cat qubit are shown in Fig. 1e along with their experimental Wigner tomograms[45]. The $|0\rangle$ and $|1\rangle$ computational basis states are approximately the $|\alpha\rangle$ and $|-\alpha\rangle$ coherent states, respectively, with a mean photon number of $|\alpha|^2$. The complementary basis states are exactly the even and odd cat states $|\pm\rangle \propto |\alpha\rangle \pm |-\alpha\rangle$. Thus, a bit-flip ($X$) error is a 180° rotation in the phase space mapping $|\alpha\rangle \leftrightarrow |-\alpha\rangle$, and a phase-flip ($Z$) error corresponds to a parity flip between the even and odd cat states. Owing to the phase-space separation of the $|\pm\alpha\rangle$ coherent states, bit-flip error rates can be exponentially suppressed with cat size $|\alpha|^2$ (refs. 23,24,34,35). By contrast, phase-flip errors, which are caused by single-photon loss and heating, have a rate that increases linearly with $|\alpha|^2$.

To ensure that their noise bias is maintained over time, the cats are stabilized using two-photon dissipation, confining them to the $|\pm\alpha\rangle$ manifold[20–22]. To realize the two-photon dissipation, we nonlinearly couple each storage mode to a lossy buffer mode (green), which is implemented using a version of the asymmetrically threaded SQUID element[23,24]. Our buffer mode implementation ensures that the storage-mode lifetime and linearity are not degraded by the coupling to the lossy and nonlinear buffer (see ref. 24 and Supplementary Information).

Figure 1f shows the bit-flip and phase-flip times of all five data cat qubits when they are being simultaneously stabilized by two-photon dissipation. Over the range of $|\alpha|^2$ considered, the bit-flip times of our cat qubits increase exponentially with the mean photon number $|\alpha|^2$. As expected, the phase-flip times degrade as $T_{1,\mathrm{eff}}/|\alpha|^2$, where the effective storage lifetimes under two-photon dissipation, $T_{1,\mathrm{eff}}$, are in the range 57–68 μs. A particularly important feature of our cat qubits is that a large noise bias is achieved even with small values of $|\alpha|^2$. Concretely, at $|\alpha|^2 = 2$, we achieve greater than 1 ms bit-flip times and 27–33 μs phase-flip times. This constitutes a sizable (>30) noise bias and at the same time a long phase-flip time in comparison to an error correction cycle time (2–3 μs).

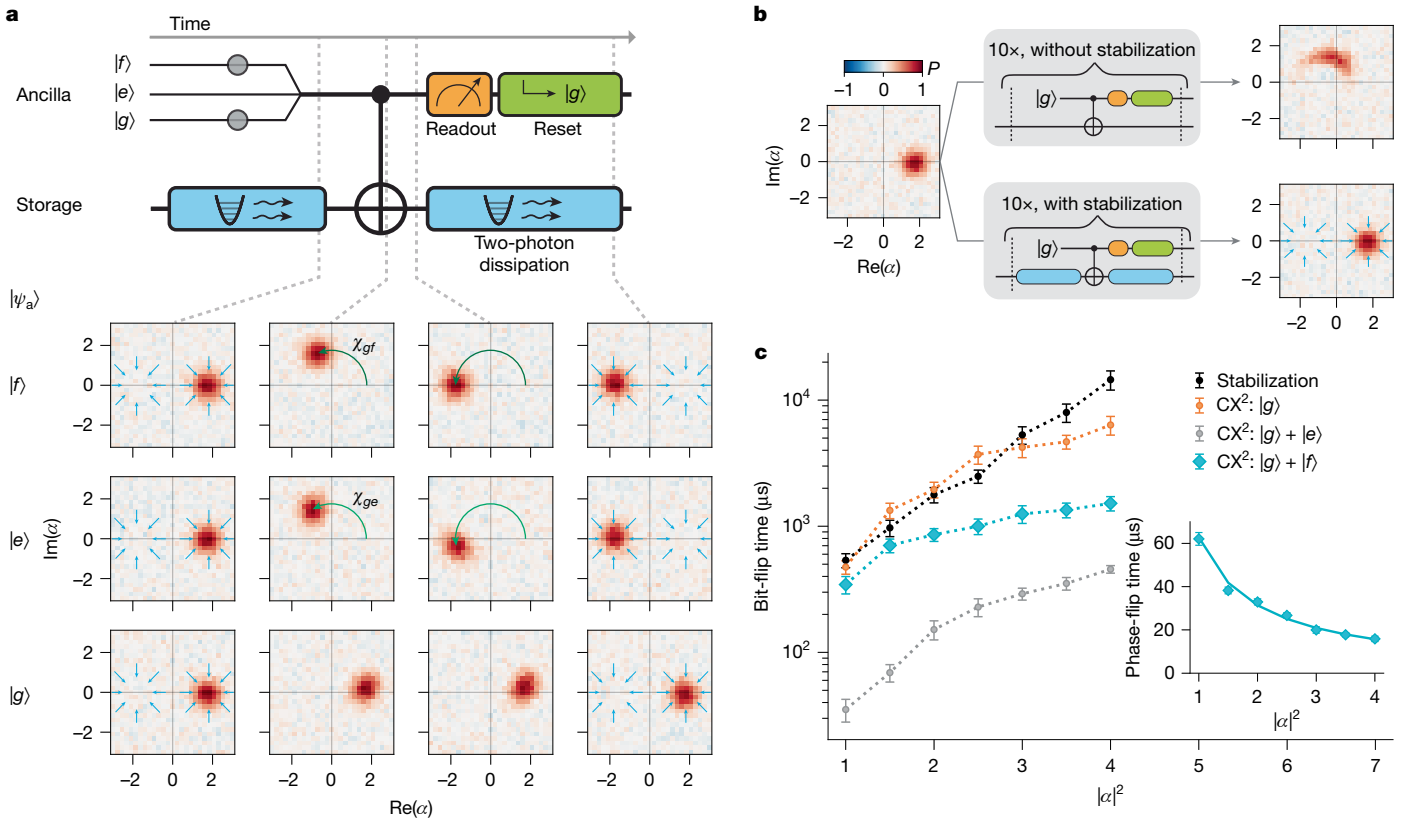

Fig. 2 | Noise-biased CX gate between a transmon and a cat qubit. a, CX gate sequence. At the start of the sequence, the ancilla is initialized and cat qubit stabilization (blue arrows) is on. The stabilization is then turned off and the CX gate is applied between the ancilla and cat qubit. After the CX gate, the stabilization is turned back on and the ancilla qubit is read out and reset to $|g\rangle$. Through the experimentally measured Wigner functions, we show the evolution of the storage state during the sequence for each of the ancilla states $|g\rangle$, $|e\rangle$ and $|f\rangle$, with an initial storage-mode state $|\alpha\rangle$. **b**, Storage-mode Wigner tomograms before and after 10 applications of the CX gate sequence with the ancilla in $|g\rangle$ and storage initialized in $|\alpha\rangle$. The sequence is applied with and without stabilization. **c**, Characterization of the CX gate. We apply repeated CX^2 cycles (see main text) with a cycle duration of 3 μs and plot the measured bit-flip time of the cat qubit as a function of cat qubit photon number, $|\alpha|^2$, for different ancilla states. The inset shows the measured phase-flip times (points) and a fit (line) when the ancilla is initialized to $|g\rangle + |f\rangle$. Error bars (standard error) incorporate sampling and fit errors. **a** and **b** use the same colour bar.

Noise-biased CX gates in the repetition cat code

Syndrome measurements require a CX gate between a data cat qubit and an ancilla qubit with computational states $|0_a\rangle$ and $|1_a\rangle$. This requires us to realize a noise-biased CX gate that minimizes undesired bit flips on the target cat qubit caused by ancilla errors. Although cat qubits can be used as ancilla qubits to implement noise-biased CX gates, these gates can induce substantial control errors and require a complex drive scheme[10,11,15].

To avoid this issue, we use transmons as ancilla qubits whose lowest three energy eigenstates are denoted by $|g\rangle$, $|e\rangle$ and $|f\rangle$. We realize the CX gate with a storage-ancilla dispersive coupling in which the data cat qubit rotates by 180° conditional on the ancilla being in $|1_a\rangle$ (refs. 46–48). As in refs. 49–51, we encode the ancilla qubit into the states $|0_a\rangle = |g\rangle$ and $|1_a\rangle = |f\rangle$ and engineer an approximately χ-matched dispersive interaction between the ancilla and the storage mode. The χ-matching means the storage frequency shift is similar for the ancilla in $|e\rangle$ and $|f\rangle$ and thus the noise bias of a CX gate is robust against the dominant ancilla decay events. Only subleading ancilla error mechanisms such as two sequential decay events and heating will cause bit-flip errors on the data cat qubit. In our implementation, the dispersive interaction is tunable, the χ-matching is natively realized without drives, and dissipative protection allows for robustness to inexact χ-matching (Supplementary Information).

Figure 2a shows a control sequence involving a CX gate similar to that used for an error correction syndrome measurement. We illustrate the robustness of our CX gate to ancilla decay by measuring the action of the gate on initial state $|\alpha\rangle \otimes |g, e, \text{or } f\rangle$ of the storage mode and ancilla. Before the CX gate begins, we turn off the cat qubit stabilization to allow the storage mode to rotate freely. Then we activate the CX gate by applying a flux pulse on the tunable coupler. As shown by the Wigner tomograms, the storage mode does not rotate when the ancilla is in $|g\rangle$, whereas it rotates by approximately 180° over the course of a CX gate when the ancilla is in $|e\rangle$ or $|f\rangle$. Owing to the imperfect χ-matching, the storage mode has slightly overrotated when the ancilla is in $|e\rangle$. Moreover, miscalibrations, self-Kerr nonlinearities and decoherence can cause mis-rotations and distortion of the storage-mode states. Notably, all these imperfections can be corrected with high probability when the two-photon dissipation is turned back on after the CX gate, as shown in the last column of the Wigner tomograms. To further highlight the importance of applying the two-photon dissipation, Fig. 2b shows the results of 10 repetitions of the CX gate cycle with and without the pulsed cat qubit stabilization. Without stabilization, errors accumulate over multiple rounds causing large distortion in the final storage mode state. With stabilization applied in every cycle, the storage mode stays well confined to the ideal target coherent state.

We quantify the performance of our CX gate by repeatedly applying the pulse sequence of Fig. 2a except with the single CX replaced by a single pulse that is the equivalent of two CX gates (a CX^2 gate) (Supplementary Information). This ensures that, similar to a stabilizer measurement, cat bit-flip times are first-order insensitive to ancilla state preparation errors.

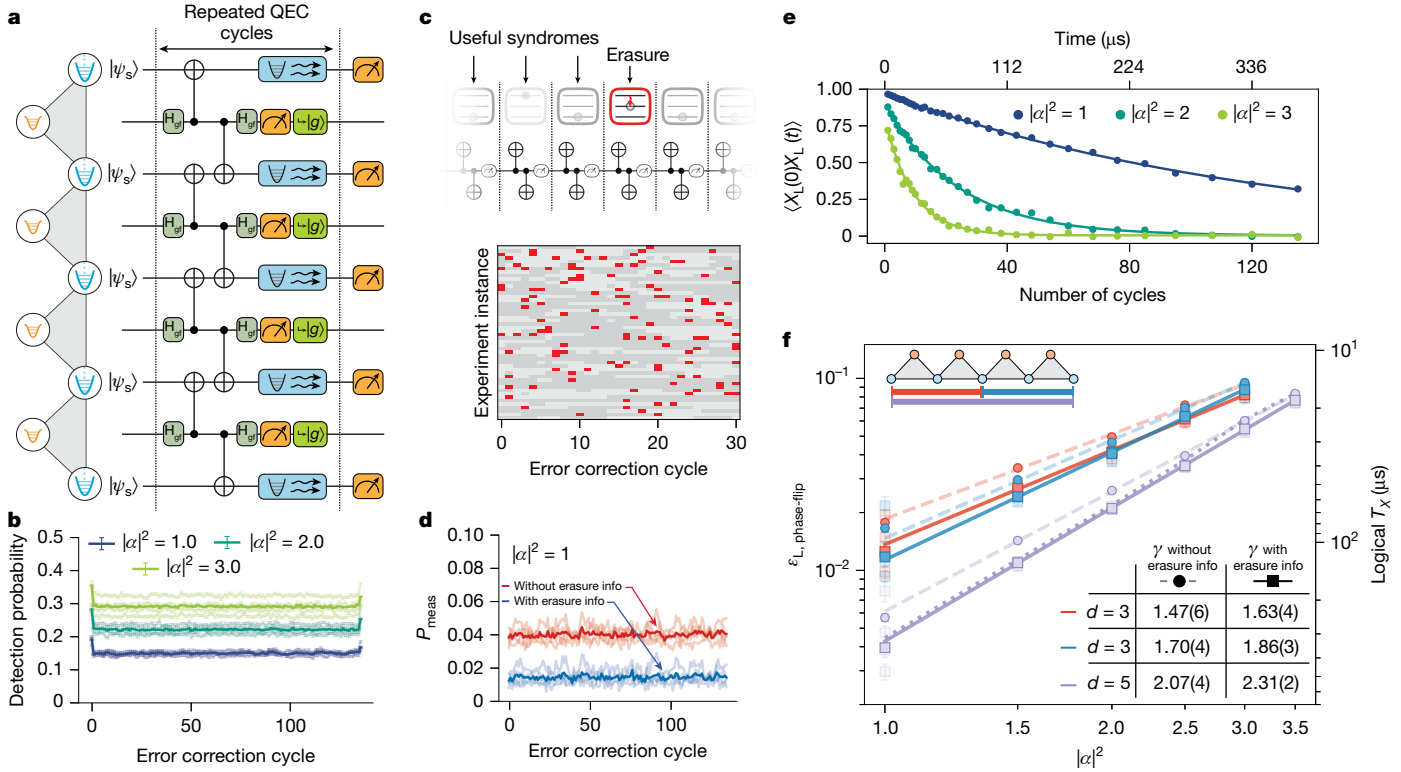

Fig. 3 | Detecting and correcting phase-flip errors with the repetition code. **a**, Error correction circuit, showing repeated error correction cycles with a duration of 2.8 μs. **b**, Detection probabilities for the measured stabilizers versus error correction cycle for three different cat qubit photon numbers, $|\alpha|^2 = 1, 2$ and 3. Bold traces correspond to the average over the individual stabilizer traces. Error bars represent the standard error of the mean. **c**, Depiction of erasures occurring in the repetition code experiment due to ancilla decay from $|f\rangle$ to $|e\rangle$. We show shots of the experiment from a representative stabilizer, in which $|f\rangle$ is light grey, $|g\rangle$ is dark grey and the erasure state $|e\rangle$ is shown in red. **d**, Effective syndrome measurement error extracted from the QEC graph before and after accounting for the erasure for $|\alpha|^2 = 1$. Bold traces correspond to averaging over the stabilizers. **e**, Example fits of the decay of the X logical operator for the distance-5 repetition code for different photon numbers. **f**, Error corrected logical phase-flip probability per cycle ($\epsilon_{L,\text{phase-flip}}$) and logical X lifetime (T_X) as a function of $|\alpha|^2$ for the different repetition code sections. Data and fits are shown with (squares and solid curves) and without (circles and dashed curves) inclusion of erasure information. The fits are to the power law $(|\alpha|^2)^\gamma$ for $|\alpha|^2 \geq 1.5$. Faded points indicate fits binned by the number of even cat states $|+\rangle$ in the initial state and serve to indicate the spread from asymmetric error rates at low photon numbers (Supplementary Information). The dotted purple curve shows the simulated logical phase-flip probability for the distance-5 section. Error bars (standard error) incorporate sampling and fit errors.

Figure 2c shows bit-flip times measured during repeated CX^2 cycles for a representative interaction between ancilla A_1 and storage S_1. Each cycle has a length of 3 μs. We measure the bit-flip times with the ancilla in state $|g\rangle + |f\rangle$, as would be used for syndrome extraction, and control experiments with the ancilla in $|g\rangle$ and $|g\rangle + |e\rangle$. The black curve is a reference showing the bit-flip times in the case for which the two-photon dissipation is continually applied (as in Fig. 1d). When the gates are applied with the ancilla in $|g\rangle$, bit-flip times exceeding 5 ms are achieved. The degradation relative to the reference performance at $|\alpha|^2 \gtrsim 3$ is because of ancilla or coupler heating during the CX^2 gate. With the ancilla in $|g\rangle + |e\rangle$, bit-flip times are severely limited to well under 1 ms because of the storage dephasing caused by the $|e\rangle \rightarrow |g\rangle$ decay errors of the ancilla. With the initial ancilla state $|g\rangle + |f\rangle$, we recover bit-flip times over 1 ms at $|\alpha|^2 \gtrsim 3$ because of the insensitivity to the $|f\rangle \rightarrow |e\rangle$ decay events of the ancilla afforded by χ-matching (here $\chi_{ge}/\chi_{gf} \approx 1.1$; Supplementary Information). The remaining ancilla-induced errors are from higher-order mechanisms such as double decay. In Fig. 2c (inset), we also show the corresponding phase-flip times with the ancilla in the state $|g\rangle + |f\rangle$. An effective storage lifetime $T_{1,\text{eff}}$ of 63 ± 2 μs is inferred, showing no substantial difference from $T_{1,\text{eff}} = 68 \pm 2$ μs measured in Fig. 1 in the absence of CX^2 gate application. The corresponding bit- and phase-flip errors per cycle are $(3.5 \pm 0.4) \times 10^{-3}$ and $(9.6 \pm 0.4) \times 10^{-2}$, respectively, at $|\alpha|^2 = 2$, corresponding to a noise bias greater than 25.

Correcting phase-flip errors with the repetition code

Equipped with the noise-biased CX gates, we now demonstrate the ability to correct the dominant phase-flip errors using a repetition code. Phase-flip errors are detected by repeatedly measuring the stabilizer generators of the repetition code, $\hat{X}_i\hat{X}_{i+1}$ (for $i = 1, \ldots, d-1$). As shown in Fig. 3a, each measurement of a stabilizer generator, referred to as a syndrome measurement, comprises initialization of the ancilla A_i, two CX gates between A_i and its adjacent data qubits S_i and S_{i+1}, and finally measurement and reset of the ancilla. During the measurement and reset, we turn on the dissipative stabilization on all the cat qubits. Each syndrome measurement cycle has a conservatively chosen duration of 2.8 μs (Supplementary Information).

After running an experiment with many error correction cycles, we decode the syndrome measurements using minimum-weight perfect matching (MWPM)[52,53]. As the first step in this decoding process, we compare the outcomes of consecutive syndrome measurements. Consecutive measurement outcomes that differ indicate an error and are referred to as detection events[54].

In Fig. 3b, we plot the probability of detection events over time for each ancilla and for different values of $|\alpha|^2$. These probabilities increase with $|\alpha|^2$, reflecting that the phase-flip error rates of the cat qubits scale with photon number. Notably, the detection probabilities in our system are approximately constant over time. We attribute the constant

detection probabilities here to the dissipative stabilization of the cat qubits, which prevents the accumulation of leakage out of the cat qubit subspace without requiring additional protocols for active leakage suppression[55,56].

Further improvements in error decoding can be achieved by making use of the fact that $|f\rangle \rightarrow |e\rangle$ ancilla transmon decay errors constitute detectable erasure errors[57,58] as shown in Fig. 3c. Specifically, although the χ-matching ensures that decay to $|e\rangle$ is unlikely to cause a bit-flip error, the decay has a high probability (about 50%) to cause a syndrome measurement error. We detect these erasures using a three-state transmon readout that separately resolves $|g\rangle$, $|e\rangle$ and $|f\rangle$. The heatmap shows the occurrence of erasure events (indicated in red) interspersed among valid syndromes in the data (grey shades). We account for these erasures in decoding by only using the non-erased syndromes (Supplementary Information). As shown in Fig. 3d, doing so effectively reduces the syndrome measurement error probability by over a factor of two for $|\alpha|^2 = 1$.

We characterize the ability of the repetition code to correct cat qubit phase-flip errors by measuring the decay time of the repetition code logical operator $\hat{X}_L = \hat{X}_1$. We prepare the repetition code into a randomly chosen one of the 2^d possible product cat states (for example, $|+\rangle|-\rangle|-\rangle|+\rangle|+\rangle$), perform a variable number of QEC cycles, and finally measure the parity of each storage-mode state (Supplementary Information). Corrections from the MWPM decoding are applied in the software. We fit $\langle \hat{X}_L(t=0)\hat{X}_L(t=t)\rangle$ to a decaying exponential and define the decay time constant, T_X, as the logical X lifetime (Fig. 3e). From T_X, we compute the logical phase-flip error per cycle as $\epsilon_{L,\text{phase-flip}} = T_{\text{cycle}}/(2T_X)$.

We can study the performance of the error-correcting code in situ because we can tune the data qubit phase-flip error rate by varying $|\alpha|^2$. In Fig. 3f, we plot the measured $\epsilon_{L,\text{phase-flip}}$ versus $|\alpha|^2$ for the distance-5 repetition code and the two minimally overlapping distance-3 repetition codes contained within it. As expected, as the photon number increases, the logical error probability increases because the cat qubit phase-flip rates increase. Across the measured range of $|\alpha|^2$, we find that the distance-5 code outperforms the distance-3 subsections. This indicates that the physical phase-flip error rates of our system are below the error threshold of the repetition code for this range of $|\alpha|^2$. Note also that there is a sizable reduction in the logical phase-flip rate when the erasure information is incorporated (for example, by about 20% at $|\alpha|^2 = 1.5$ for $d = 5$), a result of the reduced effective measurement error probabilities.

More quantitatively, the logical phase-flip rate is expected to scale as $(|\alpha|^2)^\gamma$ (refs. 53,59), where $|\alpha|^2$ is a proxy for the cat qubit phase-flip error rate. When the erasure information is incorporated, we estimate from fits to the measured logical phase-flip probability versus $|\alpha|^2$, scaling exponents of $\gamma = 1.63 \pm 0.04$ and $\gamma = 1.86 \pm 0.03$ in the two $d = 3$ subsections, and $\gamma = 2.31 \pm 0.02$ in the full $d = 5$ section. The increase in scaling exponent from $d = 3$ to $d = 5$ shows that the increased code distance is providing greater resiliency to phase-flip errors. Although the measured values of γ are lower than the ideal values, $\gamma = (d+1)/2$, they are consistent with simulations (shown in Fig. 3f as a dotted purple curve for the distance-5 code) based on a simple model that incorporates the measured probabilities of cat phase flips, ancilla erasures and syndrome measurement error.

Maintaining long bit-flip times in a repetition cat code

Having demonstrated the ability to correct the dominant phase-flip errors of cat qubits using a repetition code, we now characterize the logical bit-flip rates. Unlike the logical phase flips that are corrected using the repetition code syndrome measurements, logical bit flips are passively suppressed at the level of the individual cat qubit encodings. As a result, achieving long logical bit-flip times is challenging because any single cat qubit bit-flip event in any part of the repetition code directly causes a logical bit-flip error. We now demonstrate that

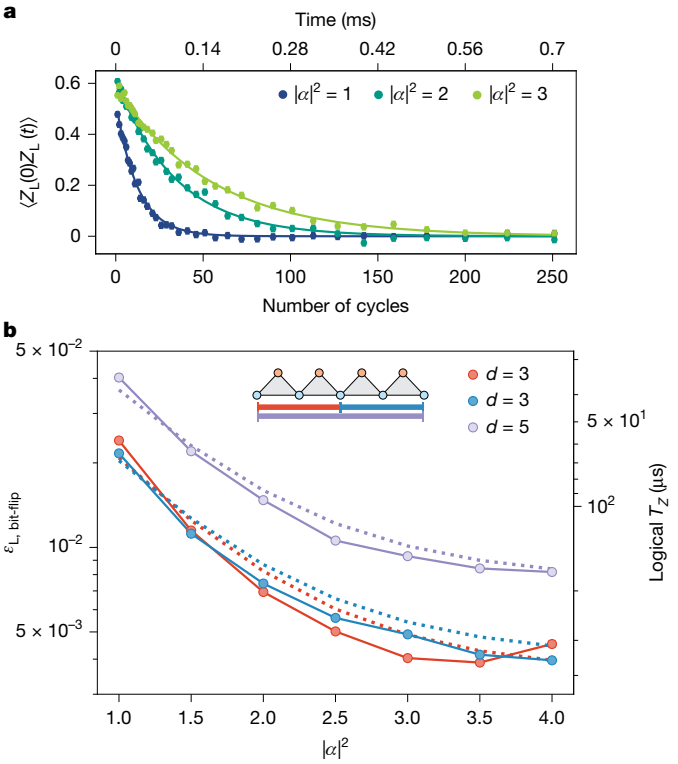

Fig. 4 | Characterizing logical bit-flip error rates. a, Fitted decay curve of the logical Z operator for several storage mean photon numbers for the distance-5 code. Error bars capture sampling error. **b**, Logical bit-flip probability per cycle ($\epsilon_{L,\text{bit-flip}}$) and logical Z lifetime (T_Z) as a function of $|\alpha|^2$ for the two distance-3 repetition-code sections and the distance-5 section. Solid lines correspond to data and dotted lines correspond to a phenomenological model. Error bars (standard error), capturing sampling variance and fit uncertainty, are smaller than the markers.

because of detailed design and calibration strategies (Supplementary Information), we can maintain long logical bit-flip times during the syndrome extraction of the repetition code in our device.

We characterize the logical bit-flip probabilities by measuring the decay time, T_Z, of the logical Z operator $\hat{Z}_L = \hat{Z}_1\hat{Z}_2\cdots\hat{Z}_d$. To do so, we first initialize the data cat qubits in a tensor-product of coherent states (for example, $|\alpha\rangle^{\otimes d}$), apply a variable number of syndrome extraction cycles and finally perform single-shot cat qubit Z-basis measurements (Supplementary Information) to measure $\hat{Z}_L$. The logical Z lifetime, T_Z, is then obtained by fitting the decay curve of $\langle \hat{Z}_L(t=0)\hat{Z}_L(t=t)\rangle$ to an exponential (Fig. 4a). From T_Z, we compute the logical bit-flip error per cycle as $\epsilon_{L,\text{bit-flip}} = T_{\text{cycle}}/(2T_Z)$.

Figure 4b shows $\epsilon_{L,\text{bit-flip}}$ as a function of $|\alpha|^2$ for the distance-5 (purple) and two distance-3 (red and blue) sections. At a low $|\alpha|^2$ of 1, $\epsilon_{L,\text{bit-flip}}$ is about 2% for the two distance-3 sections and around 4% for the distance-5 section. As $|\alpha|^2$ increases to 4, $\epsilon_{L,\text{bit-flip}}$ drops to below 0.5% for the two distance-3 sections and below 1% for the distance-5 section, because of the increased level of bit-flip protection from the cat qubits. As $\epsilon_{L,\text{bit-flip}}$ combines the bit-flip error contributions from all the cat qubits and CX gates, the distance-5 section, with more bit-flip error locations, has higher $\epsilon_{L,\text{bit-flip}}$. Nevertheless, the large noise bias maintained throughout the error correction cycle enables us to achieve sub-1% logical bit-flip probability even for the distance-5 section, which involves 5 cat qubits and 8 CX gates.

Figure 4b shows a phenomenological model of the logical bit-flip errors based on independent CX and cat qubit characterization experiments. The agreement between the model and measurements indicates that there is no marked degradation in cat qubit bit-flip rates when integrated together into the repetition code.

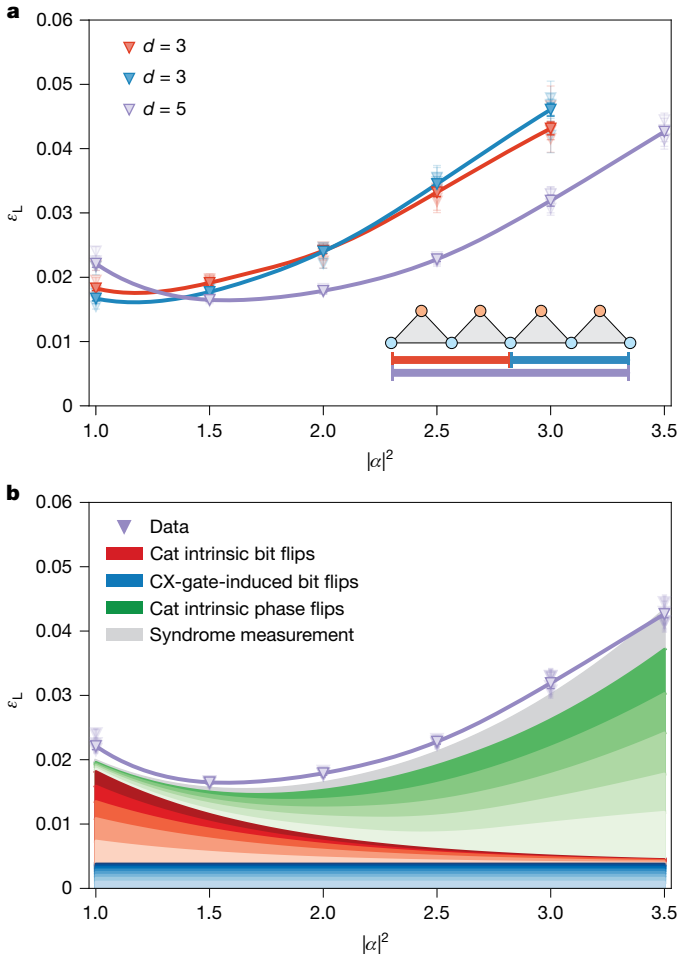

Fig. 5 | Logical qubit memory performance. a, Overall logical error per cycle of the repetition cat code, $\epsilon_L = (\epsilon_{L,\text{bit-flip}} + \epsilon_{L,\text{phase-flip}})/2$, versus cat qubit mean photon number $|\alpha|^2$. As in Fig. 3f, the faded points correspond to fits to groupings of the data by the number of even cat states in the initial state. The lines are guides to the eye, computed by interpolating both the logical phase-flip and bit-flip probabilities, $\epsilon_{L,\text{phase-flip}}$ and $\epsilon_{L,\text{bit-flip}}$, respectively. **b**, Error budget for the distance-5 repetition code using erasure information. Different shades of colour correspond to the different per cat (or per CX gate) contribution to the error budget. Error bars (standard error) incorporate sampling and fit errors.

Overall memory lifetime and error budget

Combining the logical bit-flip and phase-flip probabilities, we show in Fig. 5a the overall logical error per cycle[25,26], $\epsilon_L = (\epsilon_{L,\text{phase-flip}} + \epsilon_{L,\text{bit-flip}})/2$ ($(P_X + 2P_Y + P_Z)/2$ under Pauli noise), for the repetition cat codes. As $\epsilon_{L,\text{phase-flip}}$ increases with $|\alpha|^2$, while $\epsilon_{L,\text{bit-flip}}$ decreases with $|\alpha|^2$, ϵ_L is minimized at a certain value of $|\alpha|^2$. The shorter distance-3 codes favour operation at smaller $|\alpha|^2$ because of their weaker protection against phase-flip errors. By contrast, the distance-5 code has better protection from phase-flip errors and can thus operate at higher $|\alpha|^2$, benefiting from the larger noise bias of the cat qubits there. The best-measured performance for the distance-5 section is $\epsilon_L = 1.65 \pm 0.03\%$ at $|\alpha|^2 = 1.5$. This is comparable to the best observed performance for the distance-3 sections which are $\epsilon_L = 1.83 \pm 0.03\%$ and $\epsilon_L = 1.67 \pm 0.04\%$ at $|\alpha|^2 = 1$ (average $\epsilon_L = 1.75 \pm 0.02\%$).

We emphasize that a repetition code of biased noise qubits does not possess a proper asymptotic threshold because physical bit-flip errors are uncorrectable and place a lower bound on the achievable logical error[12]. Still, at large enough noise bias, the logical error can be reduced by increasing code distance before encountering this limit. By contrast, without bias, overall logical error would inevitably increase with code distance. The large noise bias in our device is apparent from the observations that we achieve comparable logical error as we increase distance and that the distance-5 section outperforms the distance-3 sections for $|\alpha|^2 \geq 1.5$.

In Fig. 5b, we use models of the logical bit-flip and phase-flip errors to construct an error budget for the distance-5 repetition cat code (Supplementary Information). The error budget is broken into four error mechanisms: cat intrinsic bit-flip errors (red), CX-gate-induced bit-flip errors (blue), cat intrinsic phase-flip errors capturing idling and CX gate phase flips (green) and syndrome measurement errors (grey). The bit-flip mechanisms (first two) dominate at small $|\alpha|^2$, and the phase-flip (latter two) mechanisms dominate at large $|\alpha|^2$. The minimum logical error rate is achieved at $|\alpha|^2 \simeq 1.5$, for which the bit-flip and phase-flip contributions are comparable. Notably, at this optimal value of $|\alpha|^2 \simeq 1.5$, the cat intrinsic errors are the dominant contributors as opposed to additional CX-gate-induced errors.

Conclusion and outlook

In this work, we have performed error correction using a concatenated bosonic code, in which bit-flip errors are suppressed with a bosonic cat code and residual phase-flip errors are corrected with a repetition code. This experiment serves as a promising first step in taking advantage of bosonic qubits, and also noise bias, to improve the hardware efficiency of QEC. Furthermore, having constructed our logical qubit memory using planar microfabrication processes, this work highlights the potential scalability of the concatenated bosonic qubit architecture.

The logical error in our current device is dominated by intrinsic cat bit-flip and phase-flip errors (Fig. 5b), but there are several strategies to reduce these errors in the near term. We project that by optimizing cycle time and using the further optimized cat qubit circuit in ref. 24, an overall logical error per cycle approaching 0.5% (limited by transmon errors) is achievable with a distance-5 code even without improvements in the component coherence times.

The use of ancillary transmons for syndrome measurements is important to our experiment, enabling noise-biased CX gates without undesired control errors, but comes along with ancilla-induced bit-flip errors. The logical performance at present is not limited by these errors, and improved ancilla lifetimes of 1 ms would ideally lower their probability to about 10^{-6} per CX (Supplementary Information). However, in the long term, it will be necessary to eventually correct ancilla-induced bit flips, which can be accomplished by concatenating cat qubits into surface codes tailored to noise-biased qubits[14,15]. We analyse this approach in ref. 60 and find that marked hardware-efficiency improvements are possible relative to the case without biased noise.

An alternative approach to overcome the transmon-induced limitations is to use cat qubits as the ancillas. This was proposed in ref. 10, but existing proposals for cat–cat CX gates are hampered by large control errors[10,12,15]. Searching for ways to implement syndrome measurements with a large noise bias but without undesired control errors[61–63] thus represents an important direction for future research. If the performance of gates were limited only by the intrinsic bit-flip and phase-flip rates of the cats, sizable reductions in logical-memory overhead would be possible with realistic device parameters. For example, with the cat qubit bit-flip times, we show in ref. 24 and improved storage lifetimes of about 300 μs (ref. 64), we project (Supplementary Information) that $\epsilon_L \sim 10^{-5}$ could be achieved with a $d = 11$ repetition cat code. Furthermore, with ≥100 s bit-flip times[34], and ms-scale storage T_1 (ref. 65), algorithmically-relevant $\epsilon_L \sim 10^{-8}$ could be achieved with similar overhead. Although these examples assuming coherence-limited gates are idealized hypotheticals, they nevertheless highlight the potential of cat qubits to enable hardware-efficient logical qubits.

Online content

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Data availability

Data for the logical qubit memory experiment can be found at Zenodo (https://doi.org/10.5281/zenodo.14257632; ref. 66).

66. Putterman, H. Data from "Hardware-efficient quantum error correction using concatenated bosonic qubits". *Zenodo* https://doi.org/10.5281/zenodo.14257632 (2024).

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Additional information

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