

TLE985x Evaluation Board User Manual

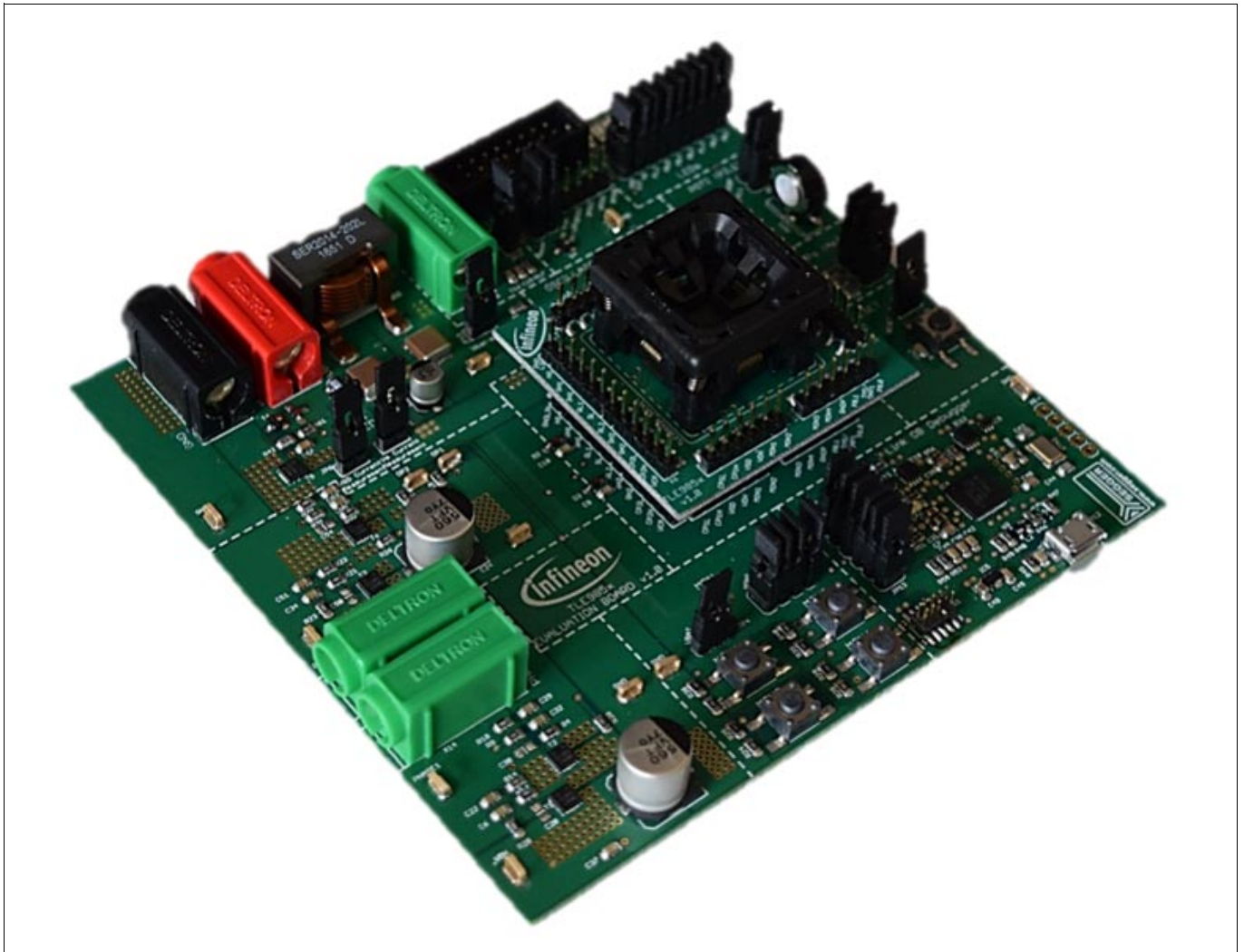


Figure 1 TLE985x Evaluation Board

About this document

Scope and purpose

The TLE985x Evaluation Board is designed to evaluate hardware and software functionalities of the TLE985x device family. All pins of the chip are able to be contacted via pin headers. Further, the on-board MOSFET H-bridge can be used to evaluate DC motor applications.

This manual provides information about the board's interconnections, jumper settings, communication and debug interfaces. Additionally, an introduction to the software toolchain is given as well as detailed information about the board's design data.

Note: This evaluation board is not optimized for EMC behavior.

Intended audience

This document is for everyone who works with the TLE985x_EVB.

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Concept

1 Concept

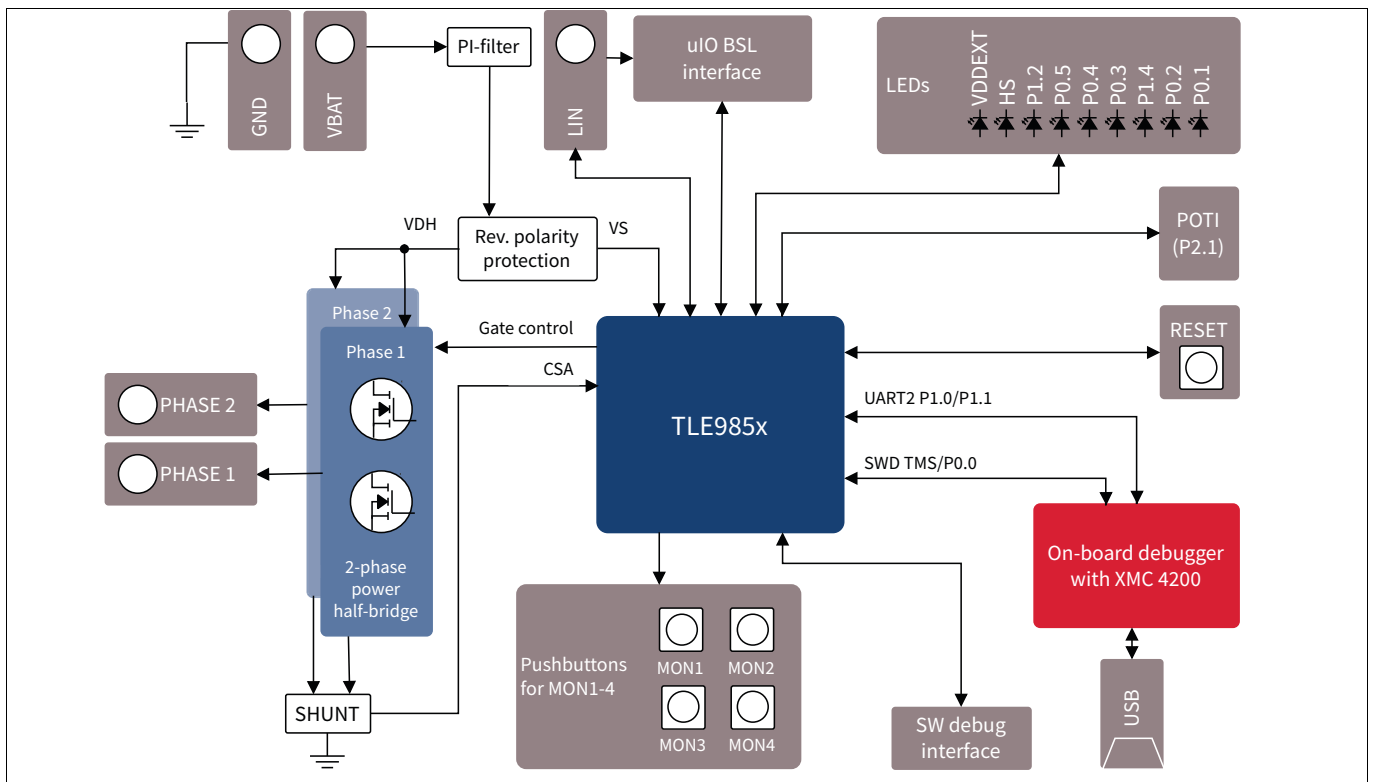


Figure 2 TLE985x Evaluation Board concept

This board is designed to provide a fast and easy start of evaluation for Infineon’s Embedded Power TLE985x device family. Initially, the evaluation board brings several interfaces and interconnections shown in **Figure 2**.

The TLE985x device is placed in the center of the PCB. A socket provides the possibility to test and evaluate all ICs out of the TLE985x device family. Every pin of the IC is connectable via rows of pin headers. The board is protected against reverse polarity of input voltage supply.

Two MOSFET half bridges are available to instantly drive a DC motor, which can be connected via banana jacks.

The evaluation board provides an on-board debugger. It is placed in the lower right of **Figure 2**. It provides a debug connection (SWD) and a virtual COM port for serial UART communication.

The high-voltage monitor pins can be triggered with dedicated pushbuttons.

For analog input values, a potentiometer is connected to pin P2.1.

The LIN connection can be configured to master or slave mode.

2 Interconnections

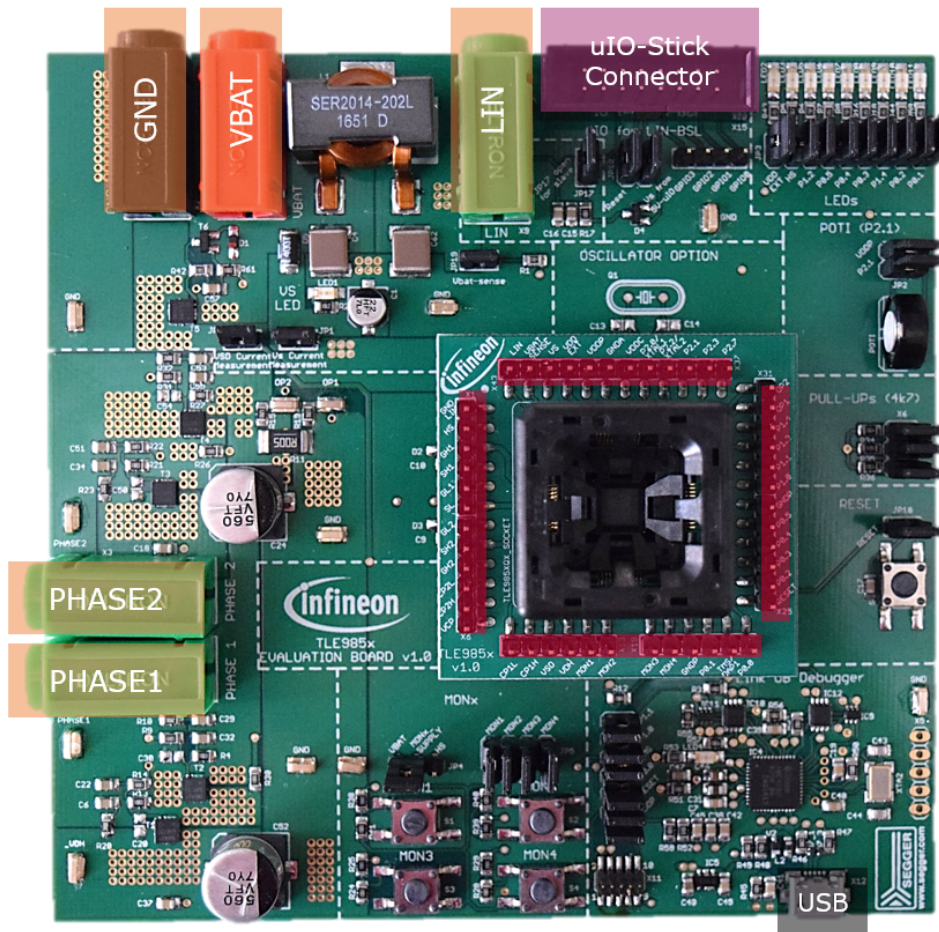


Figure 3 Interconnections

4mm laboratory connectors (orange)

Ground, supply voltage (operating voltage is documented in the datasheet) and LIN communication can be connected via banana jacks:

GND (black), VBAT (red), LIN (green)

Two MOSFET half bridges can also be accessed with laboratory equipment:

PHASE1 and PHASE2 (green)

uIO connector (purple)

The uIO Stick can be connected at the upper right corner of the evaluation board. It provides BSL programming via FastLIN. The connector provides a reverse-polarity protected connection between the evaluation board and the uIO Stick. (Signals: RESET, VS, LIN)

USB (black)

An on-board debugger is implemented on the TLE985x Evaluation Board. The USB connection provides a debug and serial interface to the PC.

Pin headers (red)

Each pin of the TLE985x is available for measurements and evaluation via pin headers.

3 Jumper Settings

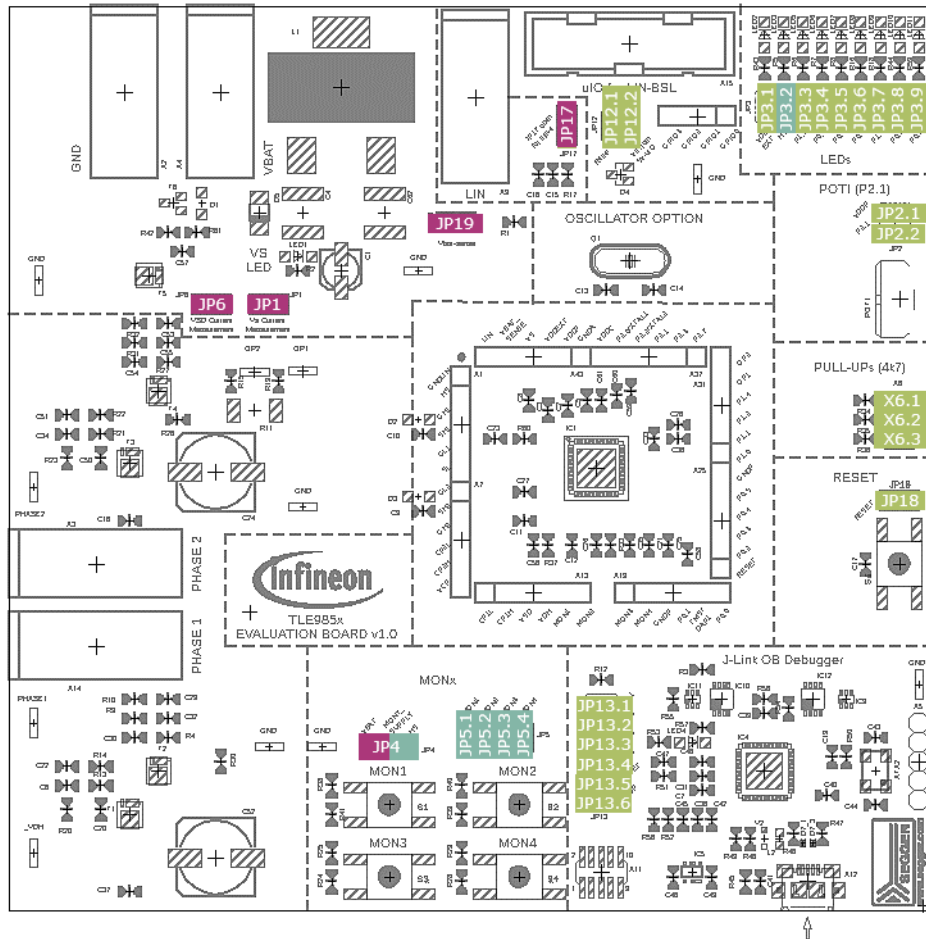


Figure 4 Jumper settings

Figure 4 shows the jumper positions on the Evaluation Board. The colors give an information about the voltage, which can appear at the jumper pins as follows:

- Green-marked jumpers are related to the 5-V domain (voltage range 0 V ... VDDP/VDDEXT).
- Blue-marked jumpers are related to high-voltage inputs or outputs of the TLE985x.
- Purple-marked jumpers are connected to the supply voltage of the evaluation board.

Table 1 shows which jumper is connected to which pins and peripherals of the TLE985x.

Table 1 Jumper list

Jumper number	Signal name	Description and board connection
JP1	VS	VS current measurement
JP2.1	VDDP	Potentiometer supply
JP2.2	P2.1	Potentiometer connected to P2.1
JP3.1	VDDEXT	LED2
JP3.2	HS	LED3
JP3.3	P1.2	LED5

Jumper Settings

Table 1 Jumper list

Jumper number	Signal name	Description and board connection
JP3.4	P0.5	LED6
JP3.5	P0.4	LED7
JP3.6	P0.3	LED8
JP3.7	P1.4	LED9
JP3.8	P0.2	LED10
JP3.9	P0.1	LED11
JP4	VBAT/HS	Supply selection for MONx switches
JP5.1	MON1	Pushbutton S1 (MON1)
JP5.2	MON2	Pushbutton S2 (MON2)
JP5.3	MON3	Pushbutton S3 (MON3)
JP5.4	MON4	Pushbutton S4 (MON4)
JP6	VSD	VSD current measurement
JP12.1	RESET	Reset connection from uIO Stick
JP12.2	VS	Supply connection from uIO Stick
JP13.1	P1.1	Disconnect UART/Debugger
JP13.2	P1.0	Disconnect UART/Debugger
JP13.3	TMS	Disconnect UART/Debugger
JP13.4	P0.0	Disconnect UART/Debugger
JP13.5	RESET	Disconnect UART/Debugger
JP13.6	VDDP	Disconnect UART/Debugger
JP17	LIN	LIN master/slave configuration
JP18	RESET	Pushbutton S6 (RESET)
JP19	VBAT	VBAT_SENSE
X6.1	VDDEXT	Pull-up for wire connection
X6.2	VDDEXT	Pull-up for wire connection
X6.3	VDDEXT	Pull-up for wire connection

4 Communication Interfaces

4.1 LIN and uIO for LIN BSL

The device-integrated LIN transceiver is connected to a banana jack and additionally to the uIO BSL interface. To integrate the device in a LIN network it is sufficient to use the single wire banana interface. The BSL interface is intended to program the device via LIN. For further information about the uIO interface see www.hitex.com/uio.

4.2 UART (virtual COM port via USB)

A virtual COM port provided by the Segger driver enables a PC-to-board communication via UART. The UART2 module of TLE985x uses the pins P1.0 (transmit) and P1.1 (receive). Those are connected to the XMC4200, which emulates Rx and Tx on PC side with the Segger firmware. Although they can be disconnected physically, bidirectional level shifters ensure that the XMC pins are hi-Z in the case the virtual COM port is not used. By connecting the evaluation board to the PC a virtual COM port gets emulated by the Segger driver automatically. The port will show up in the Microsoft® Windows® device manager.

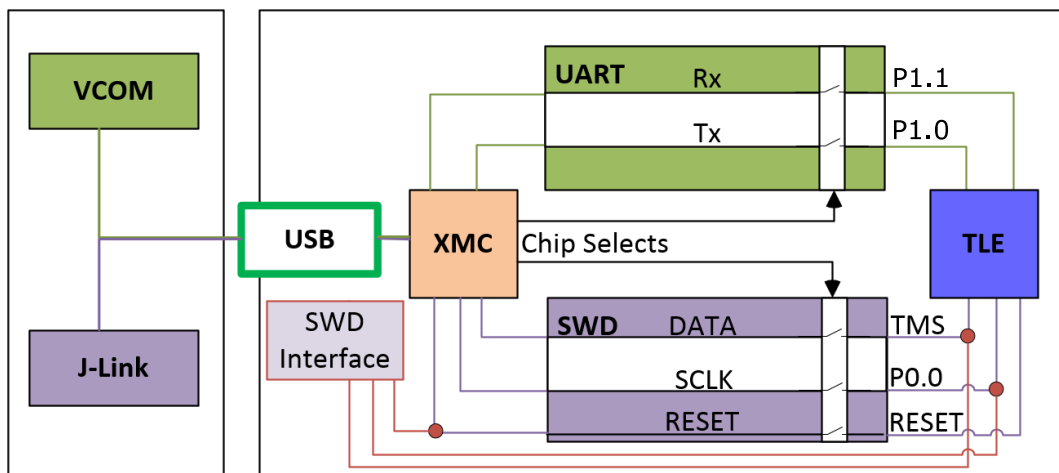


Figure 5 UART and Debugging

Note: Only one of the interfaces USB or SWD can be used at one time. While using the SWD interface the XMC is hold in reset. It therefore eliminates debugging or UART via USB while a debugger is connected with the SWD interface.

4.3 SWD debug interface (J-Link via USB)

For serial wire debug (SWD) the TLE985x uses the pins TMS (data) and P0.0 (clock). Level shifters between XMC4200 and TLE985x allow using P0.0, while it is not used for debugging.

The Segger J-Link module on board allows serial wire debugging via USB.

It is also possible to use an alternative debugger instead of the on-board Segger debugger, e.g. Keil ULINK2. For this the signals are routed through the 10 pin header SWD interface between the XMC4200 and the TLE985x. The pin configuration makes sure that the XMC is hold in reset while another debugger is physically connected at X15. The virtual COM port will be disabled, while the external ISP is connected.

5 Software Toolchain

5.1 Keil µVision 5

The recommended Integrated Software Development Environment is Keil® µVision5®. Infineon’s Embedded Power family is supported. For more information about the Toolchain go to: www.keil.com

5.2 Infineon Config Wizard

In addition to the IDE, Infineon® provides the ConfigWizard. The tool is designed for code configuration, in combination with the IDE. Infineons Config Wizard can be downloaded via: www.infineon.com/embeddedpower

5.3 TLE985x Installation

All embedded Power products can be installed to Keil® µVision5® via “Pack Installer”. Browsing to the Infineon chapter in “All Devices” will lead to the “TLE98xx Series”. The “.pack” file comes with several code examples, to provide an easy start up and speed up software development.

5.4 Debug Connection Setup

For a proper Flash and Debug Connection, Install V5.10 (or newer) from: www.segger.com/jlink-software.html

Keil® µVision5® has to be configured in the IDE Menu “Options for Target”. After connecting the USB-cable and power up the Evalboard, go to the “Debug” register-card and choose “J-LINK / J-TRACE Cortex” and press “Settings”.

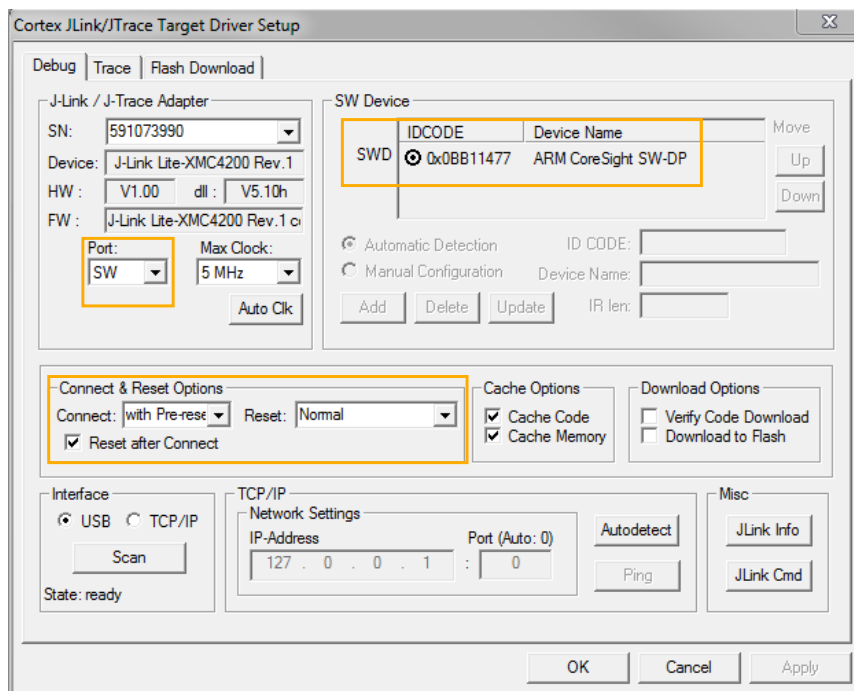


Figure 6 Debug and Flash Configuration

If the board has been connected successfully, the ARM IDCODE will be visible in the SW Device Window. If connection fails, “Connect & Reset Options” and “Port” window has to be checked.

6 PCB Design Data

This Chapter contains schematic and layout data.

6.1 Schematic

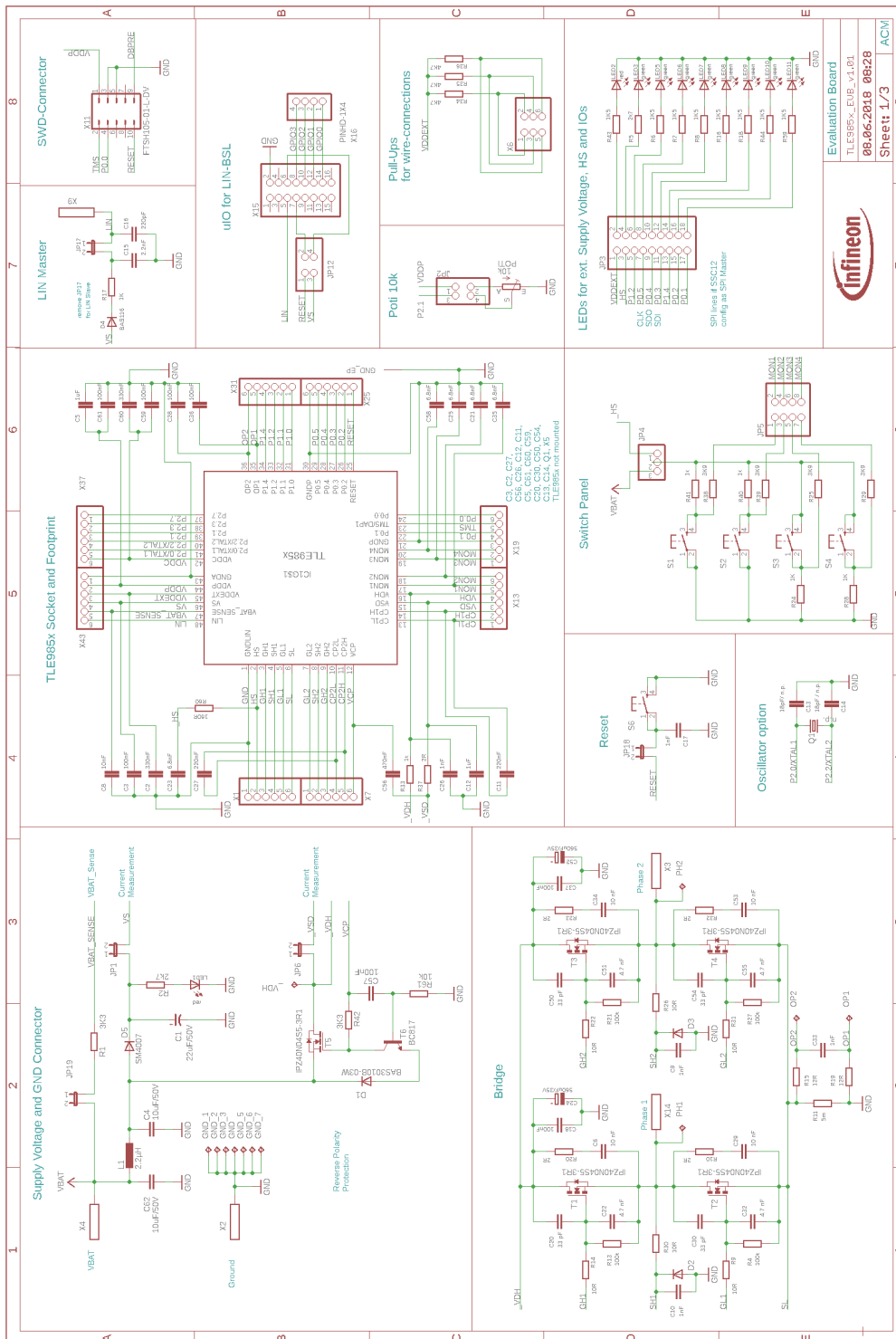


Figure 7 TLE985x Circuit and peripheral components

Note: This is a very simplified example of an application circuit and bill of material. The function must be verified in the application.

PCB Design Data

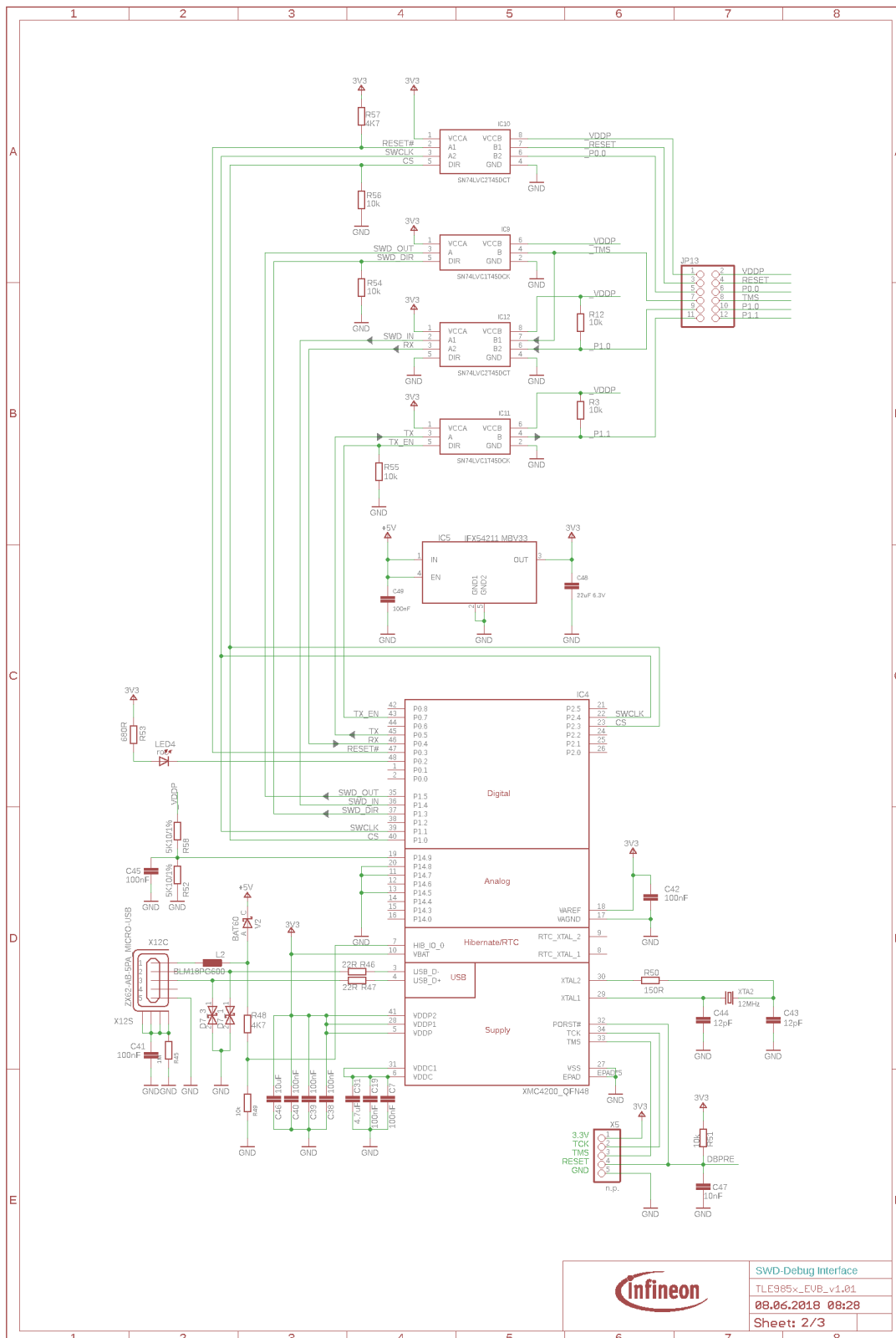


Figure 8 On-board debug circuit

Note: This is a very simplified example of an application circuit and bill of material. The function must be verified in the application.

PCB Design Data

6.2 Layout Data

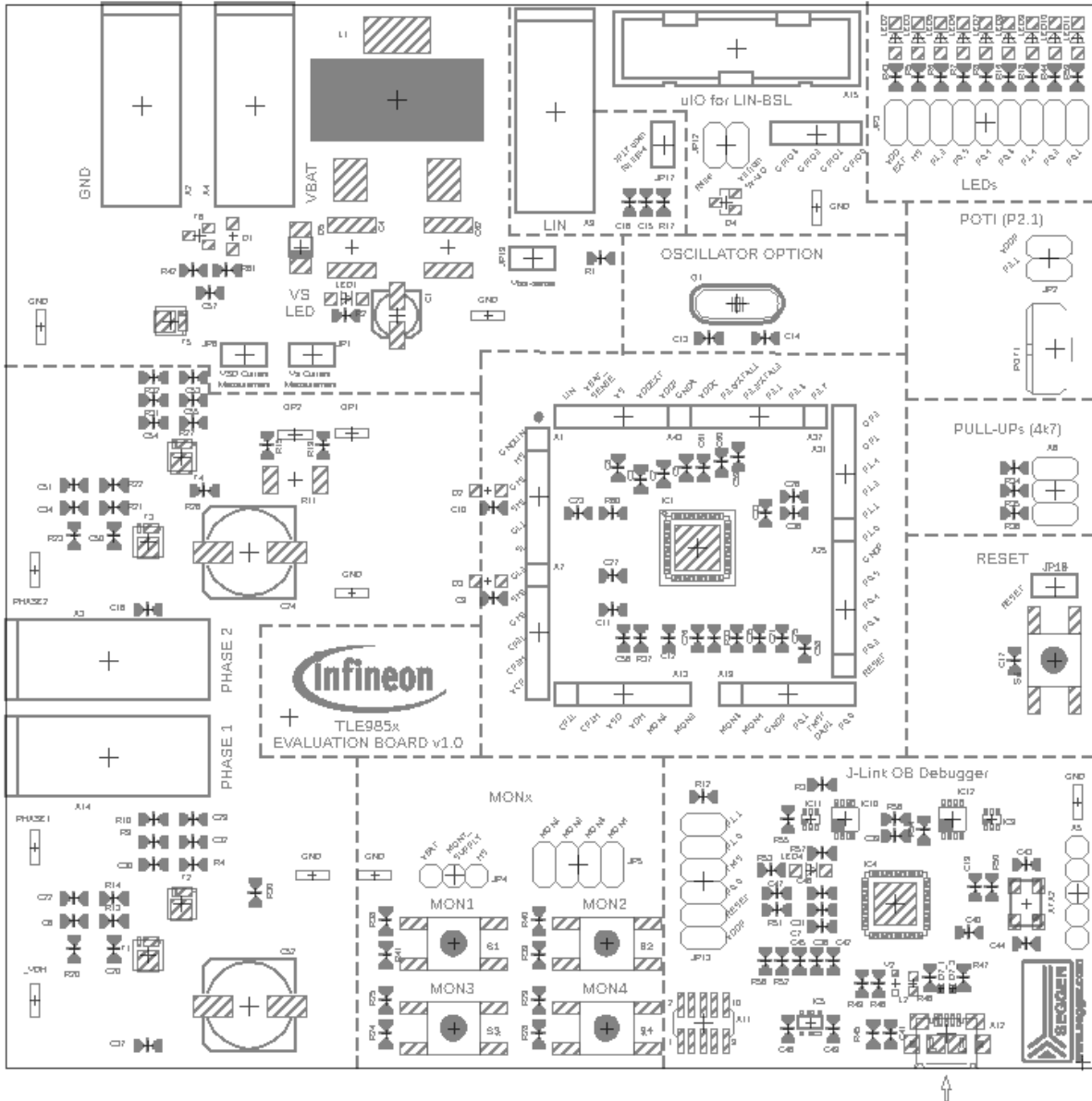


Figure 9 Parts placement

Note: This is a very simplified example of an application circuit and bill of material. The function must be verified in the application.

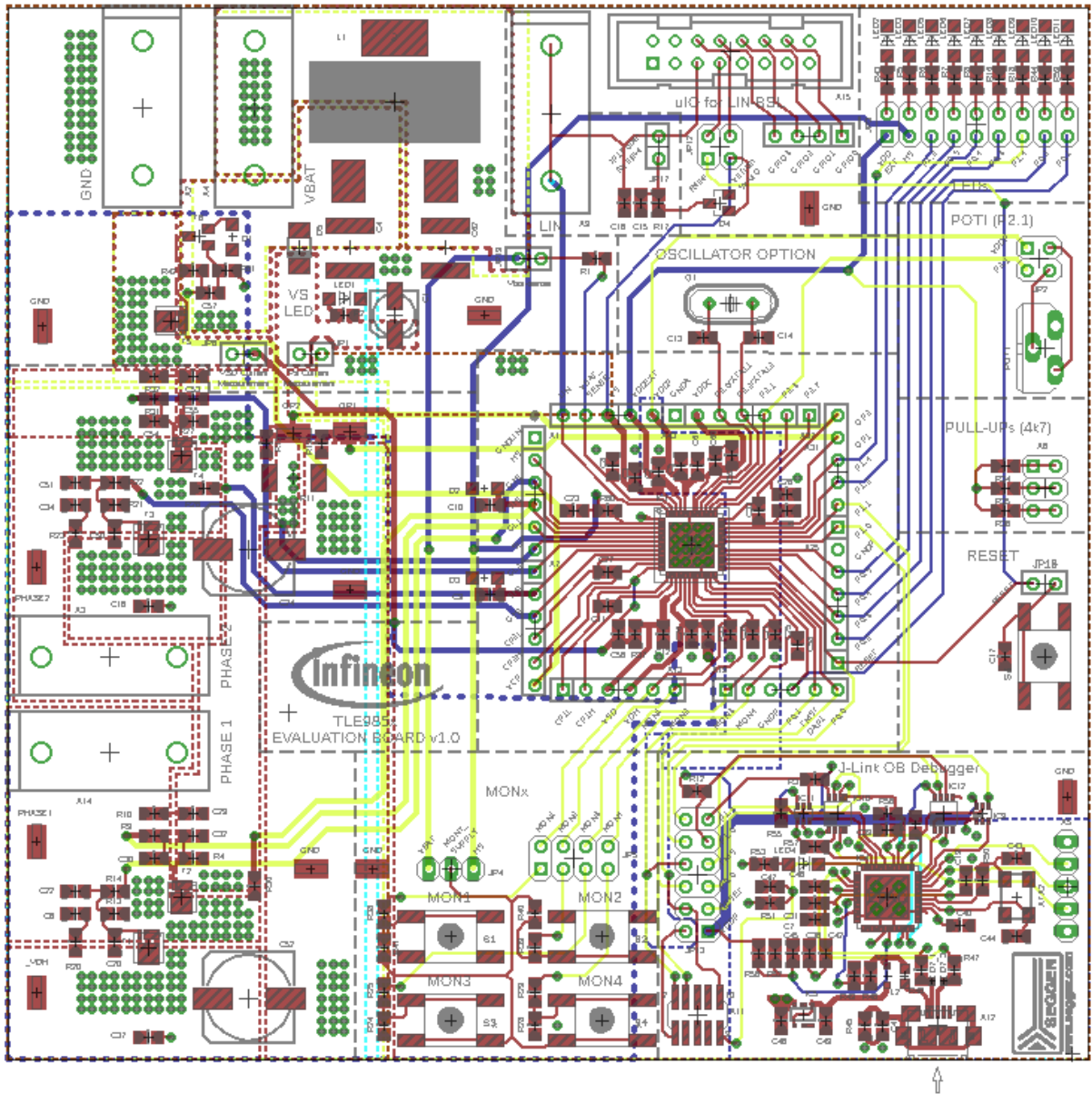


Figure 10 Full layout

Note: This is a very simplified example of an application circuit and bill of material. The function must be verified in the application.

PCB Design Data

6.3 Part List

Table 2 Evaluation board part list

Part Number	Value	Package
C1	22 μ F/50V	CAP-MASTER 153CLV-0505
C11, C27	220nF	0805
C13, C14	18pF	0805
C15	2.2nF	0805
C16	220pF	0805
C2, C60	330nF	0805
C20, C30, C50, C54	33pF	0805
C21, C23, C25, C35, C58	6.8nF	0805
C22, C32, C51, C55	4.7nF	0805
C24, C52	560 μ F/35V	153CLV-1014
C3, C7, C18, C19, C28, C36, C37, C38, C39, C40, C41, C42, C45, C49, C57, C59, C61	100nF	0805
C31	4.7 μ F	0805
C4, C62	10 μ F/50V	C2220K
C43, C44	12pF	0805
C46	10 μ F	0805
C48	22 μ F/6.3V	0805
C5, C12	1 μ F	0805
C56	470nF	0805
C6, C8, C29, C34, C47, C53	10nF	0805
C9, C10, C17, C26, C33	1nF	0805
D1, D2, D3	BAS3010B-03W	SOD323-W
D4	BAS116	SOT23
D5	SM4007	DO-214AC
D7_1, D7_3	ESD8V0L1B-02EL	TSLP-2
GND, GND_1, GND_2, GND_3, GND_5, GND_6, GND_7, OP1, OP2, PH1, PH2, VDH	Testpoint	TP_SMD
IC1	TLE985xQX	VQFN48
IC10, IC12	SN74LVC2T45DCT	R-PDSO-G8
IC4	XMC4200	QFN48
IC5	IFX54211 MBV33	SCT595
IC9, IC11	SN74LVC1T45DCK	R-PDSO-G6
JP1, JP6, JP17, JP18, JP19	Pin header 1x2	1X02
JP13	Pin header 2x6	2X06
JP2, JP12	Pin header 2x2	2X02

PCB Design Data

Table 2 Evaluation board part list

Part Number	Value	Package
JP3	Pin header 2x9	2X09
JP4	Pin header 1x3	1X03
JP5	Pin header 2x4	2X04
L1	2.2μH	SER2014
L2	BLM18PG600	L1608
LED1, LED2, LED4	LED red	1206
LED3, LED5, LED6, LED7, LED8, LED9, LED10, LED11	LED green	1206
POT1	10K	PT-10S
Q1		HC49/S
R1, R42	3K3	0805
R10, R20, R23, R32, R37	2R	0805
R11	5m	2512
R15, R19	12R	0805
R17, R24, R28, R33, R40, R41	1K	0805
R2, R5	2K7	0805
R25, R29, R38, R39	3K9	0805
R3, R12, R49, R51, R54, R55, R56, R61	10K	0805
R34, R35, R36, R48, R57	4K7	0805
R4, R13, R21, R27	100K	0805
R45	1M	0805
R46, R47	22R	0805
R50	150R	0805
R52, R58	5K1	0805
R53	680R	0805
R6, R7, R8, R16, R18, R43, R44, R59	1K5	0805
R60	160R	0805
R9, R14, R22, R26, R30, R31	10R	0805
S1, S2, S3, S4, S6	Button	SK_SMD
T1, T2, T3, T4, T5	IPZ40N04S5-3R1	PG-TSDSON-8
T6	BC817	SOT23-BEC
V2	BAT60	SOD323-R
X1, X7, X13, X19, X25, X31, X37, X43	Pin header 1x6	1X06
X11	FTSH105-01-L-DV	FTSH105_SMD
X12	ZX62-AB-5PA	MICRO-USB
X15	Pin header 2x8	PAK100/2500-16
X16	Pin header 1x4	1X04
X2	black	4mm Banana

PCB Design Data

Table 2 Evaluation board part list

Part Number	Value	Package
X3, X9, X14	green	4mm Banana
X4	red	4mm Banana
X5	Pin header 1x5	1X05
X6	Pin header 2x3	2X03
XTA2	12MHz	HC5032

References

References

- [1] www.infineon.com/embeddedpower

Revision History

Revision History

Revision History

Page or Item	Subjects (major changes since previous revision)
Rev. 1.0	Initial version

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