

TLE9845QX Evalboard Rev 1.4 User Manual



Figure 1 TLE9845QX Evalboard with PN-MOSFET single phase

About this document

Scope and purpose

The TLE9845QX Evalboard Rev 1.4 is designed to evaluate hardware and software functionalities of the TLE9845QX.

In the circuit p- and n-channel MOSFETs are placed in halfbridge connection to drive unidirectional DC motors. All Pins of the chip are able to be contacted via Pinhead connector.

This Manual provides additional information about the Boards Layout, Jumper settings, interfaces and Debug options. It introduces the Evaluation Platform as well as how to use example code and download it to the TLE9845QX.

Note: This Evaluationboard is not optimized for EMC behavior.

Intended audience

This Document is for everyone who works with the TLE9845QX Evaluation Board Rev 1.4.

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Concept

1 Concept

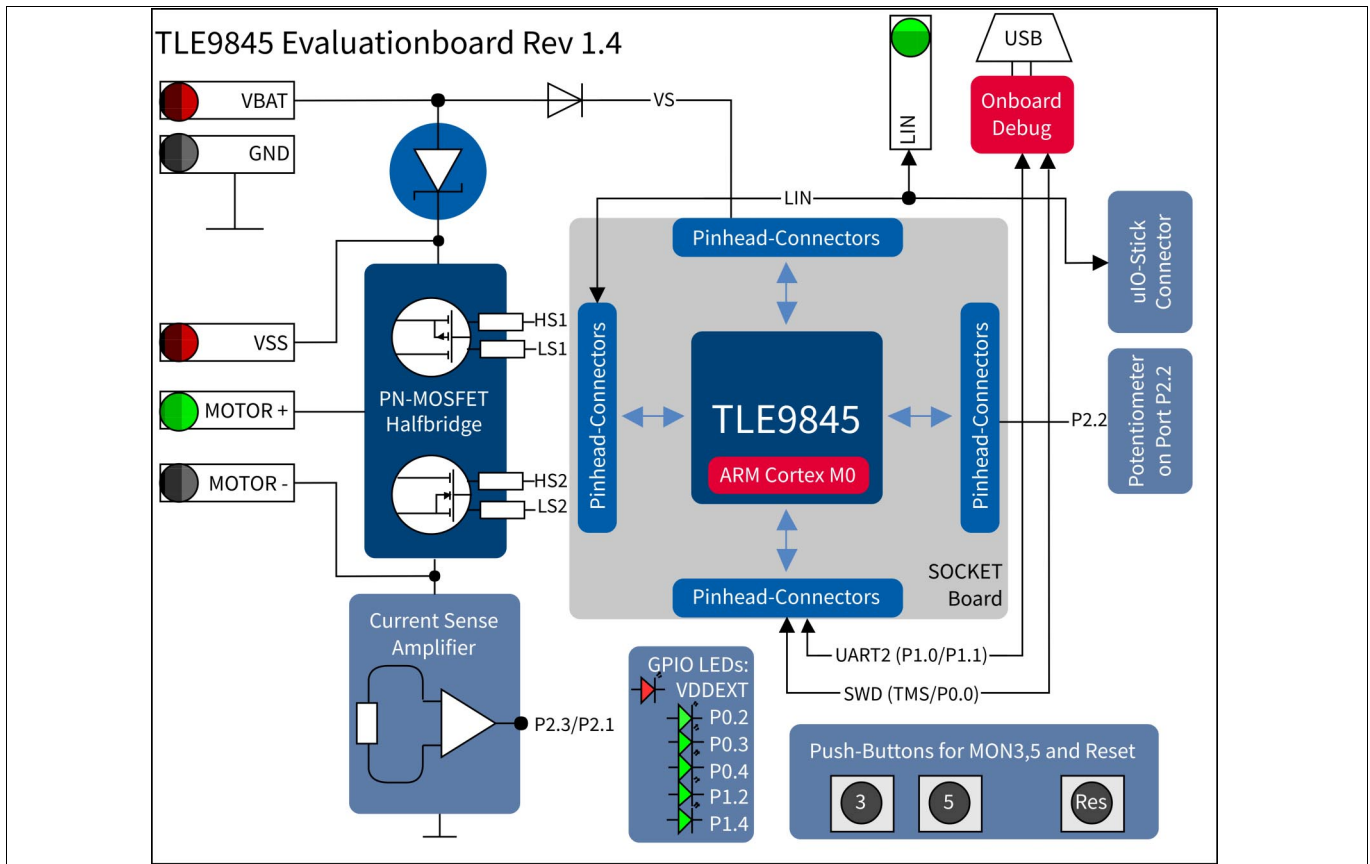


Figure 1 Evalboard Concept

This board is designed to provide a fast and easy start of evaluation, for Infineons embedded Power IC TLE9845QX. Initially, the evaluation board brings several interfaces and interconnections shown in Figure 1.

The TLE9845QX device is placed in the center of the PCB. A socket provides the possibility to test and evaluate all ICs out of the TLE984x device family. Every pin of the IC is connectable via rows of pinheader. The board is protected against reverse polarity of input voltage supply.

A PN-channel MOSFET halfbridge is connected to the integrated highside and lowside switches of the TLE9845QX Device. It can be used to evaluate several DC motor applications.

In addition to the halfbridge, a current sense resistor is placed with an external operational amplifier. It can be connected to the ADC1 inputs P2.3 or P2.1

The evaluationboard provides an on board debugger. It is placed in the upper right of Figure 1. It provides a SWD-Debug connection and a virtual COM port for serial UART communication.

Motor connections are connectable via 4mm standard laboratory plugs.

The High-Voltage-Monitor pins (MON3 and MON5) can be triggered with dedicated pushbuttons.

For analog input values a potentiometer is connected to PIN P2.2.

The LIN connection is able to be configured to master and slave mode.

Interconnections

2 Interconnections

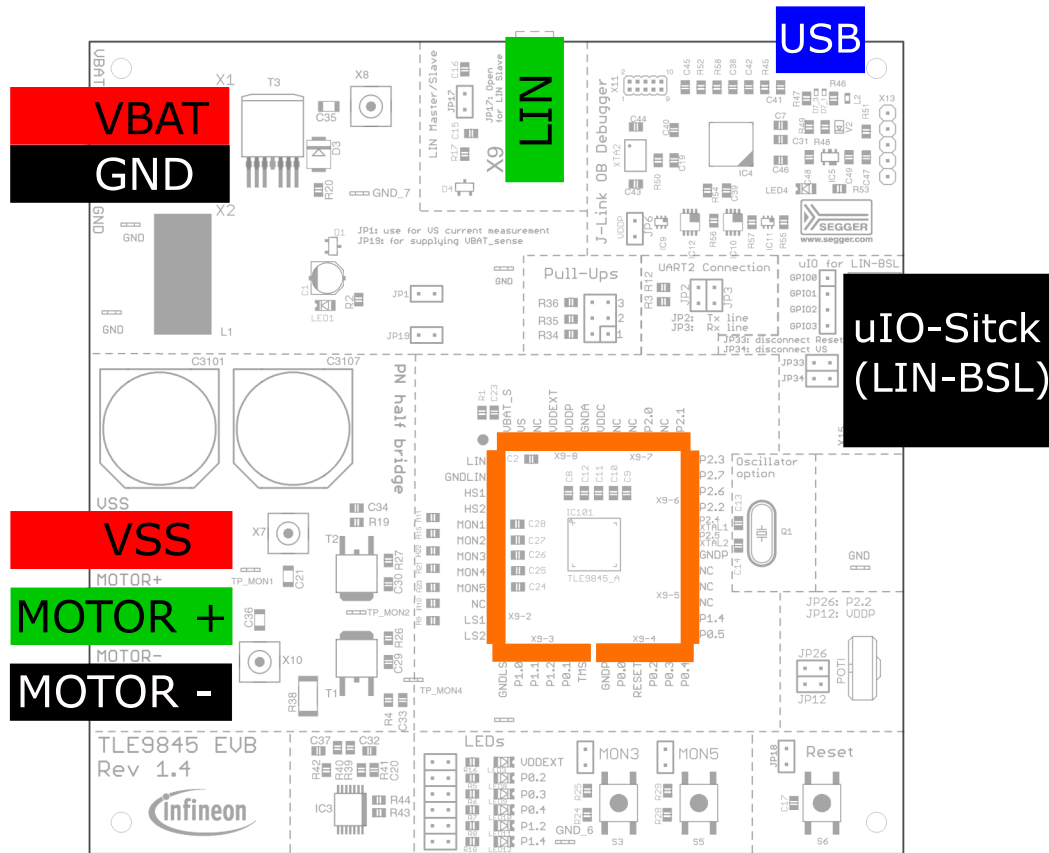


Figure 2 Interconnections

4mm Laboratory Connectors

Ground, voltagesupply (operating Voltage is documented in the datasheet) and LIN communication can be connected via banana jacks: GND (black), VBAT (red), LIN (green)

Motor contacts can also be accessed with laboratory equipment: VSS(red), MOTOR+(green), MOTOR-(black).

uIO-Connector (black)

The uIO-Stick can be connected at the upper right corner of the Evaluationboard. It provides BSL-Programming via LIN. The connector provides a polarity protected connection between the Evaluationboard and uIO-Stick. (Signals: RESET, VS, LIN)

USB (blue)

An Onboard-Debugger is implemented on the TLE9845QX_Evalboard. The USB-Connection provides a Debug- and Serial-interface to the PC. More information in [Chapter 5.4](#).

Pinhead Rows (orange)

Every Pin of the TLE9845 is available for measurements and evaluation, via Pinhead rows.

Jumper Settings

3 Jumper Settings

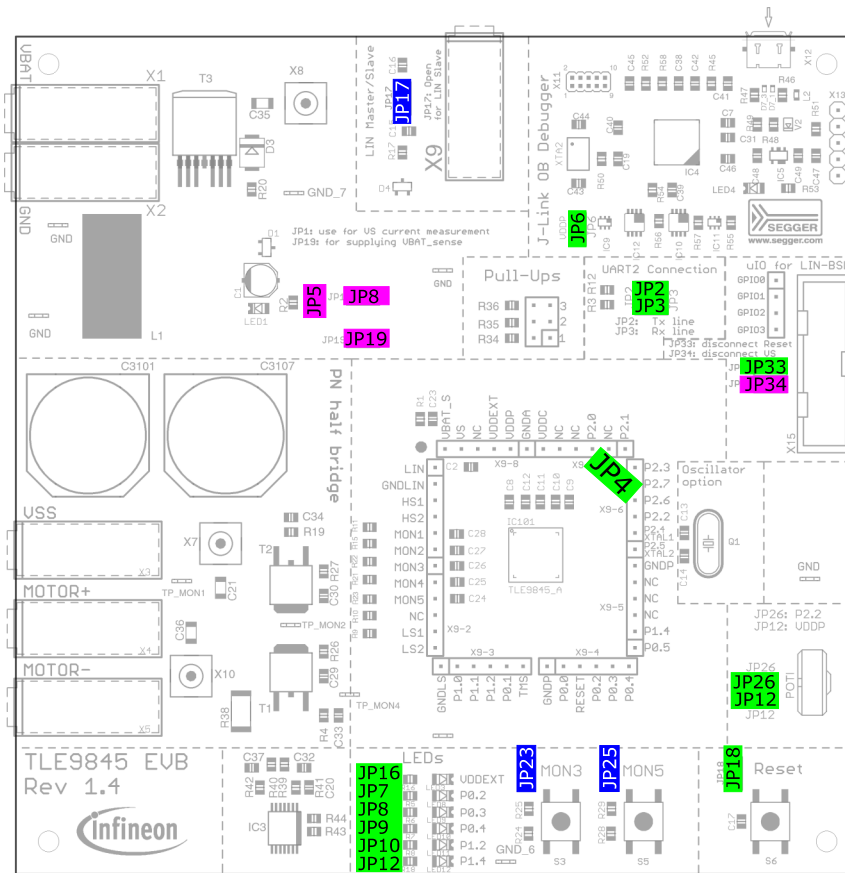


Figure 3 Jumper Settings

Figure 3 shows the jumper positions on the Evaluation Board. The color of marking gives an information about the voltage, which can appear at the Jumperpins.

Green marked jumper are related to the 5V domain (voltage range 0V...VDDP/VDDEXT).

Blue marked jumper are related to high voltage Inputs or Outputs of the TLE984x.

Purple jumper are connected to the supply voltage of the board.

Table 1 shows which Jumper is connected to the PINs of the TLE9845QX and the peripheral.

Table 1 Jumper List

Jumper Number	Signal Name	Description and Board connection
JP1	VS	VS current sense option
JP2	P1.0	UART2 TX connection
JP3	P1.1	UART2 RX connection
JP4	P2.1/P2.3	ADC1 PORT selection for OPAMP
JP5	VSS/VBAT	VS supply option (default: VS)
JP6	VDDP	Debug levelshifter supply
JP7	P0.2	LED8
JP8	P0.3	LED9
JP9	P0.4	LED10

Jumper Settings

Table 1 Jumper List

Jumper Number	Signal Name	Description and Board connection
JP10	P1.2	LED11
JP11	P1.4	LED12
JP12	VDDP	Potentiometer supply
JP16	VDDEXT	LED3
JP17	LIN	LIN Master/Slave option
JP18	RESET	Pushbutton S6
JP19	VBAT_S	VBAT-Sense option
JP23	MON3	Pushbutton S3
JP25	MON5	Pushbutton S5
JP26	P2.2	Potentiometer to ADC1 connection
JP33	RESET	uIO-Stick RESET Signal
JP34	VS	uIO-Stick VS option

4 Communication Interfaces

4.1 LIN and uIO for LIN BSL

The device integrated LIN transceiver is connected to a banana jack and additionally to the uIO BSL interface. To integrate the device in a LIN network it is sufficient to use the single wire banana interface. The BSL interface is intended to program the device via LIN. For further information about the uIO interface see www.hitex.com/uio.

4.2 UART (Virtual COM PORT via USB)

A virtual COM port provided by Segger driver enables a PC – board – communication via UART. The UART2 module of TLE9845QX uses the pins P1.0 (transmit) and P1.1 (receive). Those are connected to the XMC4200, which emulates Rx and Tx on PC side with Segger firmware. Though they can be disconnected physically, bidirectional level shifters ensure that the XMC pins are hi-Z in case the virtual COM port is not used. By connecting the evaluation board to the PC a virtual COM port gets emulated by the Segger driver automatically. The virtual COM port will show up in the Microsoft® Windows® device manager.

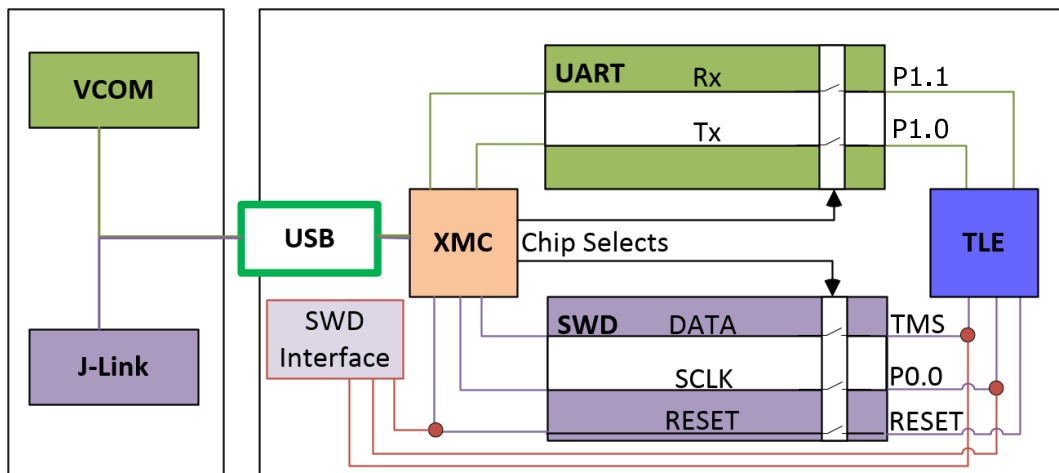


Figure 4 UART and Debugging

Note: Only one of the interfaces USB or SWD can be used at one time. While using the SWD interface the XMC is hold in reset. As long as a debugger is connected with the SWD interface it eliminates therefore debugging or UART via USB.

4.3 SWD-Debuginterface (J-Link via USB)

For serial wire debug the TLE984x uses the pins TMS (data) and P0.0 (clock). Level shifters between XMC4200 and TLE9845QX allow using P0.0, while it is not used for debugging.

The Segger J-Link module on board allows serial wire debugging via USB. Alternative debugging via SWD interface is possible to debug with another ISP than the onboard Segger e.g. U-Link2. Therefore the signals are routed through the 10 pin header SWD interface between the XMC4200 and the TLE984x. The pin configuration makes sure that the XMC is hold in reset while another debugger is physically connected to X11. The virtual COM port will be disabled, while the external ISP is connected.

5 Software Toolchain

5.1 Keil μ Vision 5

The recommended Integrated Software Development Environment is Keil[®] μ Vision5[®].

Infineons embedded Power family is supported. For more information about the Toolchain go to: www.keil.com

5.2 Infineon Config Wizard

In addition to the IDE, Infineon[®] provides the ConfigWizard. The tool is designed for code configuration, in combination with the IDE. Infineons Config Wizard can be downloaded via: www.infineon.com/embeddedpower

5.3 TLE9845QX Installation

All embedded Power products can be installed to Keil[®] μ Vision5[®] via “Pack Installer”. Browsing to the Infineon chapter in “All Devices” will lead to the “TLE98xx Series”. The “.pack” file comes with several code examples, to provide an easy start up and speed up software development.

5.4 Debug Connection Setup

For a proper Flash and Debug Connection, Install V5.10 (or newer) from:

www.segger.com/jlink-software.html

Keil[®] μ Vision5[®] has to be configured in the IDE Menu “Options for Target”. After connecting the USB-cable and power up the Evalboard, go to the “Debug” register-card and choose “J-LINK / J-TRACE Cortex” and press “Settings”.

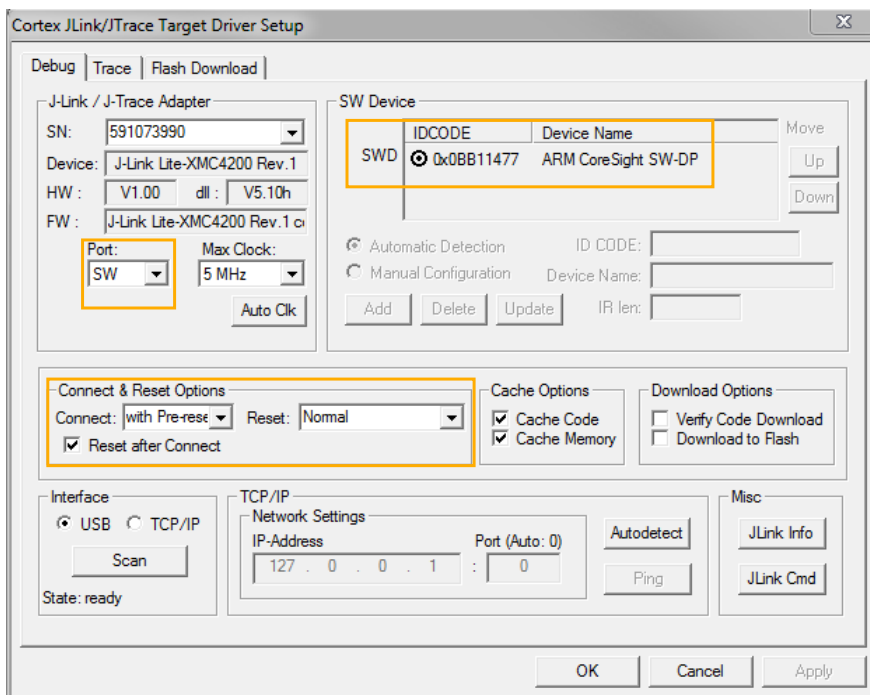


Figure 5 Debug and Flash Configuration

If the board has been connected successfully, the ARM IDCODE will be visible in the SW Device Window. If connection fails, “Connect & Reset Options” and “Port” window has to be checked.

6 Schematic and Layout

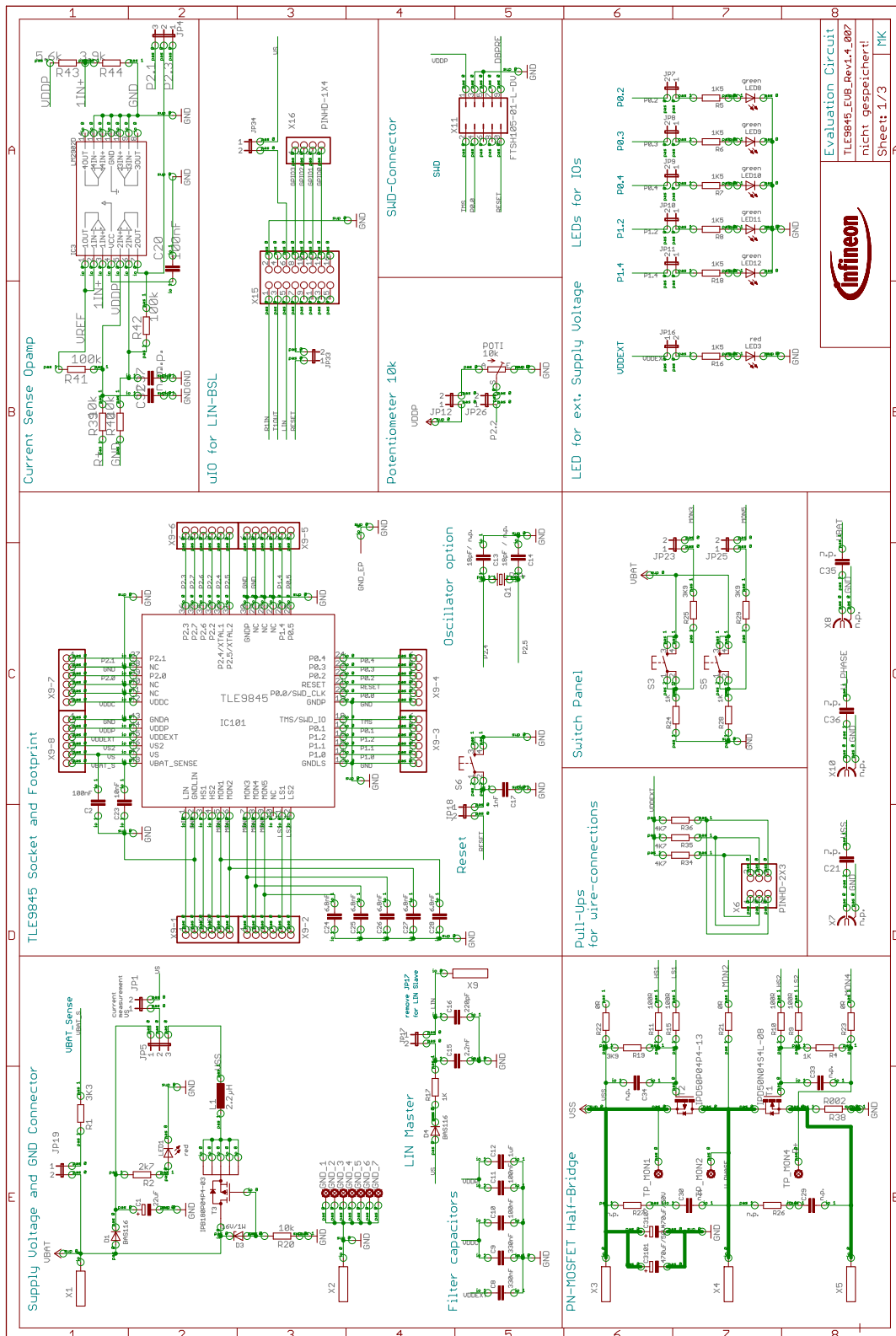


Figure 6 schematic sheet 1: TLE9845QX with peripherals and PN-MOSFET halfbridge

Note: This is a very simplified example of an application circuit and bill of material. The function must be verified in the application.

Schematic and Layout

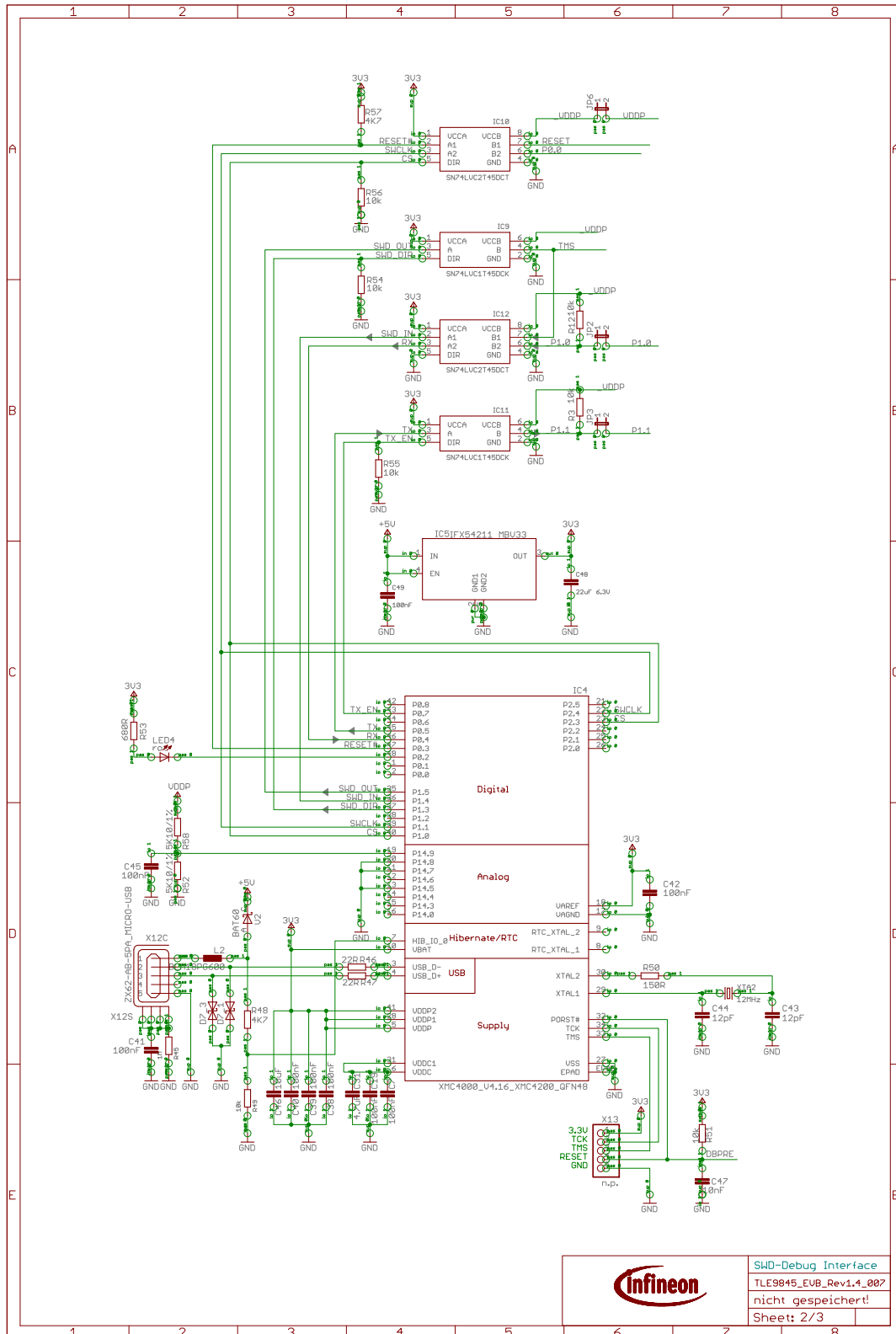


Figure 7 schematic sheet 2: Onboard Debug circuit

Note: This is a very simplified example of an application circuit and bill of material. The function must be verified in the application.

Schematic and Layout

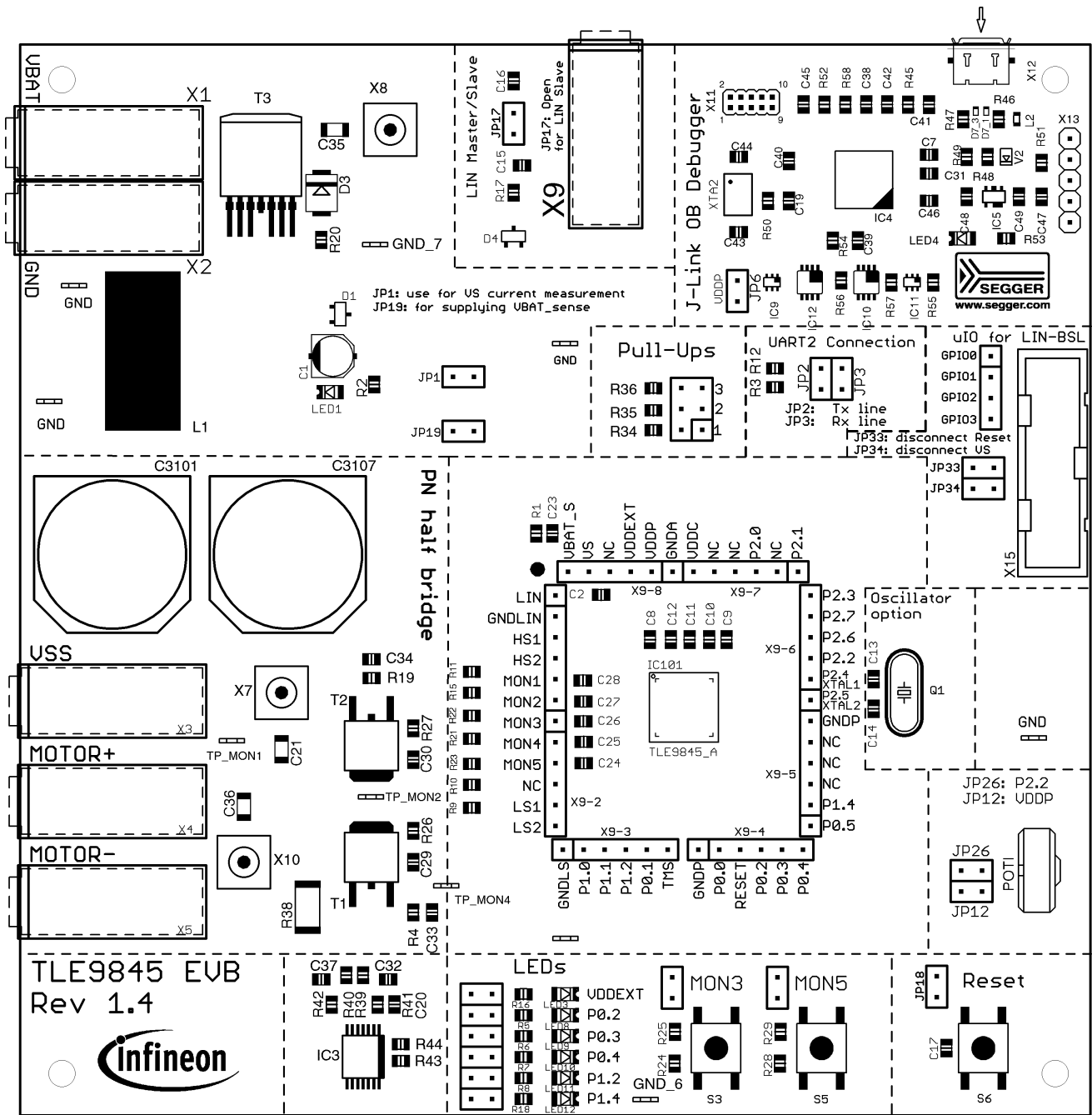


Figure 8 Parts placement

Note: This is a very simplified example of an application circuit and bill of material. The function must be verified in the application.

Schematic and Layout

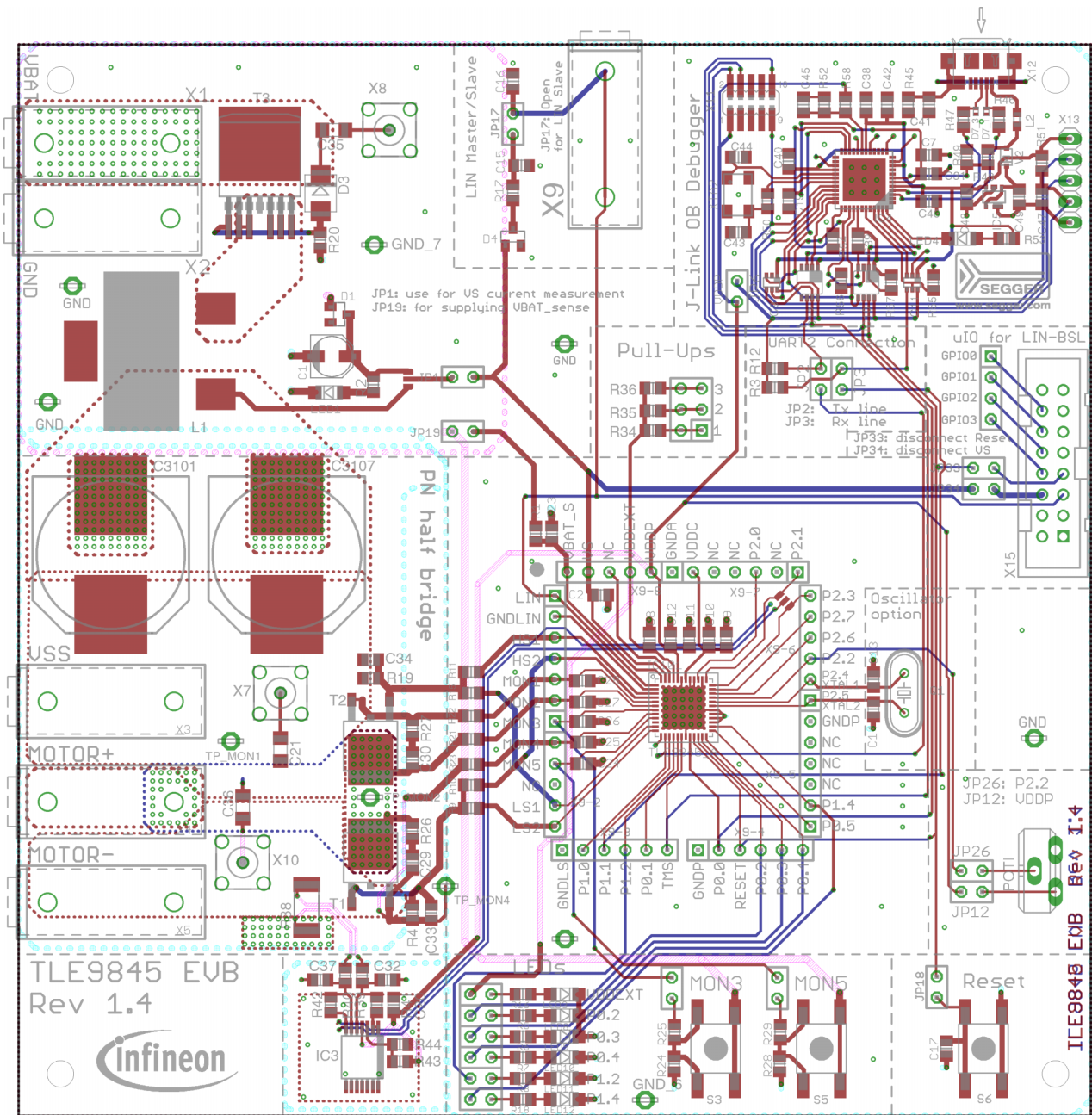


Figure 9 Layout ripup view (red:top layer, blue: bottom layer, cyan: GND layer, magenta: DC-link layer)

Note: This is a very simplified example of an application circuit and bill of material. The function must be verified in the application.

References

References

- [1] TLE984xQX Preliminary Data Sheet Rev. 0.26

Revision History

Revision History

Revision History

Page or Item	Subjects (major changes since previous revision)
Created, 2016-04-26	
Rev.1.0	Release

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