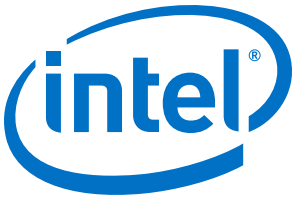

Intel® Stratix® 10 JTAG Boundary-Scan Testing User Guide

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Contents

1. Intel® Stratix® 10 Overview

Intel® Stratix® 10 devices support IEEE Std. 1149.1 BST and IEEE Std. 1149.6 BST. When you perform Boundary-Scan Test (BST), you can test pin connections without using physical test probes and capture functional data during normal operation. The boundary-scan cells (BSCs) in a device can force signals onto pins, or capture data from pin or core logic signals. Forced test data is serially shifted into the BSCs. Captured data is serially shifted out and externally compared to expected results.

Intel Stratix 10 devices are implemented using multiple die inside the package, connected together using EMIB (Embedded Multi-die Interconnect Bridge) technology. The multiple die implementation is transparent to BST. There is a single boundary-scan chain for the complete device that includes every die inside the package.

You can perform BST on Intel Stratix 10 devices before, after, and during configuration.

Related Information

Performing Intel Stratix 10 Boundary-Scan Testing on page 18

2. Intel Stratix 10 JTAG BST Architecture

2.1. JTAG Circuitry Functional Model

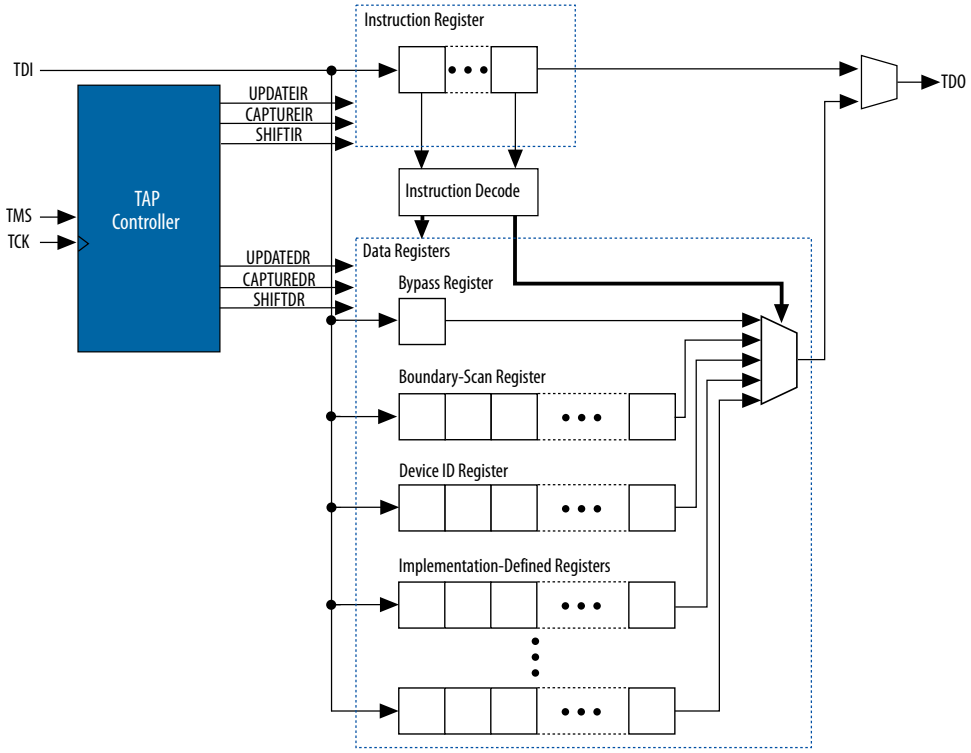
The JTAG BST circuitry requires the following registers:

- Instruction register—determines which action to perform and which data register to access.
- Bypass register (1-bit long data register)—provides a minimum-length serial path between the TDI and TDO pins.
- Boundary-scan register—shift register composed of all the BSCs of the device.

Figure 1. JTAG Circuitry Functional Model

- Test access port (TAP) controller—controls the JTAG BST.
- TMS and TCK pins—operate the TAP controller.
- TDI and TDO pins—provide the serial path for the data and instruction registers.

Note: TRST pin is not available in Intel Stratix 10 devices.



2.2. JTAG Pins

Table 1. JTAG Pin Descriptions

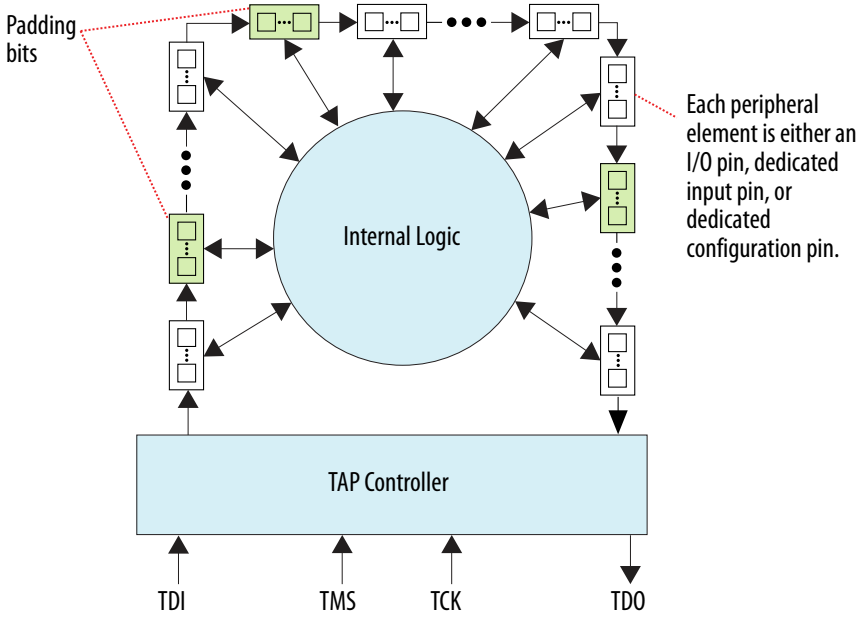
Pin	Function	Description
TDI	Serial input pin for: • Instructions • Test data • Programming data	• TDI is sampled on the rising edge of TCK and should be driven on the falling-edge of TCK. • TDI pins have internal weak pull-up resistors.
TDO	Serial output pin for: • Instructions • Test data • Programming data	• TDO is driven on the falling edge of TCK and should be sampled on the rising-edge of TCK. • The pin is tri-stated if data is not being shifted out of the device.
TMS	Input pin that provides the control signal to determine the transitions of the TAP controller state machine.	• TMS is sampled on the rising edge of TCK and should be driven on the falling-edge of TCK. • TMS pins have internal weak pull-up resistors.
TCK	The clock input to the BST circuitry.	—

2.3. IEEE Std. 1149.1 Boundary-Scan Register

The boundary-scan register is a large serial shift register that uses the TDI pin as an input and the TDO pin as an output. The boundary-scan register consists of boundary-scan cells for each I/O pin and padding bits. You can use the boundary-scan register to test external pin connections or to capture internal data.

Figure 2. Boundary-Scan Register

This figure shows how test data is serially shifted around the periphery of the IEEE Std. 1149.1 device.



Note: Padding bits are present in the scan-chain and must be ignored when read and must be written with 0.

2.3.1. Boundary-Scan Cells of Intel Stratix 10 Device I/O Pin

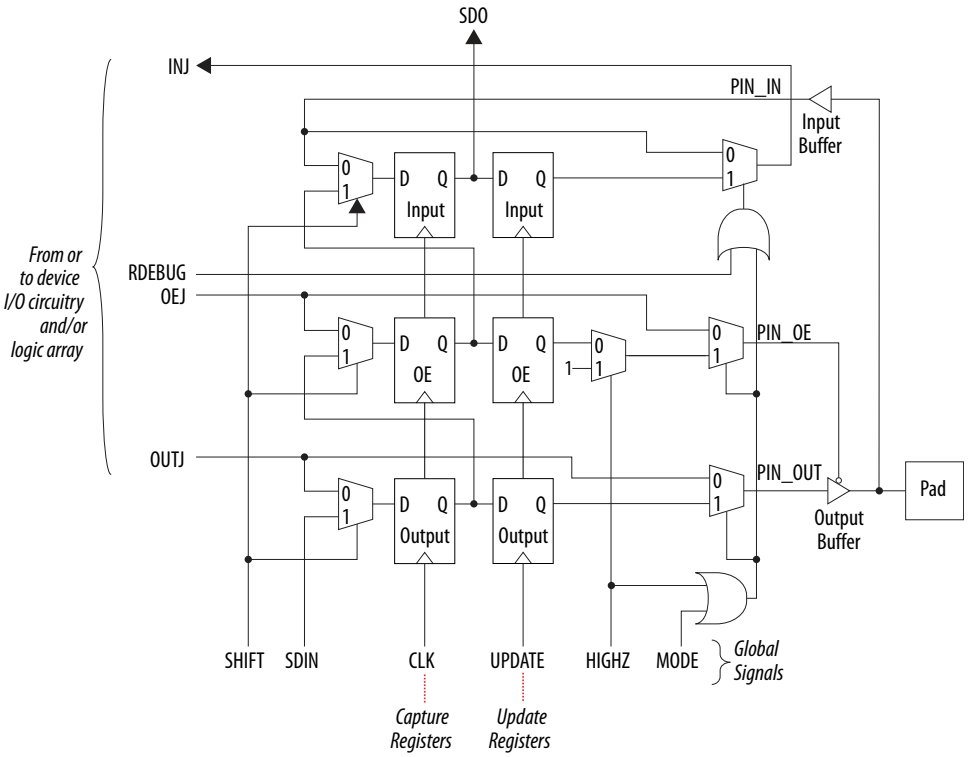
The Intel Stratix 10 device 3-bit BSC consists of the following registers:

- Capture registers—connect to internal device data through the OUTJ, OEJ, and PIN_IN signals.
- Update registers—connect to external data through the PIN_OUT and PIN_OE signals.

The TAP controller generates the global control signals for the IEEE Std. 1149.1 BST registers (SHIFT, CLOCK, and UPDATE) internally. A decode of the instruction register generates the MODE signal.

The data signal path for the boundary-scan register runs from the serial data in (SDI) signal to the serial data out (SDO) signal. The scan register begins at the TDI pin and ends at the TDO pin of the device.

Figure 3. User I/O BSC with IEEE Std. 1149.1 BST Circuitry for Intel Stratix 10 Devices



Note: TDI, TDO, TMS, TCK, TRST, VCC, GND, VREF, VSIGP, VSIGN, TEMPDIODE, and RREF pins do not have BSCs.

Table 2. Boundary-Scan Cell Descriptions for Intel Stratix 10 Devices

This table lists the capture and update register capabilities of all BSCs within Intel Stratix 10 devices.

Pin Type	Captures			Drives			Comments
	Output Capture Register	OE Capture Register	Input Capture Register	Output Update Register	OE Update Register	Input Update Register	
User I/O pins	OUTJ	OEJ	PIN_IN	PIN_OUT	PIN_OE	INJ	—
Dedicated input	0	1	PIN_IN	N.C.	N.C.	N.C.	PIN_IN drives to the core logic
Dedicated bidirectional (1)	0	OEJ	PIN_IN	N.C.	N.C.	N.C.	PIN_IN drives to the core logic
Dedicated output (2)	OUTJ	0	0	N.C.	N.C.	N.C.	OUTJ drives to the output buffer

2.4. IEEE Std. 1149.6 Boundary-Scan Register

The BSCs for HSSI transmitters (GXB_TX[p,n]) and receivers/input clock buffers (GXB_RX[p,n])/(REFCLK[p,n]) in Intel Stratix 10 devices are different from the BSCs for the I/O pins.

Note: You have to use the EXTEST_PULSE JTAG instruction for AC-coupling on HSSI transceiver. Do not use the EXTEST JTAG instruction for AC-coupling on HSSI transceiver. You can perform AC JTAG on the Intel Stratix 10 device before, after, and during configuration.

(1) This includes the NCONFIG, MSEL0, MSEL1, MSEL2, MSEL3, NCE, and PORSEL pins.

(2) This includes the CONF_DONE, NSTATUS, and DCLK pins.

Figure 4. HSSI Transmitter BSC for Intel Stratix 10 Devices

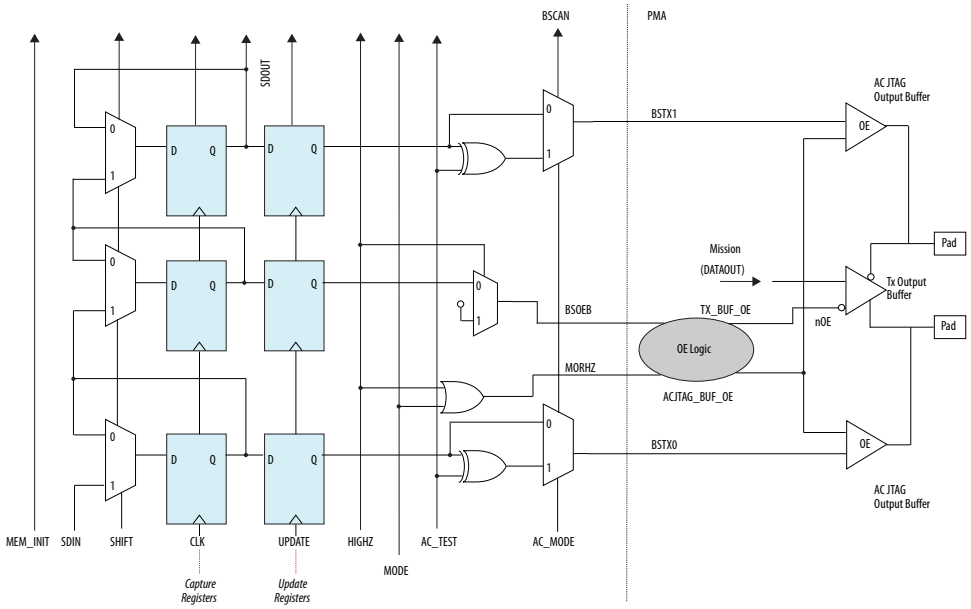


Figure 5. HSSI Receiver/Input Clock Buffer for Intel Stratix 10 Devices

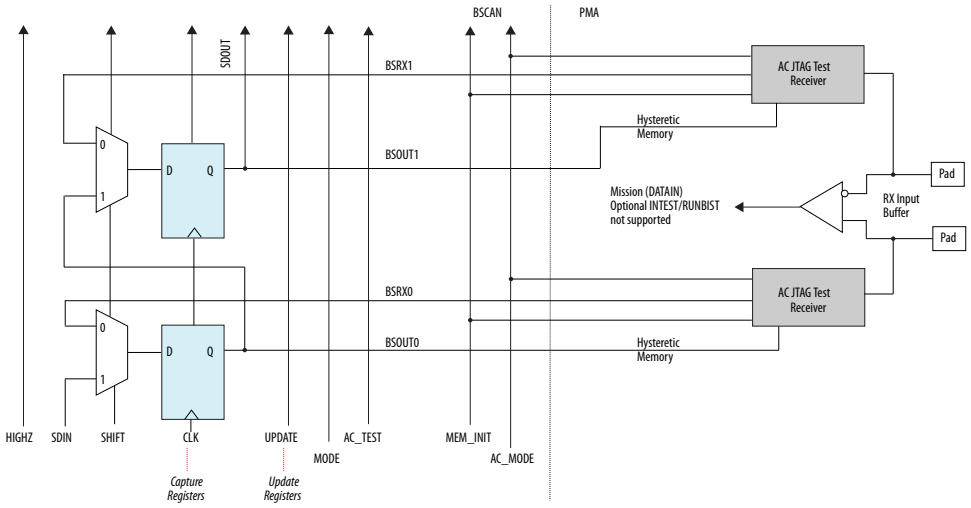
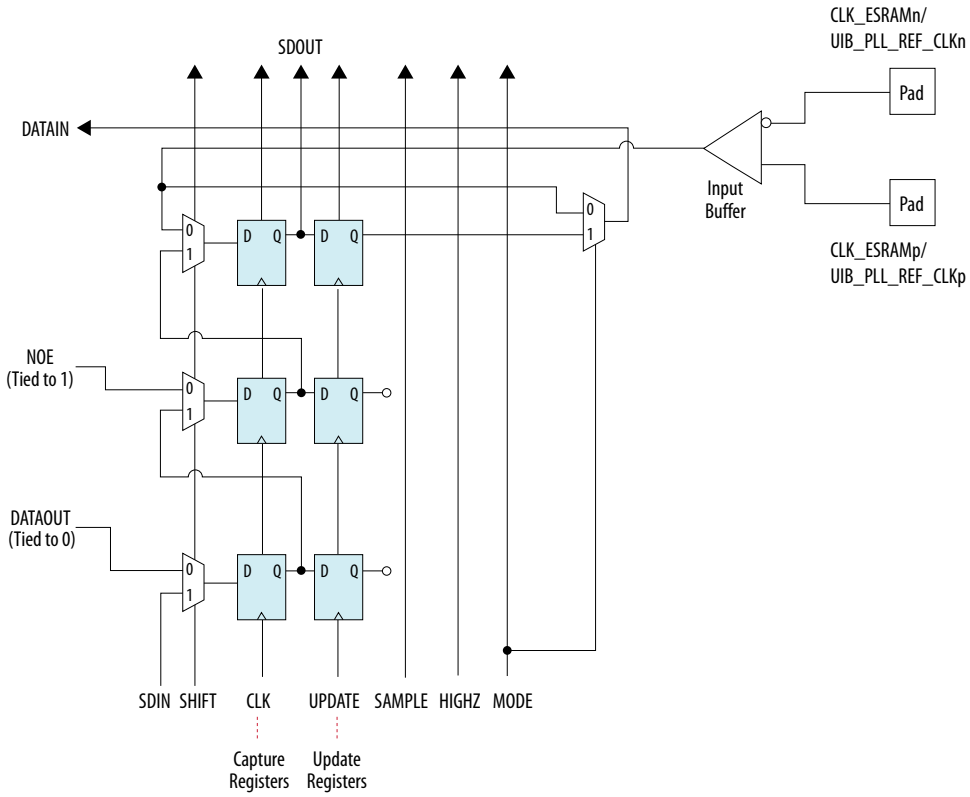


Figure 6. UIB and eSRAM BSC for Intel Stratix 10 Devices

The differential reference clock input pins for UIB and eSRAM are sharing the BSC per pair as shown in this figure. The capture value (DATAIN) would be invalid if one or both differential inputs are abnormal.



2.4.1. IEEE Std. 1149.6 BST Circuitry for Intel Stratix 10 E-Tile Transceiver

Figure 7. HSSI Transmitter BSC for Intel Stratix 10 E-Tile Transceiver

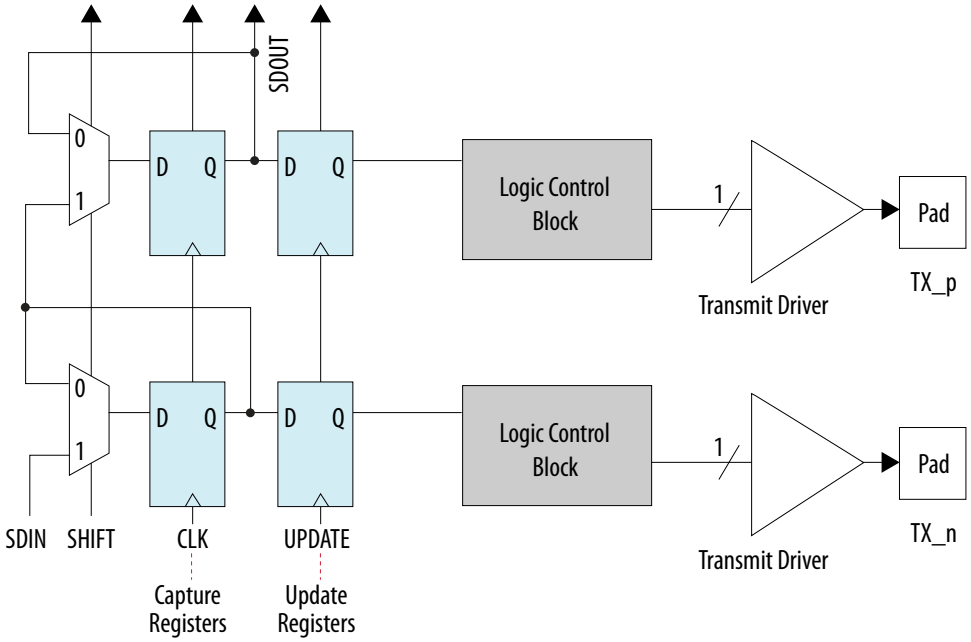
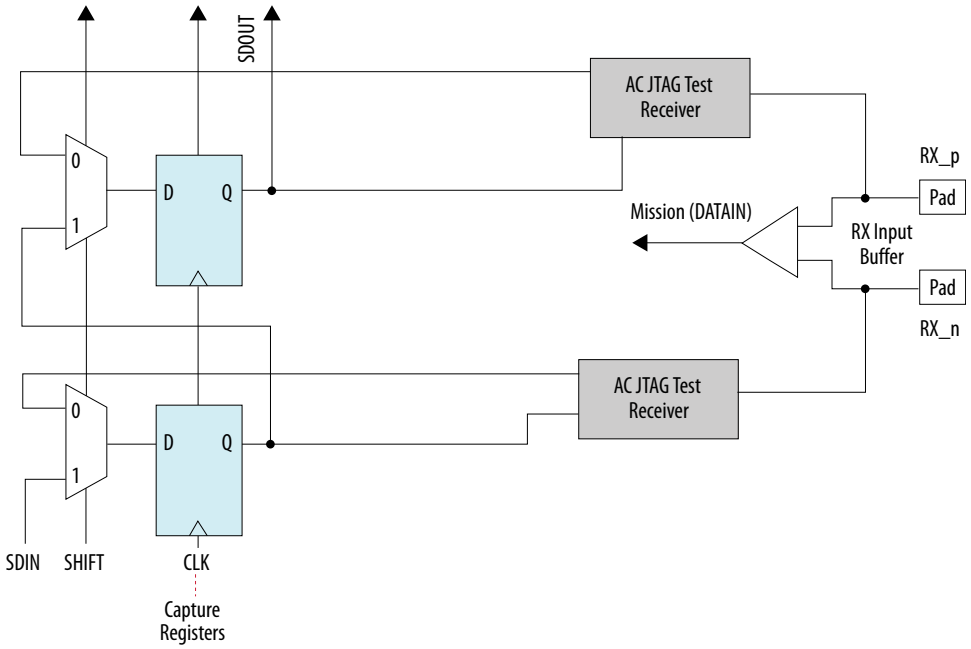


Figure 8. HSSI Receiver BSC for Intel Stratix 10 E-Tile Transceiver



2.4.2. IEEE Std. 1149.6 BST Circuitry for Intel Stratix 10 P-Tile Transceiver

Figure 9. HSSI Transmitter BSC for Intel Stratix 10 P-Tile Transceiver

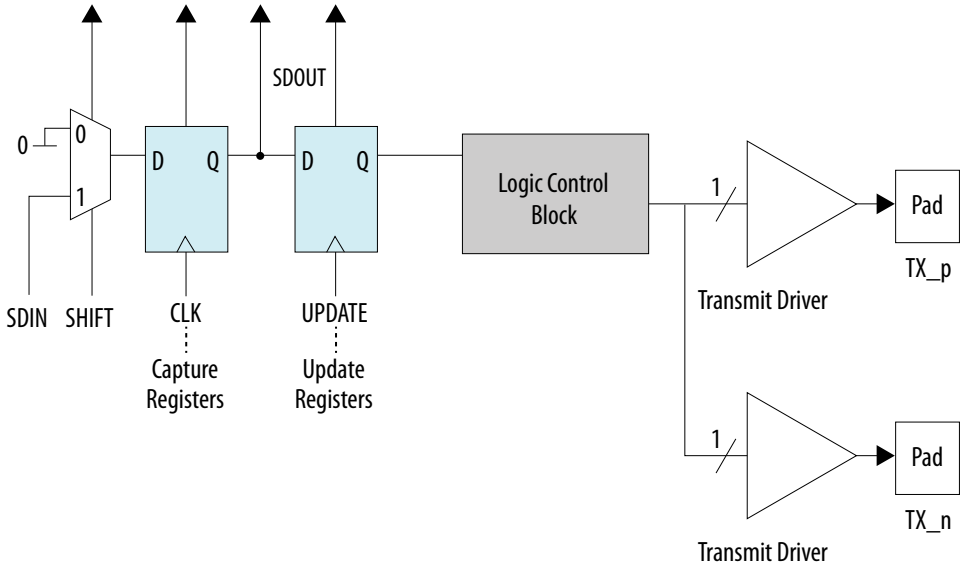


Figure 10. HSSI Receiver BSC for Intel Stratix 10 P-Tile Transceiver

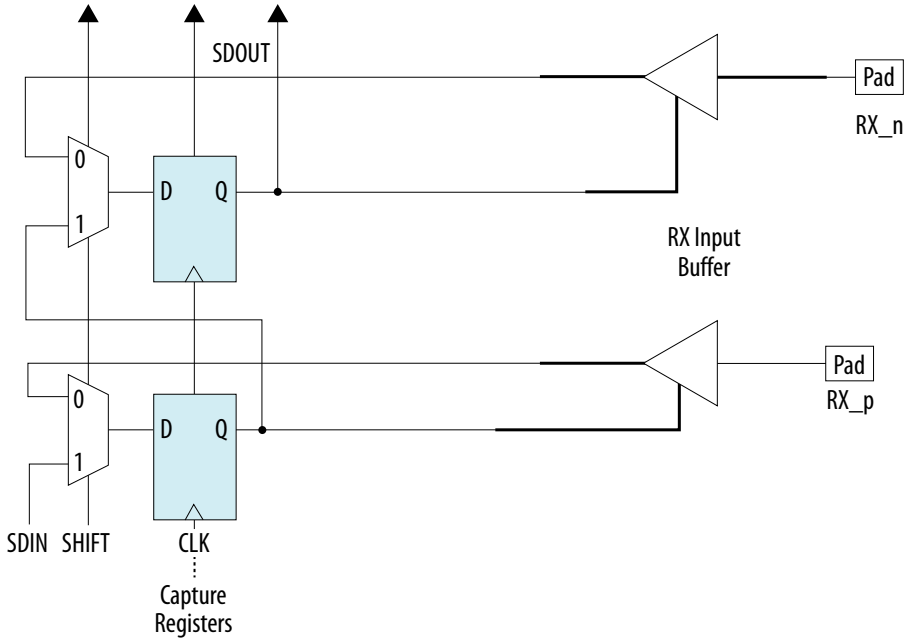
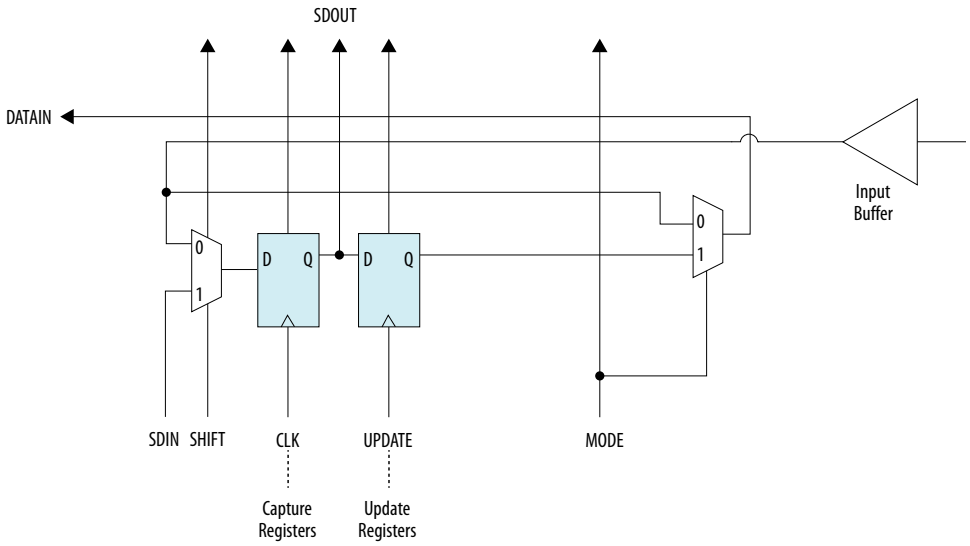


Figure 11. I_PIN_PERST_N Input Pin BSC for Intel Stratix 10 P-Tile Transceiver



3. Intel Stratix 10 BST Operation Control

3.1. Device ID

The device ID is unique for each Intel Stratix 10 device. Use this code to identify the devices in a JTAG chain.

Table 3. Device ID Information for Intel Stratix 10 Devices

Product Line	Device ID (32 bits)			
	Version (4 bits)	Part Number (16 Bits)	Manufacture Identity (11 Bits)	LSB (1 Bit)
1SG040H	0000	0011 0010 0010 0000	000 0110 1110	1
1SG065H	0000	0011 0010 0010 0001	000 0110 1110	1
1SG085H	0001	0011 0010 0010 0010	000 0110 1110	1
1SG110H	0000	0011 0010 0010 0010	000 0110 1110	1
1SG165H	1111	0011 0010 0010 0101	000 0110 1110	1
1SG166H	0101	0011 0010 0010 0100	000 0110 1110	1
1SG210H	1110	0011 0010 0010 0101	000 0110 1110	1
1SG210H(ES1)	0010	0011 0010 0010 0101	000 0110 1110	1
1SG211H	0100	0011 0010 0010 0100	000 0110 1110	1
1SG250L	1101	0011 0010 0001 0101	000 0110 1110	1
1SG250H	1101	0011 0010 0010 0101	000 0110 1110	1
1SG280L	1100	0011 0010 0001 0101	000 0110 1110	1
1SG280L(ES1)	0000	0011 0010 0001 0101	000 0110 1110	1
1SG280L(ES2)	0000	0011 0010 0010 0101	000 0110 1110	1
1SG280L(ES3)	1100	0011 0010 0001 0101	000 0110 1110	1
1SG280H	1100	0011 0010 0010 0101	000 0110 1110	1
1SG280H(ES1)	0000	0011 0010 0010 0101	000 0110 1110	1
1SG280H(ES2)	1100	0011 0010 0001 0101	000 0110 1110	1
1SG280H(ES3)	1100	0011 0010 0010 0101	000 0110 1110	1
1SX040H	0000	0011 0010 0010 1000	000 0110 1110	1
1SX065H	0000	0011 0010 0010 1001	000 0110 1110	1
1SX085H	0001	0011 0010 0010 1010	000 0110 1110	1
1SX110H	0000	0011 0010 0010 1010	000 0110 1110	1

continued...

Product Line	Device ID (32 bits)			
	Version (4 bits)	Part Number (16 Bits)	Manufacture Identity (11 Bits)	LSB (1 Bit)
1SX165H	1111	0011 0010 0010 1101	000 0110 1110	1
1SX210H	1110	0011 0010 0010 1101	000 0110 1110	1
1SX250L	1101	0011 0010 0001 1101	000 0110 1110	1
1SX250H	1101	0011 0010 0010 1101	000 0110 1110	1
1SX280L	1100	0011 0010 0001 1101	000 0110 1110	1
1SX280L(ES1)	0100	0011 0010 0001 1101	000 0110 1110	1
1SX280L(ES2)	0100	0011 0010 0001 1101	000 0110 1110	1
1SX280H	1100	0011 0010 0010 1101	000 0110 1110	1
1SX280H(ES1)	0100	0011 0010 0010 1101	000 0110 1110	1
1SX280H(ES2)	1100	0011 0010 0010 1101	000 0110 1110	1
1ST040E	0000	0011 0010 0011 1000	000 0110 1110	1
1ST085E	0001	0011 0010 0011 1010	000 0110 1110	1
1ST110E	0000	0011 0010 0011 1010	000 0110 1110	1
1ST165E	0001	0011 0010 0011 0100	000 0110 1110	1
1ST210E	0000	0011 0010 0011 0100	000 0110 1110	1
1ST250E	1101	0011 0010 0011 1101	000 0110 1110	1
1ST280E 1ST280E(ES1)	1100	0011 0010 0011 1101	000 0110 1110	1
1SM16BE 1SM16BE(ES1)	0011	0011 0010 1011 1100	000 0110 1110	1
1SM16BH	0011	0011 0010 1010 1100	000 0110 1110	1
1SM16CH	0001	0011 0010 1010 1100	000 0110 1110	1
1SM21BE 1SM21BE(ES1)	0010	0011 0010 1011 1100	000 0110 1110	1
1SM21BH 1SM21BH(ES1)	0010	0011 0010 1010 1100	000 0110 1110	1
1SM21CH 1SM21CH(ES1)	0000	0011 0010 1010 1100	000 0110 1110	1
1SD110P	0000	0011 0010 0100 1010	000 0110 1110	1
1SD21BP	0110	0011 0010 1100 1100	000 0110 1110	1
1SD280P	1100	0011 0010 0100 0101	000 0110 1110	1

3.2. Supported JTAG Instructions

Table 4. JTAG Instructions Supported by Intel Stratix 10 Devices

Caution: Never invoke instruction codes other than the supported JTAG instructions in the following table. Invoking unsupported instruction can damage and render the device unusable.

JTAG Instruction	Instruction Code	Description
MISCCTRL	00 0001 0011	• Required instruction to enable the boundary-scan circuitry for JTAG BST. • Set the LSB of the 8-bit data register to '1' and the remaining bits to '0' to enable the boundary-scan circuitry.
SAMPLE(3)/PRELOAD	00 0000 0101	• Allows you to capture and examine a snapshot of signals at the device pins during normal device operation and permits an initial data pattern to be an output at the device pins. • Use this instruction to preload the test pattern into the update registers before loading the EXTEST instruction.
EXTEST	00 0000 1111	• Board-level interconnects by forcing a test pattern at the output pins, and capturing the test results at the input pins. Forcing known logic high and low levels on output pins allows you to detect opens and shorts at the pins of any device in the scan chain. • The high-impedance state of EXTEST is overridden by bus hold and weak pull-up resistor features.
BYPASS	11 1111 1111	• Places the 1-bit bypass register between the TDI and TDO pins. During normal device operation, the 1-bit bypass register allows the BST data to pass synchronously through the selected devices to adjacent devices. • You will get a '0' reading in the bypass register out.
USERCODE	00 0000 0111	• Selects the 32-bit USERCODE register and places it between the TDI and TDO pins to allow serial shifting of USERCODE out of TDO. • The 32-bit USERCODE is a programmable user-defined pattern.
IDCODE	00 0000 0110	• Identifies the devices in a JTAG chain. When the IDCODE register is selected by the IR then in the CAPTURE_DR state, the IDCODE instruction places the 32-bit Device ID register between the TDI and TDO pins to allow serial shifting of Device ID out of TDO. • Selects the Device ID register and places it between the TDI and TDO pins to allow serial shifting of Device ID register out of TDO. • IDCODE instruction is the default instruction in the Test-Logic-Reset state.
HIGHZ	00 0000 1011	• Sets all user I/O pins to an inactive drive state. • Places the 1-bit bypass register between the TDI and TDO pins. • The programmable weak pull-up resistor or the bus hold feature overrides the HIGHZ value at the pin.
CLAMP	00 0000 1010	• Places the 1-bit bypass register between the TDI and TDO pins. • The programmable weak pull-up resistor or the bus hold feature overrides the CLAMP value at the pin. The CLAMP value is the value stored in the update register of the boundary-scan cell (BSC).
EXTEST_PULSE	00 1000 1111	Enables board-level connectivity checking between the transmitters and receivers that are AC coupled by generating three output transitions:

continued...

(3) SAMPLE instruction is not supported for high-speed serial interface (HSSI) pins.

JTAG Instruction	Instruction Code	Description
		• Driver drives data on the falling edge of TCK in the UPDATE_IR/DR state. • Driver drives inverted data on the falling edge of TCK after entering the RUN_TEST/IDLE state. • Driver drives data on the falling edge of TCK after leaving the RUN_TEST/IDLE state.
EXTEST_TRAIN	00 0100 1111	Behaves the same as the EXTEST_PULSE instruction except that the output continues to toggle on the TCK falling edge provided that the TAP controller is in the RUN_TEST/IDLE state.

Related Information

Device ID on page 13

3.3. JTAG Secure Mode

JTAG Secure mode in Intel Stratix 10 devices is supported through the Secure Device Manager (SDM).

4. Intel Stratix 10 I/O Voltage for JTAG Operation

The Intel Stratix 10 device operating in IEEE Std. 1149.1 and IEEE Std. 1149.6 modes uses four required JTAG pins—TDI, TDO, TMS, and TCK.

The TCK pin has an internal weak pull-down resistor, while the TDI and TMS pins have internal weak pull-up resistors. The V_{CCIO_SDM} supply powers the TDI, TDO, TMS, and TCK pins.

The JTAG pins support 1.8 V TTL/CMOS I/O standard.

Note: For any voltages higher than 1.8 V, you have to use level shifter. The output voltage of the level shifter for the JTAG pins must be the same as set for the V_{CCIO_SDM} supply.

Table 5. TDO Output Buffer

TDO Output Buffer Condition	Voltage (V)
V_{CCIO_SDM}	1.8

5. Performing Intel Stratix 10 Boundary-Scan Testing

You can issue BYPASS, IDCODE, and SAMPLE JTAG instructions before, after, or during configuration without having to interrupt configuration.

To interrupt configuration in order to perform BST, you can either hold nCONFIG low or issue the following sequence via JTAG: an IR scan updating with 0x201 (COMMAND) followed by two 34 bit DR scans updating with 34'h3_0000_0000 then 35'h1_0000_0005. Once configuration is interrupted, you can issue other JTAG instructions to perform BST.

If you design a board for JTAG configuration using Intel Stratix 10 devices, consider the connections for the dedicated configuration pins.

Note: Dummy bits exist in the boundary-scan register during boundary-scan operations in Intel Stratix 10 devices. However, these dummy bits do not have any impact on the pins. The dummy bits appear on the TDO immediately before the corresponding boundary-scan register segment and have an unknown value *X*, which can be either a 0 or 1.

SoC Devices

For SoC device, you can only see the FPGA TAP controller in the JTAG chain upon device power up. The TAP controller for the HPS component only appears in the JTAG chain once the device is configured with a programming file/design containing the HPS component. You need to include the information about the HPS component when generating the test patterns for boundary-scan testing. You can download the boundary-scan description language (BSDL) file for the SoC device from the *Intel Stratix 10 Device BSDL Files* page.

1SG040 and 1SX040 Devices

For 1SG040 and 1SX040 devices, you must follow the guidelines to perform BST on I/O bank 3C to avoid broken chain in the device.

Table 6. Boundary-Scan Cell Location and the Corresponding I/O Pins

You must set a constant value on the dedicated boundary-scan cell.

Boundary-Scan Cell Location in BSDL File	Boundary-Scan Cell Value	I/O Pins Location
469	1	U3, V3, U5, V4, W2, Y1, W3, W4
466	0	
457 (4)	0 = output	

continued...

(4) Set this boundary-scan cell to '0' to perform drive-out test on the listed I/O pins. Set to '1' to perform capture test on the listed I/O pins.

Boundary-Scan Cell Location in BSDL File	Boundary-Scan Cell Value	I/O Pins Location
	1 = input	
577	1	Y2, AA2, AB1, AB2, AC1, AD1, AF2, AG2
586	0	
574 (4)	0 = output 1 = input	
481	1	AE1, AE2, AD2, AD3, AF3, AF4, AG3, AH3
478	0	
454 (4)	0 = output 1 = input	
583	1	AG1, AH1, AJ1, AK1, AJ2, AJ3, AK2, AL2
589	0	
580 (4)	0 = output 1 = input	
475	1	AE4, AE5, Y4, AA4, AA3, AB3, AC3, AD4
472	0	
463 (4)	0 = output 1 = input	
451	1	AM1, AM2, Y5, AA5, AC4, AB5, AC5, AB6
460	0	
448 (4)	0 = output 1 = input	

Related Information

Intel Stratix 10 Device BSDL Files page
Provides the BSDL files for the Intel Stratix 10 devices.

6. Enabling and Disabling Intel Stratix 10 BST Circuitry

6.1. Enabling BST Circuitry

The IEEE Std. 1149.1 BST circuitry is enabled after the device is configured. If you need to perform the boundary-scan test prior to configuration, you must execute the MISCCTRL instruction upon device power up to enable the BST circuitry.

Example 1. MISCCTRL Instruction

```
!Shift 10-bit MISCCTRL instruction (0x013) to Instruction Register
SIR 10 TDI (013);
!Transition to Run-Test-Idle state
STATE IDLE;
!Shift 8-bit data (0x01) to Data Register for BST circuitry enabling
SDR 8 TDI (01);
```

6.2. Disabling BST Circuitry

To ensure that you do not inadvertently enable the IEEE Std. 1149.1 circuitry when it is not required, disable the circuitry permanently with pin connections as listed in the following table.

Table 7. Pin Connections to Permanently Disable the IEEE Std. 1149.1 Circuitry for Intel Stratix 10 Devices

JTAG Pins[5]	Connection for Disabling
TMS	V_{CCIO_SDM}
TCK	GND
TDI	V_{CCIO_SDM}
TDO	Leave open

(5) The JTAG pins are dedicated. Software option is not available to disable JTAG in Intel Stratix 10 devices.

7. Intel Stratix 10 IEEE Std. 1149.1 BST Guidelines

Consider the following guidelines when you perform BST with IEEE Std. 1149.1 devices:

- If the first two bits shifted out of the instruction register in the SHIFT_IR state are not 1 and then 0, the TAP controller did not reach the proper state. To solve this problem, try one of the following procedures:
  - Verify that the TAP controller has reached the SHIFT_IR state correctly. To advance the TAP controller to the SHIFT_IR state, return to the TEST-LOGIC-RESET state and send the 01100 code to the TMS pin.
  - Check the connections to the VCC, GND, JTAG, and dedicated configuration pins on the device.
- Perform a SAMPLE/PRELOAD test cycle before the first EXTEST test cycle to ensure that known data is present at the device pins when you enter EXTEST mode. If the OEJ update register contains 0, the data in the OUTJ update register is driven out. The state must be known and correct to avoid contention with other devices in the system.
- Do not perform EXTEST testing during in-circuit reconfiguration because EXTEST is not supported during in-circuit reconfiguration.
- After configuration, you cannot test any pins in a differential pin pair. To perform BST after configuration, edit and redefine the BSC group that correspond to these differential pin pairs as an internal cell.

8. Document Revision History for the Intel Stratix 10 JTAG Boundary-Scan Testing User Guide

Document Version	Changes
2020.03.13	Updated the *Device ID Information for Intel Stratix 10 Devices* table. • Added 1SG280H(S3) device. • Rearranged the device ID information for better clarity.
2019.12.24	• Added the following devices in the *Device ID Information for Intel Stratix 10 Devices* table: — 1SG040H — 1SX040H • Updated the descriptions for HIGHZ and CLAMP JTAG instructions in the *JTAG Instructions Supported by Intel Stratix 10 Devices* table. • Added information for 1SG040 and 1SX040 devices in the *Performing Intel Stratix 10 Boundary-Scan Testing* section.
2019.11.07	• Added diagrams for IEEE Std. 1149.6 BST Circuitry for Intel Stratix 10 P-Tile Transceiver. • Added the following devices in the *Device ID Information for Intel Stratix 10 Devices* table: — 1SD110P — 1SD21BP — 1SD280P — 1SX065H
2019.09.30	Added the following devices in the *Device ID Information for Intel Stratix 10 Devices* table. • 1SG065H • 1ST040E • 1ST085E • 1ST110E
2019.07.01	• Updated the figure titles in the following sections: — *IEEE Std. 1149.6 Boundary-Scan Register* — *IEEE Std. 1149.6 BST Circuitry for Intel Stratix 10 E-Tile Transceiver* • Updated the *Device ID Information for Intel Stratix 10 Devices* table. — Added 1SG166H and 1SG211H. — Removed unsupported device: 1SM11AH. • Updated the description for SAMPLE/PRELOAD in the *JTAG Instructions Supported by Intel Stratix 10 Devices* table.
2019.01.08	Added the following diagrams in the *IEEE Std. 1149.6 Boundary-Scan Register* section. • UIB and eSRAM BSC with IEEE Std. 1149.1 BST Circuitry for Intel Stratix 10 Devices • HSSI Transmitter BSC with IEEE Std. 1149.6 BST Circuity for Intel Stratix 10 E-Tile Transceiver • HSSI Receiver BSC with IEEE Std. 1149.6 BST Circuity for Intel Stratix 10 E-Tile Transceiver

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Document Version	Changes
2018.09.24	• Updated the following product lines in the *Device ID Information for Intel Stratix 10 Devices* table. — Updated 1ST280E/ES1 to 1ST280E and 1ST280E(ES1) — Updated 1SM11AH/ES1 to 1SM11AH — Updated 1SM16BE/ES1 to 1SM16BE and 1SM16BE(ES1) — Updated 1SM16BH/ES1 to 1SM16BH — Updated 1SM16CH/ES1 to 1SM16CH — Updated 1SM21BE/ES1 to 1SM21BE and 1SM21BE(ES1) — Updated 1SM21BH/ES1 to 1SM21BH and 1SM21BH(ES1) — Updated 1SM21CH/ES1 to 1SM21CH and 1SM21CH(ES1) • Updated the *JTAG Instructions Supported by Intel Stratix 10 Devices* table. — Updated the description for the USERCODE JTAG instruction. — Removed the COMMAND, RESPONSE, and PROGRAM JTAG instructions. • Updated the note in the *Performing Intel Stratix 10 Boundary-Scan Testing* section. • Updated the description in the *Enabling BST Circuitry* section. • Updated the MISCCTRL Instruction example.
2018.07.11	Updated the device ID – part number for 1SG280L (ES2) and 1SG280H (ES2) in the *Device ID Information for Intel Stratix 10 Devices* table.
2018.05.07	• Added MISCCTRL instruction code in *Supported JTAG Instructions*. • Added a note to *Enabling BST Circuitry* stating that the MISCCTRL instruction is required before performing boundary-scan testing. • Updated the *Device ID Information for Intel Stratix 10 Devices* table.

Date	Version	Changes
November	2017.11.06	Updated Device ID code.
May 2017	2017.05.08	Updated Device ID code.
October 2016	2016.10.31	Initial release.