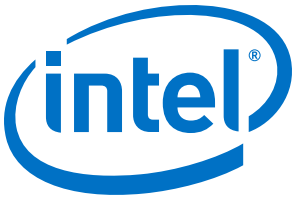


Intel® FPGA Power and Thermal Calculator User Guide

Updated for Intel® Quartus® Prime Design Suite: **19.4**

Subscribe
Send Feedback

UG-20252 | 2020.02.14
Latest document on the web: PDF | HTML

Contents

1. Overview of the Intel® FPGA Power and Thermal Calculator

This user guide describes the Intel® FPGA Power and Thermal Calculator (PTC).For version 19.4, the PTC supports Intel Agilex™ devices.

This user guide provides guidelines for using the PTC, and details about thermal analysis and the factors contributing to FPGA power consumption.

You can calculate FPGA power consumption using the PTC, and for more accurate power estimation, use the Power Analyzer in the Intel Quartus® Prime software. Intel recommends that you switch from the PTC to the Power Analyzer once your design is available. The Power Analyzer produces more accurate results because it has more detailed information about your design, including routing and configuration information about each of the resources in your design.

You should treat the PTC results as an estimate of power, not as a specification. You must verify the actual power consumption during device operation, because the information is sensitive to the actual device and design input signals. See the appendix *Measuring Static Power* for information on how to measure device static power in a way that correlates with the way that PTC reports static power.

The features of the PTC include:

- The ability to estimate the power consumption of your design before creating the design or during the design process.

1.1. Intel FPGA PTC Power Model Status

The power models in the Power and Thermal Calculator (PTC) can be in advance, preliminary, or final status.

The Main tab of the Power and Thermal Calculator shows the current power model status for the selected device. Power models may be at an *advance*, *preliminary*, or *final* state:

- Advance power models are based on simulation results, process model projections, and design targets. Advance power models may change over time.
- Preliminary power models include post-layout simulation results, process data, and initial silicon correlation results. Preliminary power models may change over time.
- Final power models correlate to production devices with thousands of designs, and are not expected to change.

The accuracy of the power model is determined on a per-power-rail basis for both the Power Analyzer and the Power and Thermal Calculator. For most designs, the Power Analyzer and the PTC have the following accuracies, assuming final power models:

Intel Corporation. All rights reserved. Agilex, Altera, Arria, Cyclone, Enpirion, Intel, the Intel logo, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.
*Other names and brands may be claimed as the property of others.

ISO 9001:2015 Registered

- Power Analyzer: Within 10% of silicon for the majority of power rails and the highest power rails, assuming accurate inputs and toggle rates.
- Power and Thermal Calculator: Within 15% of silicon for the majority of power rails and the highest power rails, assuming accurate inputs and toggle rates.

1.2. Definitions of Power Terms Used in this Document

The total power consumption of an Intel Agilex device consists of the following components:

- Static power—the power that the configured device consumes when powered up but no user clocks are operating.
- Dynamic power—the additional power consumption of the device due to signal activity or toggling.

2. Setting Up the Intel FPGA Power and Thermal Calculator

2.1. Availability

For Intel Agilex devices, the Intel FPGA Power and Thermal Calculator is integrated with the Intel Quartus Prime software. You can access the Power and Thermal Calculator (PTC) from the **Tools** menu in the Intel Quartus Prime software, or by running the `quartus_ptc` command in your command shell.

For the convenience of designers who may be working only on power estimation and not running design compilations with the Intel Quartus Prime software, a standalone version of the PTC is also available. The standalone version offers all the same features as the version integrated within the Intel Quartus Prime software.

Licensing: The Intel FPGA Power and Thermal Calculator is a licensed feature. Contact your Intel representative to obtain a license.

Note: To use the Power and Thermal Calculator, you must have either the standalone Power and Thermal Calculator or the Intel Quartus Prime software installed with Intel Agilex device support, and a license for the Power and Thermal Calculator.

2.2. Obtaining the Standalone Intel FPGA Power and Thermal Calculator

The standalone Power and Thermal Calculator (PTC) is available from the *Additional Software* tab of the Intel Quartus Prime Pro Edition page of the *Download Center for FPGAs*, here: https://fpgasoftware.intel.com/19.4/?edition=pro.

Both the standalone version and the version integrated into the Intel Quartus Prime software require a license for use.

2.3. Estimating Power Consumption with the Intel FPGA Power and Thermal Calculator

With the Intel FPGA Power and Thermal Calculator (PTC), you can estimate power consumption at any point in your design cycle.

Intel Corporation. All rights reserved. Agilex, Altera, Arria, Cyclone, Enpirion, Intel, the Intel logo, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.
*Other names and brands may be claimed as the property of others.

ISO 9001:2015 Registered

You can estimate the power consumption when you have not yet begun your design, or if your design is partially complete. Although the PTC can provide a power estimate for your completed design, Intel recommends that you use the Power Analyzer in the Intel Quartus Prime software when the design is available, for a more accurate estimate based on the exact placement and routing information of the completed design.

2.3.1. Estimating Power Consumption Before Starting the FPGA Design

Table 1. Advantage and Constraints of Power Estimation before Designing FPGA

Advantage	Constraint
• You can obtain power estimates before starting your FPGA design. • You can adjust design resources and parameters and see how those changes affect total power consumption.	• Accuracy depends on your inputs and your estimate of the device resources; where this information may change (during or after your design is complete), your power estimation results may be less accurate. • The Power and Thermal Calculator uses averages and not the actual design implementation details. The Power Analyzer has access to the full design details. For example, the PTC uses average values for ALM configuration, while the Power Analyzer user an exact configuration for each ALM. • As of version 19.4, the Power and Thermal Calculator cannot import device resources from a design implemented in the Intel Quartus Primesoftware. You can, however, capture the implementation details manually from the fitter report to make the Power and Thermal Calculator output closer to the implementation than what you would get by your estimate of device resources.

To estimate power consumption with the PTC before starting your FPGA design, follow these steps:

1. On the Main tab of the PTC, select the target family, device, and package from the **Family**, **Device**, **Device Grade**, **Package**, and **Transceiver Grade** drop-down lists.
2. Enter values for each tab in the PTC. Different tabs display different power sections, such as clocks and phase-locked loops (PLLs).
3. The calculator displays the total estimated power consumption in the **Total Power (W)** cell of the Power Summary.
4. Save the file as <*project_name*>.ptc for later use.

2.3.2. Estimating Power Consumption While Creating the FPGA Design

Table 2. Advantages and Constraints of Power Estimation if your FPGA Design is Partially Complete

Advantage	Constraint
• You can perform power estimation early in the FPGA design cycle. • You can adjust design resources and parameters and see how those changes affect total power consumption.	• Accuracy depends on your inputs and your estimate of the device resources; where this information may change (during or after your design is complete), your power estimation results may be less accurate. • Unlike the Power Analyzer, which has access to the full design details, the PTC uses averages and not the actual design implementation. For example, the PTC uses average values for ALM configuration., while the Power Analyzer uses an exact configuration for each ALM. • As of version 19.4, the Power and Thermal Calculator cannot import device resources from a design implemented in the Intel Quartus Primesoftware. You can, however, capture the implementation details manually from the fitter report to make the Power and Thermal Calculator output closer to the implementation than what you would get by your estimate of device resources.

Importing a File

To update the power estimate of a design that is partially complete, with some actual device resource counts from a design in progress, you can update a previously created **.ptc** file.

Importing a **.ptc** file saves you time and effort otherwise spent on manually entering all the information once again into the PTC. You can also manually change any of the values after importing a file.

Importing Data into the Power and Thermal Calculator

You must import the PTC file into the PTC before modifying any information. Also, you must verify all your information after importing a file.

Importing a file from the Intel Quartus Prime software populates all input values that were specified in the Intel Quartus Prime software. Alternatively, you can import values exported from an earlier version of the PTC.

Importing resource usage details directly from a compiled design will be supported in a future version of the software. Currently you can import a **.ptc** file generated in a previous version of the software. After importing a **.ptc** file, you can manually edit its values to suit your changing design requirements.

To import data into the PTC, follow these steps:

1. On the **File** menu, click **Open**.
2. Browse to an existing PTC file generated by the current or earlier version of the PTC, and click **Open**. The file has the name <*revision name*>`_early_pwr.ptc`.
3. After the file is imported into the PTC, the mouse cursor changes from busy to normal. If there are any warnings during the importation, the PTC displays the **PTC Import Warnings** dialog box. Analyze each warning carefully to understand the cause; if any of the warnings are unexpected, you must manually modify the corresponding fields in the PTC after the importation is completed. You can copy all warning messages to the clipboard for future reference by clicking **Copy**. Click **OK** to dismiss the **PTC Import Warnings** dialog box. (Examples of warnings that

could occur, would be if device ordering codes had changed such that previous values for Device Grade, Device, and Package and Transceiver Grade fields could not be imported directly, or if the V_{CC} voltage isn't applicable to the selected device.)

2.3.3. Estimating Power Consumption After Completing the FPGA Design

If your design is complete, Intel strongly recommends that you do not use the Power and Thermal Calculator, and instead use the Power Analyzer in the Intel Quartus Prime software. The Power Analyzer uses toggle rates from simulation, user assignments, and placement-and-routing information to provide more accurate power estimates.

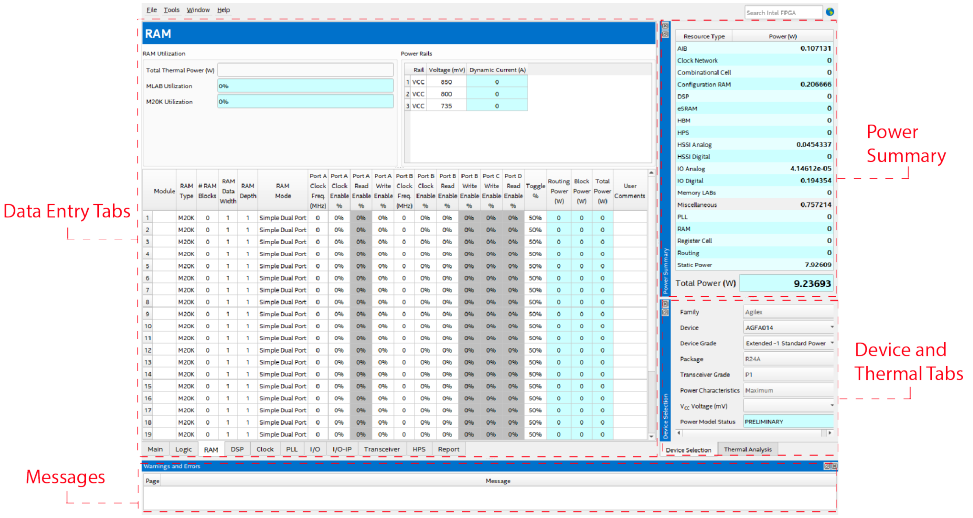
3. Intel FPGA Power and Thermal Calculator Graphical User Interface

The Intel FPGA Power and Thermal Calculator employs a standard graphical user interface (GUI) similar to other tools in the Intel Quartus Prime software.

In general, input fields are not shaded, and are editable, either by double-clicking and selecting a value from a popup or by typing a value directly. Fields that are not editable do not allow you to change their values.

Fields that are shaded in light blue contain calculated values, based on parameters that you have entered in the data entry tabs.

Figure 2. Power and Thermal Calculator Graphical User Interface (GUI)



Data Entry Tabs

The data entry area provides tabs for entering parameters associated with various aspects of your design.

Power Summary

The Power Summary shows the calculated power consumption of various types of resources, based on the current values in the data entry tabs. The fields of the Power Summary cannot be edited directly, and therefore are shaded in light blue as read-only.

Intel Corporation. All rights reserved. Agilex, Altera, Arria, Cyclone, Enpirion, Intel, the Intel logo, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.
*Other names and brands may be claimed as the property of others.

ISO 9001:2015 Registered

Device and Thermal Analysis Tabs

The **Device** and **Thermal Analysis** tabs summarize device characteristics and presumed thermal operating conditions, respectively. This information is also available on the **Main** tab of the data entry area.

Messages Window

The **Messages** area at the bottom of the screen displays any warning or error messages that may occur.

3.1. Intel FPGA PTC Data Entry Tabs

The Intel FPGA Power and Thermal Calculator (PTC) is a tool within the Intel Quartus Prime software that allows you to enter information into tabs based on architectural features. The PTC then reports, in watts, subtotals of the power consumed by each architectural feature.

- The **Main** tab allows you to enter device, package, and cooling information, and displays thermal analysis information.
- The **Logic** tab allows you to enter logic resources for all modules in your design.
- The **RAM** tab represents design modules using RAM blocks. Among other information, enter RAM type, data width, RAM depth (if applicable), RAM mode, and port parameters.
- The **DSP** tab represents DSP design modules. Among other information, enter DSP configuration, clock frequency, toggle percentage, and register usage.
- The **Clock** tab represents clock networks or separate clock domains.
- The **PLL** tab represents one or more I/O PLLs in the device. (This tab does not apply to transceiver PLLs.)
- The **I/O** tab represents design modules using general-purpose I/O pins. (This tab does not apply to transceiver I/O pins.) Among other information, enter I/O standard, input termination, current strength or output termination, data rate, clock frequency, output enable static probability, and capacitive load.
- The **I/O-IP** tab represents design modules using complex I/O IP, such as DDR.
- The **Transceiver** tab allows you to enter transceiver resources and their settings for all modules in your design.
- The **HPS** tab applies to Intel Agilex devices with HPS.
- The **Report** tab shows per-rail currents calculated by the Intel FPGA Power and Thermal Calculator (PTC).

3.2. Intel FPGA PTC Field Types

The Intel FPGA Power and Thermal Calculator employs input fields with which you configure the tool for your design, output fields which report calculated values, and input/output fields, which can serve as both inputs and outputs, depending on circumstances.

Field Types

Input fields let you enter information about the device and design for which you want to calculate power estimates. Some input fields let you type values directly, and others let you select from a list of values on a dropdown menu.

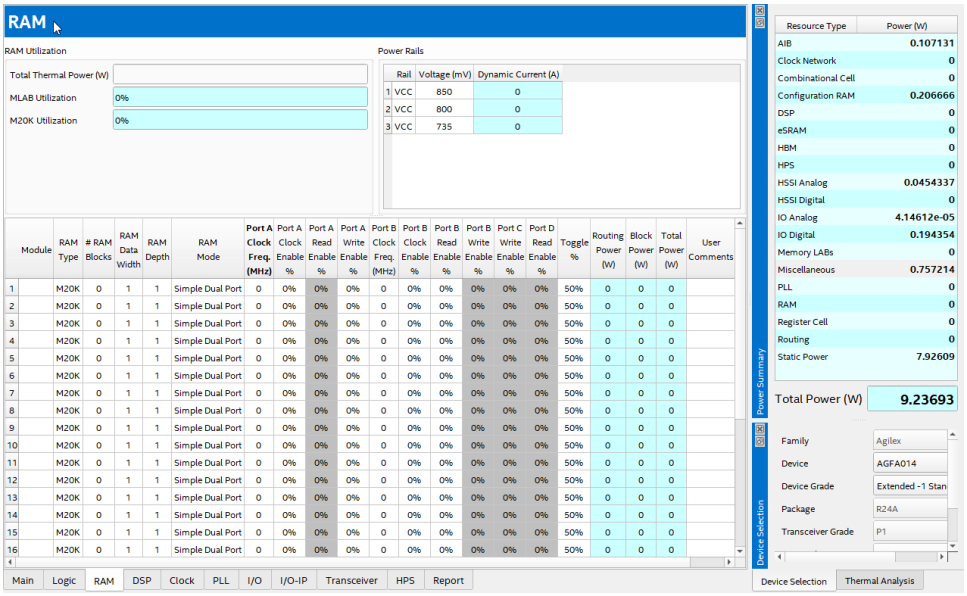
Output fields display estimated values for power, current, temperature, or resource utilization for a design specification that you have entered into the Power and Thermal Calculator.

Input/output fields fields may serve as input fields in some configurations, and output fields in others. For example, you may enter a *Pin Clock Frequency* value manually for some I/O modes, while in other I/O modes *Pin Clock Frequency* is calculated automatically, based on values of other input fields. If you enter a value into an input/output field when it is serving as an output, there is no effect. The value reverts to the calculated value.

Field Shading

The Power and Thermal Calculator uses shading to distinguish between input and output fields, and to help identify fields with only one allowed value.

Figure 3. Field Shading in the PTC GUI



Regular input fields, such as the **Module**, **RAM Type**, **# RAM Blocks**, and other columns in the above figure, have white shading. White shading also denotes input/output fields.

Input fields that currently have only one allowed value, such as **Port A Read Enable %**, **Port B Write Enable %**, and others in this example, have gray shading. A different combination of specified parameters might allow for more than one allowed value for these fields, in which case the field shading would become white, to allow user input.

Output fields, such as those in the **Routing Power (W)**, **Block Power (W)**, and **Total Power (W)** columns, as well as all of the fields in the **Power Summary** section, have pale blue shading.

3.3. Intel FPGA PTC Input Field Dependencies

The value you specify for some input fields may affect the allowed values for other fields.

For example, the device package that you select may determine what transceiver grades are selectable. If you change the selected device package, and the currently selected transceiver grade is still legal for the new package, the **Transceiver Grade** value does not change. However, if the currently selected transceiver grade is not compatible with the selected device package, the **Transceiver Grade** value automatically changes to one of the legal values.

Changes that you make in one tab may affect values on another tab, because of dependencies between input fields. For example, if you select a device that does not support the current I/O standard specified in the I/O tab, that I/O standard automatically changes to one of the I/O standards supported by the new device.

In general, the Intel FPGA Power and Thermal Calculator does not automatically change an input value unless it is necessary to preserve the legality of the input. Changes in one field have minimal impact on other fields, while ensuring that overall combination of field values are legal. However, this can sometimes lead to unanticipated results. Consider the following example:

Assume that **Dev1** is selected in the Main tab, and I/O standard **IO1** is selected in the I/O tab. Assume also that device **Dev1** supports I/O standards **IO1** and **IO2**. Suppose that you change the device selection to **Dev2**, which supports only one I/O standard, **IO2**. As a result of you changing the device selection, the I/O standard in the I/O tab changes to **IO2**. If you then reverted the device selection back to **Dev1**, the I/O standard does not change, because **IO2** is a legal I/O standard value for the device **Dev1**. The important point to note, is that the changing of device from **Dev1** to **Dev2** and back again, had the—potentially unintended—consequence of changing the I/O standard in the I/O tab.

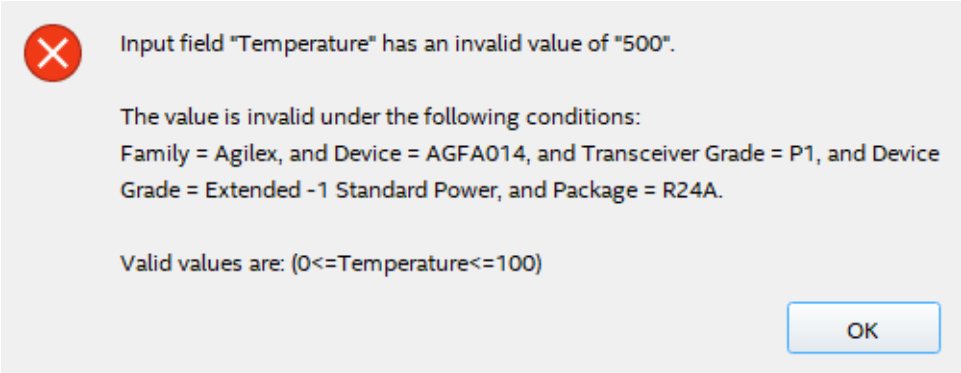
Note: In most cases, field dependencies are limited to the same tab, and often even within the same row. However, device, device grade, package and transceiver grade selection can have a much wider impact, as illustrated above. A simple way to verify that no unintended changes resulted from changing a device is to use the **File ➤ Save As** function to export the PTC state before and after the change in device selection. You can then compare the two .ptc files using a third-party *diff* utility to identify any fields that have changed.

3.4. Intel FPGA PTC Data Entry Error Messages

If the value you enter does not pass legality checks, or is inappropriate for the field, the system displays an error message.Typically the message may indicate the conditions under which a value is invalid, or specify a valid range of values.

Sample Error Message: Invalid Value

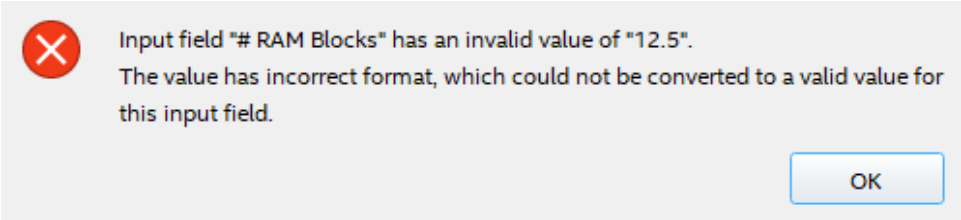
In this example you have entered a temperature that is outside the allowed range for a selected family, device, transceiver grade, device grade and package combination. The error message indicates the allowed range of 0 to 100. After you click OK, the field reverts to its previous value.



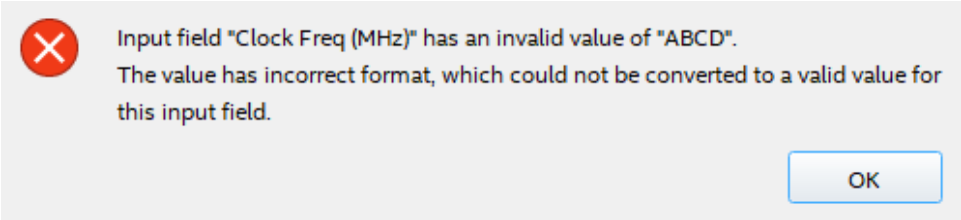
Sample Error Message: Incorrect Format

Many fields require a specific type of data. If the data you enter is not of the type required, an error message will appear.

For example, if an integer value is expected and you enter a fractional value, the resulting error message indicates that the entered value cannot be converted to a valid value for the input field. After you click OK, the field reverts to its previous value.



If a numerical value is expected and you enter a text value, the resulting error message indicates that the entered value cannot be converted to a valid value for the input field. After you click OK, the field reverts to its previous value.



4. Power and Thermal Calculator Tabs

The Intel FPGA Power and Thermal Calculator (PTC) is a tool within the Intel Quartus Prime software that allows you to enter information into tabs based on architectural features. The PTC then reports, in watts, subtotals of the power consumed by each architectural feature.

For more information about each architectural feature refer to the respective tab descriptions.

4.1. Intel FPGA PTC - Power Summary

The **Power Summary** tile of the Intel FPGA Power and Thermal Calculator (PTC) can be displayed at all times, and shows the calculated power consumption by resource type.

The values displayed in the **Power Summary** update in real time, as you change parameters on the data entry tabs.

In addition to displaying total power consumption, the **Power Summary** displays power consumption values for the following resource types:

- AIB: Advanced Interface Bus.
- Clock Network: The various clocks driving the synchronous portions of a design.
- Combinational Cell: The combinational logic in a design.
- Configuration RAM: The static RAM that configures an FPGA.
- DSP: Specialized blocks optimized for fast math operations.
- eSRAM: Additional memory available to the user.
- HBM: High-bandwidth memory.
- HPS: The hard-processor subsystem: a dedicated CPU integrated into the FPGA.
- HSSI Analog: The analog components of the FPGA's high-speed transceiver blocks.
- HSSI Digital: The digital components of the FPGA's high-speed transceiver blocks.
- I/O Analog: Power dissipated in the analog domain of the I/O subsystem, for example, I/O buffers.
- I/O Digital: Power dissipated in the digital domain of the I/O subsystem including GPIO, EMIF controller and SerDes controller.
- Memory LABs: Portions of logic modules configured as small memory blocks.
- Miscellaneous: Any power that doesn't fit into any of the other categories.
- PLL: Converts the fixed external clock to one or more high-speed on-chip clocks that drive synchronous portions of the design.
- RAM: Specialized blocks optimized for data storage and retrieval.

Intel Corporation. All rights reserved. Agilex, Altera, Arria, Cyclone, Enpirion, Intel, the Intel logo, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.
*Other names and brands may be claimed as the property of others.

ISO 9001:2015 Registered

- Register Cell: The synchronous portions of a logic module.
- Routing: The wires on the chip and all of their drivers and interconnects.
- Static Power: The power that the configured device consumes when powered up but with no user clocks operating.

4.2. Intel FPGA PTC - Common Tab Elements

The Intel FPGA Power and Thermal Calculator (PTC) is divided into multiple tabs, each allowing entry of a subset of FPGA resources. Some elements are common to more than one tab.

Total Thermal Power

The Total Thermal Power field estimates the total thermal power consumed by all FPGA resources in the specific tab. Some tabs may also provide a breakdown of the components contributing to the total thermal power. The total thermal power displayed in individual tabs does not include static power, which is reported in the Power Summary for the whole device.

Resource Utilization

Most tabs contain one or more fields that provide an estimate of the percentage resource utilization for the modules in the specific tab. Such values are calculated based on the maximum available resources of a given type for a selected device. If resource utilization exceeds 100%, it indicates that the current device may not be able to support the resources entered into the tab.

Power Rail Current Consumption

Most tabs include a table showing the dynamic current consumption for all power rails used by the FPGA resources in the specific tab. The same power rail may appear in multiple tabs, and the dynamic currents reported in the **Report** tab are the sums of all corresponding currents for a given rail at a given voltage in individual tabs. The **Report** tab also includes static currents, which are not reported in individual tabs.

4.3. Intel FPGA PTC - Device Selection and Thermal Analysis Tabs

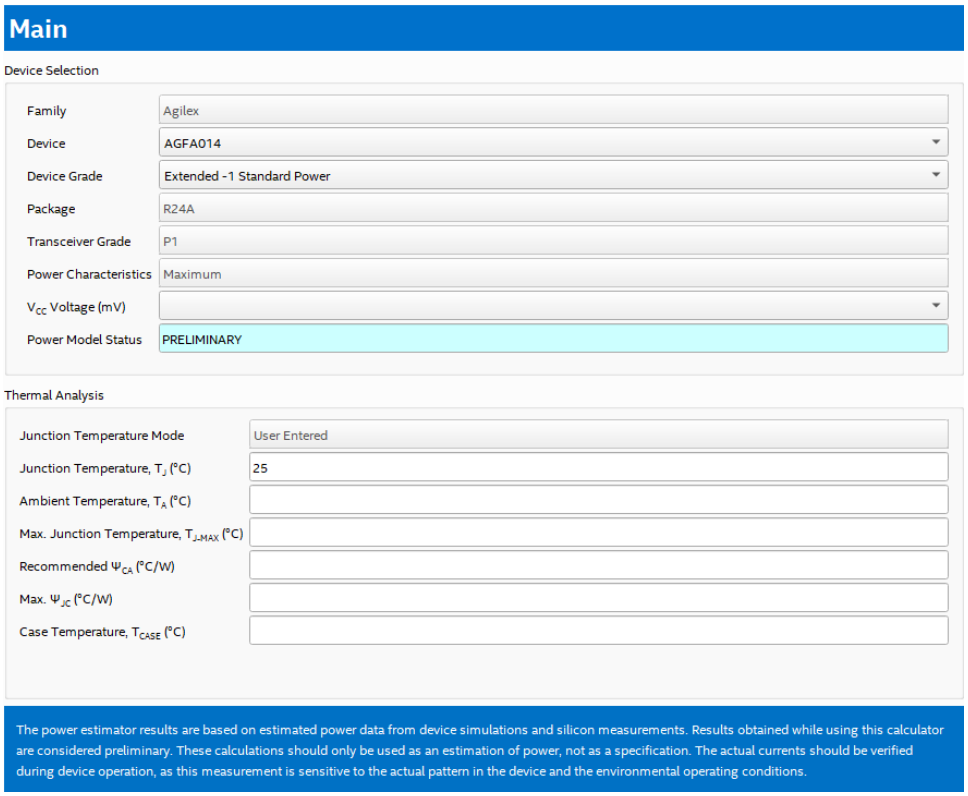
The **Device Selection** and **Thermal Analysis** tabs contain the same fields as the **Main** tab.

The **Device Selection** and **Thermal Analysis** tabs can be displayed at all times, allowing you to modify device, package, and cooling information, and to view thermal analysis information, while working on a tab other than the **Main** tab.

4.4. Intel FPGA PTC - Main Tab

The Main tab of the Intel FPGA Power and Thermal Calculator (PTC) allows you to enter device, package, and cooling information, and displays thermal analysis information.

Figure 4. Intel FPGA PTC Main Tab



The required parameters depend on whether the junction temperature is manually entered or auto computed.

Table 3. Device Selection Parameters

Parameter	Description
Family	Select the device family.
Device	Select your device. Larger devices consume more static power and have higher clock dynamic power. All other power components are unaffected by device selection.
Device Grade	Select the combination of Operating Temperature, Speed Grade, and Power Option used. Refer to the device datasheet for available combinations.
Package	Select the device package. Larger packages provide a larger cooling surface and more contact points to the circuit board, thus they offer lower thermal resistance. Package selection does not affect dynamic power directly.
Transceiver Grade	Select the transceiver grade. *Note:* For information on transceiver grades, refer to *Intel Agilex Device Variants and Packages*, in the *Intel Agilex Device Overview*.
Power Model Status	Indicates whether the power model for the device is in advance, preliminary, or final status.

The Thermal Analysis Summary section displays the junction temperature (T_J) and other thermal parameters, depending on the thermal analysis mode.

Table 4. Thermal Analysis Summary

Column Heading	Description
Junction Temp Mode	Select whether you provide the junction temperature, or whether detailed thermal analysis should be performed to determine junction temperature. In user-entered mode, the junction temperatures for all dies in the package are assumed to have one value, which you provide. When using a detailed thermal model, temperatures of different dies may be different, depending on the characteristics of a specific design. *Tip:* For faster responsiveness from the system, you should leave this value as **User Entered** until you are ready to perform detailed thermal analysis. *Note:* In version 19.4, only **User Entered** mode is supported for Intel Agilex devices. The detailed thermal model will be supported in a future release.
Junction Temp, T_J (°C)	Specify the junction temperature for all dies in the package. *Note:* This field is applicable only when the selected **Junction Temp Mode** value is **User Entered**.
Ambient Temp, T_A (°C)	Specifies the temperature of the air that is cooling the device. *Note:* This field is applicable only when the selected **Junction Temp Mode** value is **Detailed Thermal Model**.
Max. Junction Temp $T_{J\text{-}MAX}$ (°C)	Specifies the maximum junction temperature that no part of any die in the package should exceed. *Note:* This field is applicable only when the selected **Junction Temp Mode** value is **Detailed Thermal Model**.
Recommended ψ_{CA}(°C/W)	ψ_{CA} is the thermal resistance between the center of the package integrated heat spreader (IHS) and ambient temperature. The recommended Ψ_{CA} is the highest possible thermal resistance of the cooling solution that ensures no part of any die exceeds the specified maximum junction temperature. *Note:* This field is applicable only when the selected **Junction Temp Mode** value is **Detailed Thermal Model**.
Max. ψ_{JC}(°C/W)	ψ_{JC} is the thermal resistance between each of the dies in the package and the center of the package integrated heat spreader. This field shows the maximum Ψ_{JC} among all die, assuming the recommended Ψ_{CA} value above. *Note:* This field is applicable only when the selected **Junction Temp Mode** value is **Detailed Thermal Model**.
Case Temperature T_{CASE} (°C)	The case temperature, which is the temperature at the top center of the integrated heat spreader, assuming the recommended Ψ_{CA} value listed above. *Note:* This field is applicable only when the selected **Junction Temp Mode** value is **Detailed Thermal Model**.

You can directly enter or automatically compute junction temperatures based on the information provided. To enter the junction temperature, select **User Entered** in the **Junction Temp Mode** field, then enter the desired junction temperature in the **User-Entered Junction Temp T_J (°C)** field in the **Thermal Analysis Summary** section. In this mode, the junction temperatures for all dies in the package are assumed to have the specified value. To automatically compute junction temperatures, select **Detailed Thermal Model** in the same field.

Thermal power is the power dissipated in the device. Total thermal power is the sum of the thermal power of all the resources used in the device, including dynamic power. Total thermal power includes only the thermal component for the I/O tab and does not include external power dissipation, such as from voltage-referenced termination resistors.

The static power (P_{STATIC}) is the thermal power dissipated on the chip, independent of design activity. P_{STATIC} includes the static power from all FPGA functional blocks. P_{STATIC} is the only thermal power component that varies with junction temperature and power characteristics (process). P_{STATIC} is also the only thermal power component that varies significantly with selected device.

4.5. Intel FPGA PTC - Logic Tab

The Logic tab of the Intel FPGA Power and Thermal Calculator (PTC) allows you to enter logic resources for all modules in your design.

Figure 5. Logic Tab of the Power and Thermal Calculator

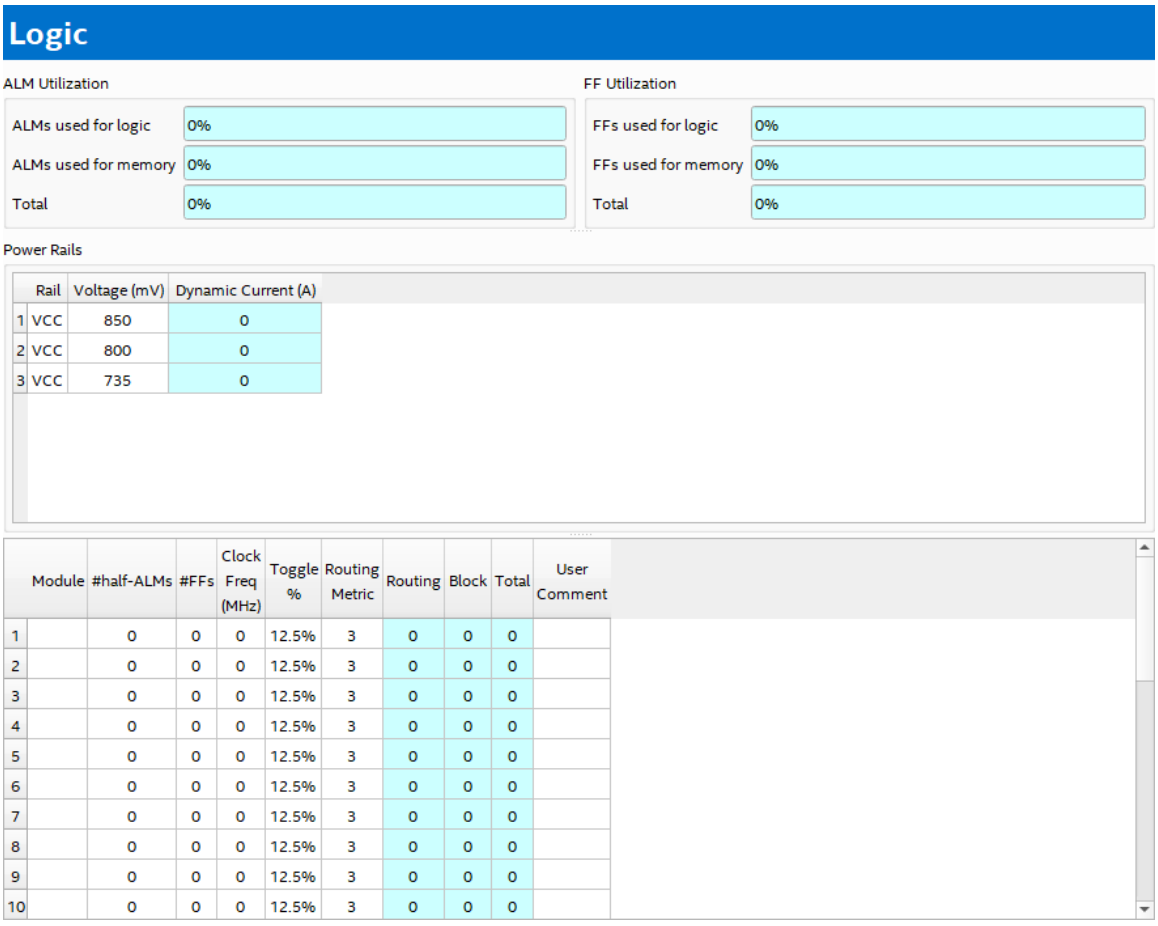


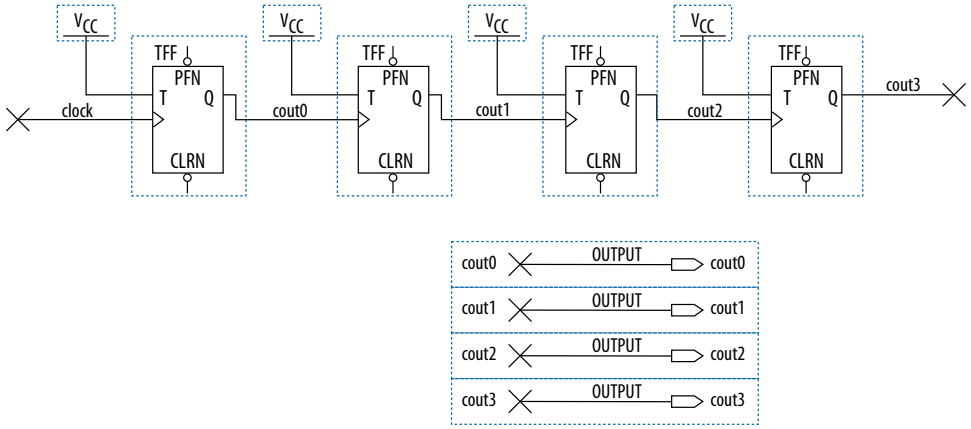
Table 5. Logic Tab Information

Input Parameter	Description
Module	Specify a name for each module of the design. This is an optional entry.
#Half ALMs	Enter twice the number of Adaptive Logic Modules (ALMs) used in your design, which you can find in the Compilation Report, by selecting **Fitter ➤ Place Stage ➤ Resource Usage Summary**. For power estimation purposes, the number of ALMs used in your design is the sum of the following values in the Compilation Report: • ALMs used for LUT logic and register circuitry • ALMs used for LUT logic • ALMs used for register circuitry • ALMs adjustment for power estimation The adjustment for power estimation is necessary because some unused ALMs may still consume power due to Fitter optimizations.
# FFs	Enter the number of **Primary logic registers**, plus **Secondary logic registers**, plus the number of registers reported as **Register control circuitry for power estimation**, all of which you can find in the Compilation Report, by selecting **Fitter ➤ Place Stage ➤ Resource Usage Summary**. The **Register control circuitry for power estimation** adjustment is necessary because some unused registers may still consume power due to fitter optimizations. Clock routing power associated with flipflops is calculated separately on the Clock tab of the PTC.
Clock Freq (MHz)	Enter a clock frequency (in MHz). This value is limited by the maximum frequency specification for the device family.
Toggle %	Enter the average percentage of clock cycles when the block output signals change values. Toggle percentage is multiplied by clock frequency to determine the number of transitions per second. For example, 100 MHz frequency with a 12.5% toggle rate, means that each LUT or flipflop output toggles 12.5 million times per second (100MHz × 12.5%). The toggle percentage ranges from 0 to 100%. Typically, the toggle percentage is 12.5%, which is the toggle percentage of a 16-bit counter. Most logic only toggles infrequently; therefore, toggle rates of less than 50% are more realistic. To ensure you do not underestimate the toggle percentage, use a realistic toggle percentage obtained through simulation. For example, a T flipflop (TFF) with its input tied to VCC has a toggle rate of 100% because its output is changing logic state on every clock cycle. Refer to the 4-Bit Counter Example below for a more detailed analysis. For any rows containing flipflops, toggle percentage cannot exceed 100%. A small portion of ALMs in a design may experience glitching that results in toggle percentage exceeding 100% for such ALMs. Enter such ALMs into a separate row with # FFs set to 0.
Routing Metric	Indicates the extent of the routing power of the outputs. Characteristics that have a large power impact and are captured by this factor include the following: • The fanout of the outputs • The number of routing resources used • The relative power usage of the different types of routing resources used The default value for this field is typical; the actual value varies between blocks in your design, and depends on the placement of your design. For most accurate results, you should import this value from the Intel Quartus Prime software after compiling your design, because the Intel Quartus Prime software has access to detailed placement and routing information. In the absence of an Intel Quartus Prime design, higher values generally correspond to signals that span large distances on the FPGA and fanout to many destinations, while lower values correspond to more localized signals. You can change this field from its default value to explore possible variations in power consumption depending on block placement. When changing this value, keep in mind that typical designs rarely use extreme values, and only for a small subset of the design.

continued...

Input Parameter	Description
Routing	Indicates the power dissipation due to estimated routing (in W). Routing power depends on placement and routing, which is a function of design complexity. The values shown are representative of routing power based on observed behavior across more than 100 real-world designs. Use the Intel Quartus Prime Power Analyzer for accurate analysis based on the exact routing used in your design.
Block	Indicates the power dissipation due to internal toggling of the ALMs and registers (in W). Logic block power is a combination of the function implemented and the relative toggle rates of the various inputs. The PTC uses an estimate based on observed behavior across more than 100 real-world designs. Use the Intel Quartus Prime Power Analyzer for accurate analysis based on the exact synthesis of your design.
Total	Indicates the estimated power (in W), based on information entered into the PTC. It is equal to the sum of routing power and block power.
User Comment	Enter any comments. This is an optional entry.

Figure 6. 4-Bit Counter Example



The `cout0` output of the first TFF has a toggle percentage of 100% because the signal toggles on every clock cycle. The toggle percentage for the `cout1` output of the second TFF is 50% because the output toggles every two clock cycles. Similarly, the toggle percentage for the `cout2` and `cout3` outputs are 25% and 12.5%, respectively. Therefore, the average toggle percentage for this 4-bit counter is (100 + 50 + 25 + 12.5)/4 = 46.875%.

For more information about logic block configurations, refer to the Intel Agilex Logic Array Blocks and Adaptive Logic Modules User Guide.

4.6. Intel FPGA PTC - RAM Tab

Each row in the RAM tab of the Intel FPGA Power and Thermal Calculator (PTC) represents a design module with RAM blocks of the same type, same data width, same RAM depth (if applicable), same RAM mode, and the same port parameters.

Each row in the RAM tab of the PTC represents a logical RAM module that you can implement using one or more physical RAM blocks. The PTC implements each logical RAM module with the minimum number of physical RAM blocks, in the most power-efficient way possible, based on the specified logical width and depth.

You must know how your RAM is implemented by the Intel Quartus Prime Compiler when you are selecting the RAM block mode. For example, if a ROM is implemented with two ports, it is considered a true dual-port memory and not a ROM. Single-port and ROM implementations use only one port. Simple dual-port and true dual-port implementations use both Port A and Port B.

Note:

- The Power and Thermal Calculator reports MLAB power in the RAM tab as described above, as well as in the *Power Summary* table.
- In the *Power Summary* table, the MLAB power is spread across four categories: Memory LAB, Miscellaneous, Register and Routing; this is done to be consistent with the reporting provided in the Intel Quartus Prime Power Analyzer.

Figure 7. RAM Tab of the Power and Thermal Calculator

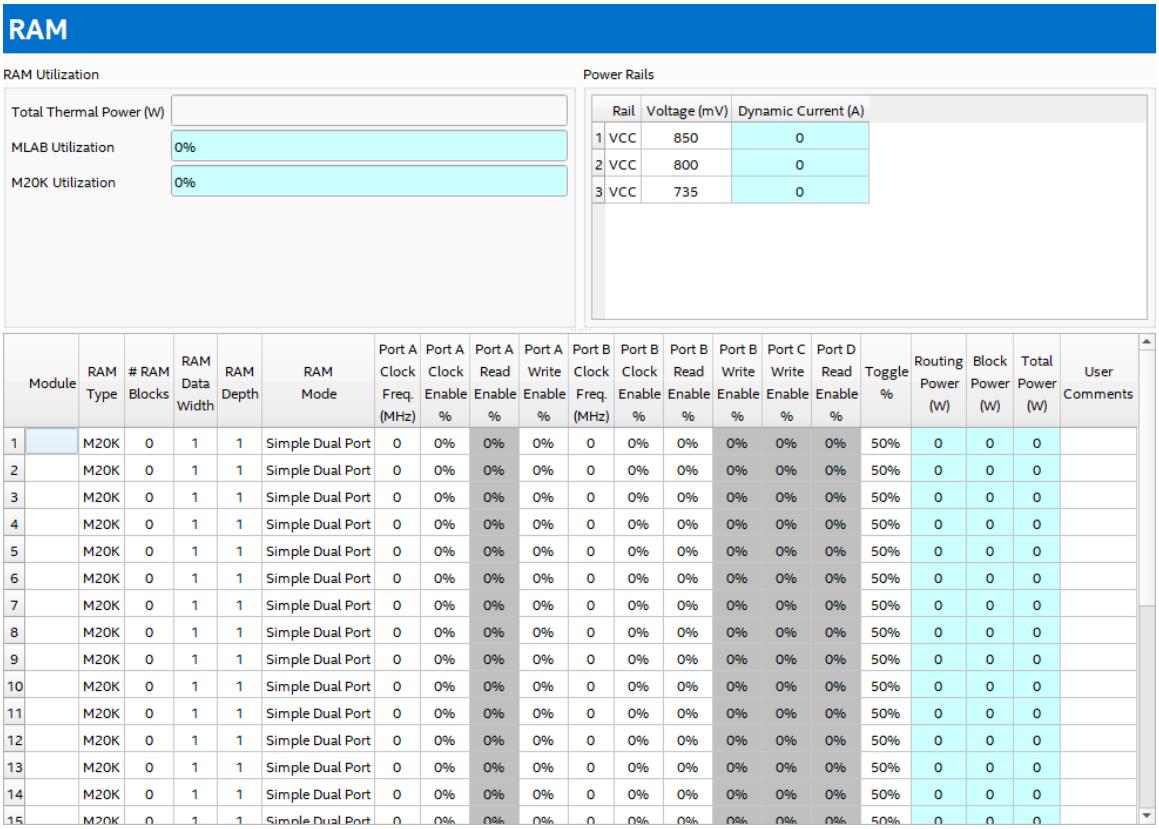


Table 6. RAM Tab Information

Column Heading	Description
Module	Enter a name for the RAM module in this row. This is an optional value.
RAM Type	Select the implemented RAM type.

continued...

Column Heading	Description
	You can find the RAM type in the *Type* column of the Intel Quartus Prime Compilation Report. In the Compilation Report, select **Fitter ➤ Place Stage ➤ Fitter RAM Summary**.
# RAM Blocks	Enter the number of RAM blocks in the module that use the same memory type and mode and have the same port parameters. The parameters for each port are as follows: • Clock frequency in MHz • Percentage of time the RAM is enabled • Percentage of time the port is writing as opposed to reading You can find the number of RAM blocks in either the *MLAB cells* or *M20K blocks* column of the Intel Quartus Prime Compilation Report. In the Compilation Report, select **Fitter ➤ Place Stage ➤ Fitter RAM Summary**. *Note:* The value entered into this field represents the number of logical memory blocks. Depending on the specified memory depth and data width, more than one physical memory block may be required to implement one logical block. The Power and Thermal Calculator calculates the number of physical memory blocks based on the specified memory depth and data width, such that the minimum number of physical blocks is used, and assuming the most power efficient physical configuration.
RAM Data Width	Enter the width of the data for the RAM block. This value is limited based on the RAM type. You can find the width of the RAM block in the *Port A Width* or the *Port B Width* column of the Intel Quartus Prime Compilation Report. In the Compilation Report, select **Fitter ➤ Place Stage ➤ Fitter RAM Summary**. For RAM blocks that have different widths for Port A and Port B, use the larger of the two widths.
RAM Depth	Enter the depth of the RAM block in number of words. You can find the depth of the RAM block in the *Port A Depth* or the *Port B Depth* column of the Intel Quartus Prime Compilation Report. In the Compilation Report, select **Fitter ➤ Place Stage ➤ Fitter RAM Summary**.
RAM Mode	For MLAB and eSRAM RAM types, this field has only one possible value: Simple Dual Port. For M20K RAM type, select from the following modes: • Simple Dual Port • True Dual Port • Simple Dual Port with ECC • ROM • Simple Quad Port The mode is based on how the Intel Quartus Prime Compiler implements the RAM. If you are unsure how your memory module is implemented, you can compile a test case in the required configuration in the Intel Quartus Prime software. You can find the RAM mode in the *Mode* column of the Intel Quartus Prime Compilation Report. In the Compilation Report, select **Fitter ➤ Place Stage ➤ Fitter RAM Summary**. A single-port RAM has one port with a read and a write control signal. A simple dual-port RAM has one read port and one write port. A true dual-port RAM has two ports, each with a read and a write control signal. ROMs are read-only single-port RAMs. A simple quad-port RAM has a total of four ports, two read ports and two write ports.
Port A - Clock Freq (MHz)	Enter the clock frequency for Port A of the RAM blocks (in MHz). This value is limited by the maximum frequency specification for the RAM type and device family.
Port A - Clock Enable %	The average percentage of time the Port A clock enable is active, regardless of activity on RAM data and address inputs. This number must be a percentage between 0% and 100%. RAM power is consumed primarily when a clock event occurs. Using a clock enable signal to disable a port when no read or write operation is occurring can result in significant power savings.
Port A - Read Enable %	Enter the percentage of time Port A of the RAM block is in read mode. This field is applicable only for true dual port RAMs.

continued...

Column Heading	Description
	This value must be a percentage number between 0 and 100%.
Port A - Write Enable %	Enter the average percentage of time Port A of the RAM block is in write mode. This field applies only for dual port, true dual port, and quad port RAMs. This value must be a percentage number between 0 and 100%.
Port B - Clock Freq (MHz)	Enter the clock frequency for Port B of the RAM blocks (in MHz).
Port B - Clock Enable %	Enter the average percentage of time the input clock enable for Port B is active, regardless of the activity on the RAM data and address inputs. The enable percentage ranges from 0 to 100%. RAM power is consumed primarily when a clock event occurs. Using a clock-enable signal to disable a port when no read or write operation is occurring can result in significant power savings.
Port B - Read Enable %	Enter the percentage of time Port B of the RAM block is in read mode. This field is applicable only to dual port, true dual port, and quad port RAMs and ROMs. This value must be a percentage number between 0 and 100%.
Port B - Write Enable %	Enter the percentage of time Port B of the RAM block is in write mode. This field is available only for true dual-port mode. This value must be a percentage number between 0 and 100%.
Port C - Write Enable %	Enter the percentage of time the RAM block is writing to this port. In Simple Quad-Port Mode, clock and clock enable for all parts are shared and the same as Port A. This value must be a percentage number between 0 and 100%.
Port D - Read Enable %	Enter the percentage of time the RAM block is reading on this port. In Simple Quad-Port Mode, clock and clock enable for all parts are shared and the same as Port A. This value must be a percentage number between 0 and 100%.
Toggle %	The percentage of clock cycles when the block output signal changes value. This value is multiplied by the clock frequency and the enable percentage to determine the number of transitions per second. This value affects only routing power. 50% corresponds to a randomly changing signal, since half the time the signal holds the same value and thus not transition. This is considered the highest meaningful toggle rate for a RAM block.
Routing Power (W)	Indicates the power dissipation due to estimated routing (in W). Routing power depends on placement and routing, which is a function of design complexity. The values shown represent the routing power estimate based on observed behavior across more than 100 real-world designs. Use the Intel Quartus Prime Power Analyzer for accurate analysis based on the exact routing used in your design.
Block Power (W)	Indicates the power dissipation due to internal toggling of the RAM (in W). Use the Intel Quartus Prime Power Analyzer for accurate analysis based on the exact RAM modes in your design.
Total Power (W)	Indicates the estimated power (in W), based on information entered into the PTC. Total power is equal to the sum of routing power and block power.
User Comments	Enter any comments. This is an optional entry.

4.7. Intel FPGA PTC - DSP Tab

Each row in the DSP tab of the Intel FPGA Power and Thermal Calculator (PTC) represents a DSP design module where all instances have the same configuration, clock frequency, toggle percentage, and register usage.

Figure 8. DSP Tab of the Power and Thermal Calculator

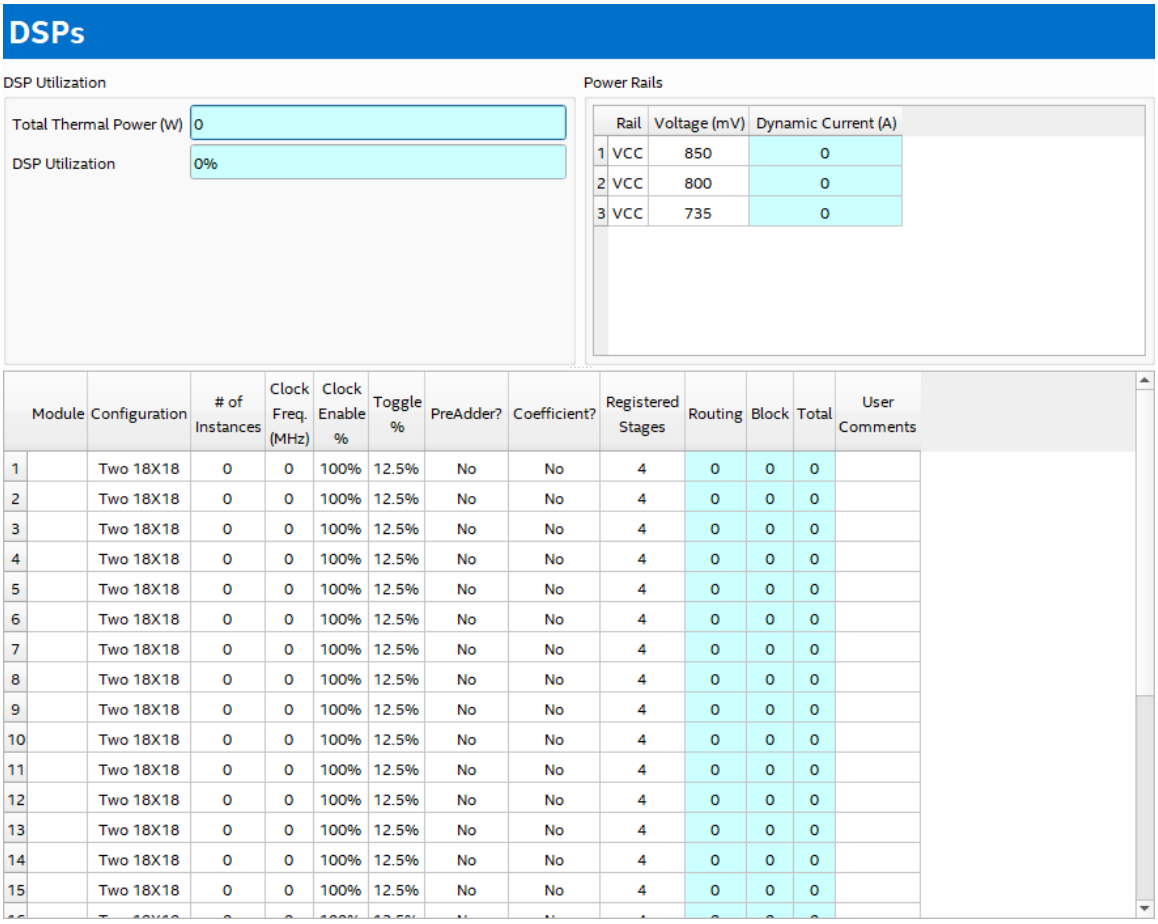


Table 7. DSP Tab Information

Column Heading	Description
Module	Enter a name for the DSP module in this column. This is an optional value.
Configuration	Select the DSP block configuration for the module.
# of Instances	Enter the number of DSP block instances that have the same configuration, clock frequency, toggle percentage, and register usage. This value is not necessarily equal to the number of dedicated DSP blocks you use. For example, it is possible to use two 18 × 18 simple multipliers that are implemented in the same DSP block in the FPGA devices. In this case, the number of instances would be two. To determine the maximum number of instances you can fit in the device for any particular mode, follow these steps: 1. Open the "Variable Precision DSP Blocks" chapter of the Intel Agilex Device Handbook. 2. In the "Number of DSP Blocks" table, take the maximum number of DSP blocks available in the device for the mode of operation. 3. Divide the maximum number by the "# of Mults" for that mode of operation from the "DSP Block Operation Modes" table. The resulting value is the maximum number of instances supported by the device.
Clock Freq (MHz)	Enter the clock frequency for the module (in MHz). This value is limited by the maximum frequency specification for the device family.

continued...

Column Heading	Description
Clock Enable %	Specifies the percentage of time that the DSP block is enabled.
Toggle %	Enter the average percentage of DSP data outputs toggling on each clock cycle. The toggle percentage ranges from 0 to 50%. The default value is 12.5%. For a more conservative power estimate, use a higher toggle percentage. 50% corresponds to a randomly changing signal, since half the time the signal holds the same value and thus not transition. This is considered the highest meaningful toggle rate for a DSP block.
Preadder?	Select **Yes** if the PreAdder function of the DSP block is turned on.
Coefficient?	Select **Yes** if the Coefficient function of the DSP block is turned on.
Registered Stages	Select number of the registered stages. Permitted values depend on the selected mode; some modes, such as floating-point multiply and accumulate cannot have 0 register stages.. • 0—None • 1—Input • 2—Input and Output • 3—Input, Output, and Multiplier • 4— Input, Output, Multiplier, and Pipeline Stage 2 • 5—Input, Output, Multiplier, Pipeline Stage 2, and Floating-Point Adder
Routing	Indicates the power dissipation due to estimated routing (in W). Routing power depends on placement and routing, which is a function of design complexity. The values shown represent the routing power estimate based on observed behavior across more than 100 real-world designs.
Block	Indicates the estimated power consumed by the DSP blocks (in W).
Total	Indicates the estimated power (in W), based on information entered into the PTC. It is the total power consumed by the DSP blocks and is equal to the routing power and block power.
User Comments	Enter any comments. This is an optional entry.

4.8. Intel FPGA PTC - Clock Tab

Each row in the Clock tab of the Intel FPGA Power and Thermal Calculator (PTC) represents a clock network or a separate clock domain.

Intel Agilex devices support global, regional, and periphery clock networks. The PTC does not distinguish between global or regional clocks because the difference in power is not significant.

Figure 9. Clock Tab of the Power and Thermal Calculator

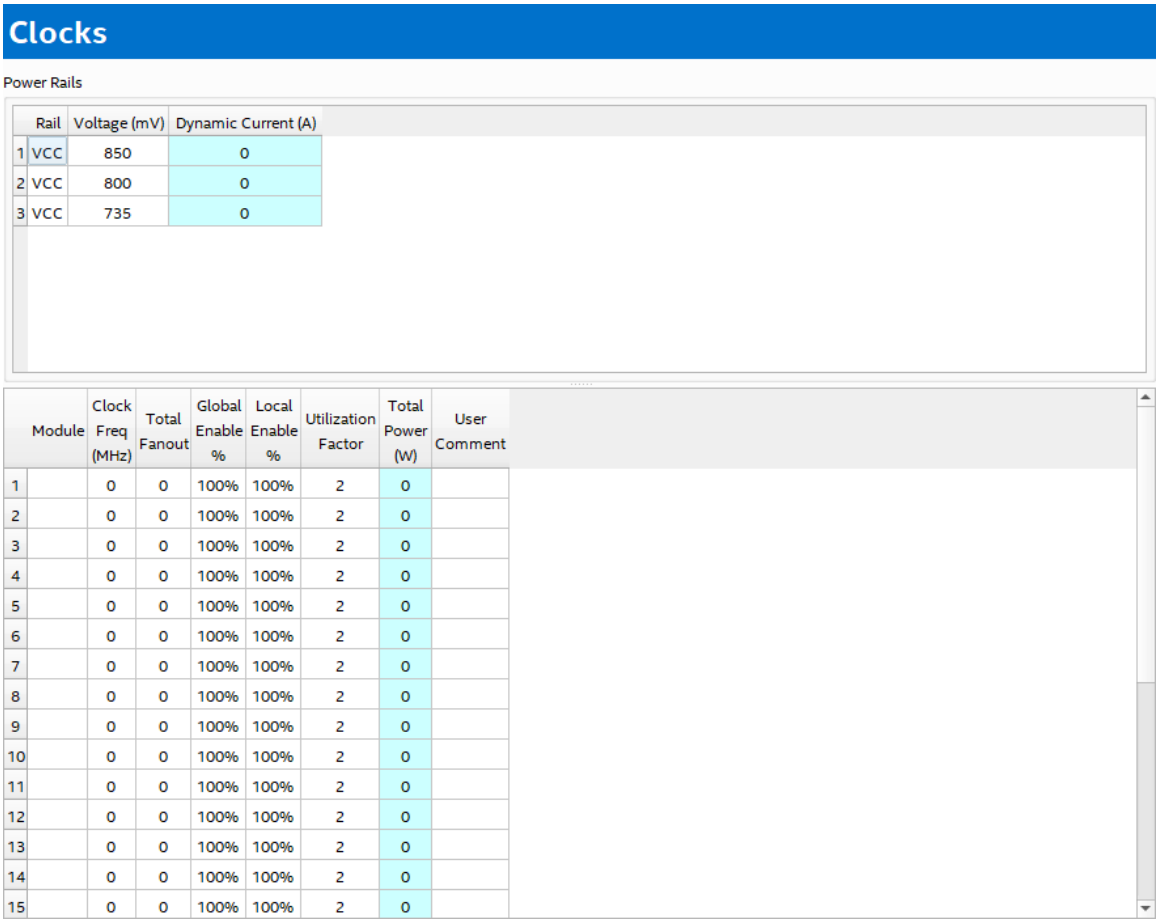


Table 8. Clock Tab Information

Column Heading	Description
Module	Enter a name for the clock domain in this column. This is an optional value.
Clock Freq (MHz)	Enter the frequency of the clock domain. This value is limited by the maximum frequency specification for the device family. *Note:* When you import a design from the Intel Quartus Prime software, some imported clocks may have a frequency of 0 MHz, due to either of the following reasons: • The Intel Quartus Prime software did not have sufficient information to determine clock frequency due to incomplete clock constraints. • Clock resources were used to route a reset signal, which toggles infrequently, so its frequency is reported as 0 MHz.
Total Fanout	Enter the total number of flipflops, hyper-registers, RAMs, digital signal processing (DSP) blocks, and I/O pins fed by this clock. Power consumed by MLAB clocks is accounted for in the RAM tab; therefore, clock fanout on this tab does not include any MLABs driven by this clock domain. The number of resources driven by every global clock and regional clock signal is reported in the *Fan-out* column of the Intel Quartus Prime Compilation Report. In the Compilation Report, select **Fitter** and click **Place Stage**. Select **Global & Other Fast Signals Summary** and observe the *Fan-out* value.

continued...

Column Heading	Description
Global Enable %	Enter the average percentage of time that the entire clock tree is enabled. Each global clock buffer has an enable signal that you can use to dynamically shut down the entire clock tree.
Local Enable %	Enter the average percentage of time that clock enable is high for destination flipflops. Local clock enables for flipflops in ALMs are promoted to LAB-wide signals. When a given flipflop is disabled, the LAB-wide clock is disabled, cutting clock power and the power for down-stream logic. This tab models only the impact on clock tree power.
Utilization Factor	Represents the impact of the clock network configuration on power. Characteristics that have a large impact on power and are captured by this factor include the following: • Whether the network is widely spread out • Whether the fanout is small or large • The clock settings within each LAB The default value for this field is typical; the actual value varies between clocks in your design, and depends on the placement of your design. For most accurate results, you should import this value from the Intel Quartus Prime software after compiling your design, because the Intel Quartus Prime software has access to detailed placement information. In the absence of an Intel Quartus Prime design, higher values generally correspond to signals that span large distances on the FPGA and fanout to many destinations, while lower values correspond to more localized signals. You can change this field from its default value to explore possible variations in power consumption depending on block placement. When changing this value, keep in mind that typical designs rarely use extreme values, and only for a small subset of the design.
Total Power (W)	Indicates the total power dissipation due to clock distribution (in W).
User Comments	Enter any comments. This is an optional entry.

For more information about the clock networks of Intel Agilex devices, refer to the Intel Agilex Clocking and PLL User Guide.

4.9. Intel FPGA PTC - PLL Tab

Each row in the PLL tab of the Intel FPGA Power and Thermal Calculator (PTC) represents one or more PLLs in the device.

For Intel Agilex devices, the supported PLL types are I/O bank IOPLL and fabric-feeding IOPLL.

Figure 10. PLL Tab of the Power and Thermal Calculator

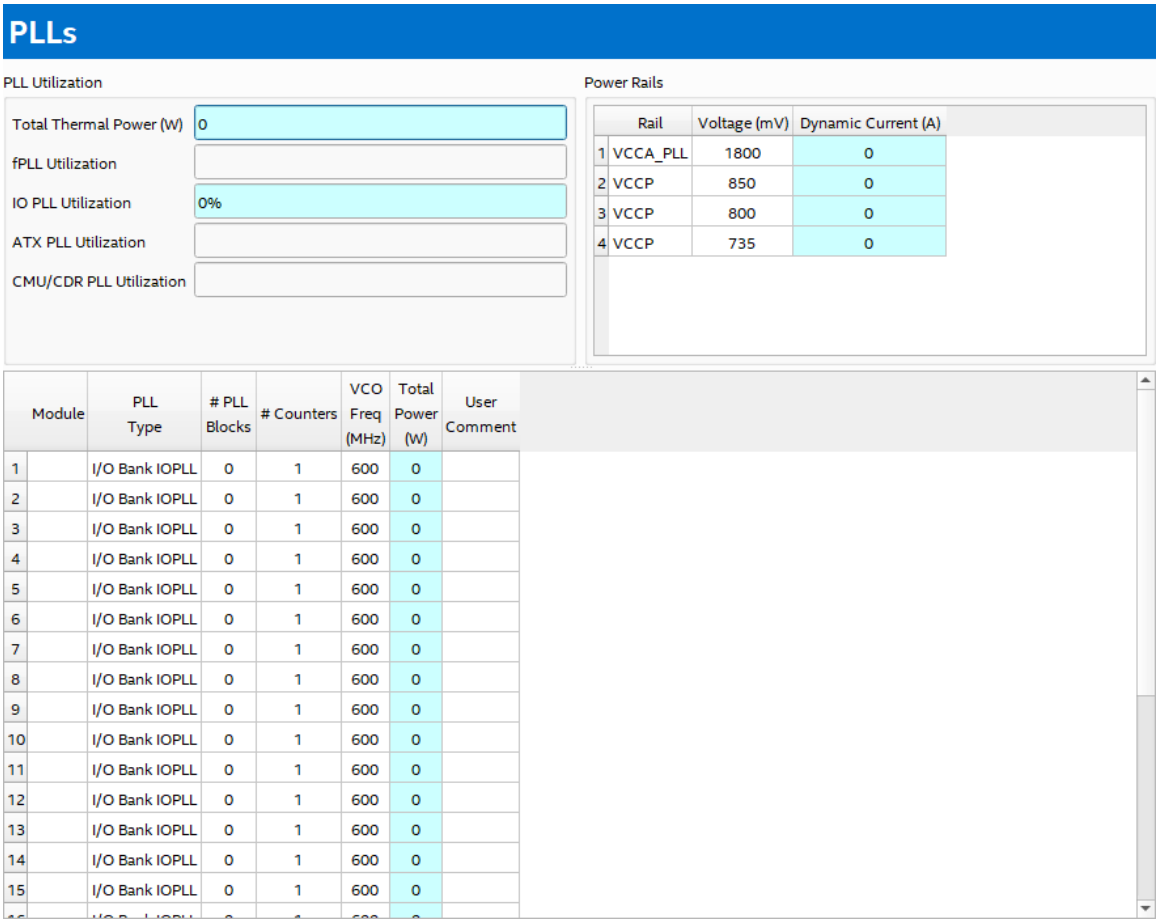


Table 9. PLL Tab Information

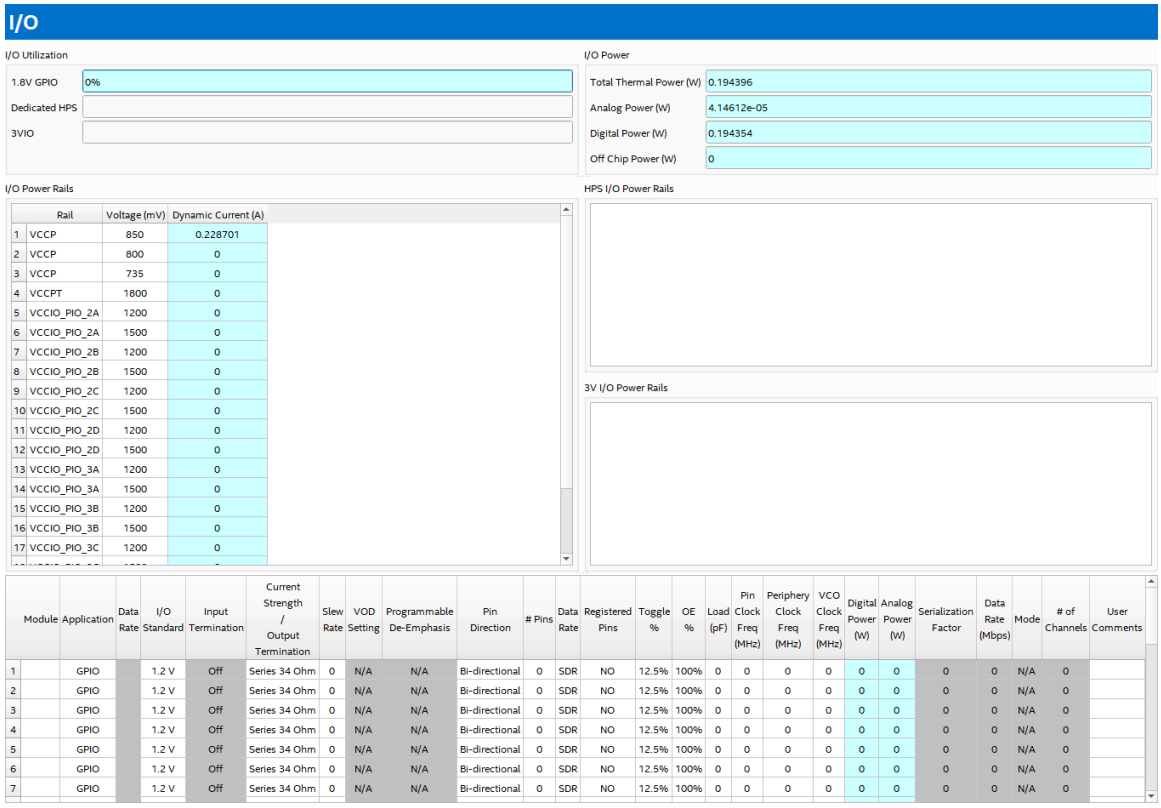
Column Heading	Description
Module	Specify a name for the PLL in this column. This is an optional value.
PLL Type	Specifies the type of PLL. Intel Agilex devices have I/O bank IOPLLs and fabric-feeding IOPLLs.
# PLL Blocks	Enter the number of PLL blocks with the same combination of parameters.
# Counters	Enter the number of counters of the PLL.
VCO Freq (MHz)	Specify the internal VCO operating frequency for PLLs.
Total Power (W)	Shows the total estimated power for this row (in W).
User Comments	Enter any comments. This is an optional entry.

For more information about the PLLs available in Intel Agilex devices, refer to the Intel Agilex Clocking and PLL User Guide.

4.10. Intel FPGA PTC - I/O Tab

Each row in the I/O tab of the Intel FPGA Power and Thermal Calculator (PTC) represents a design module where the I/O pins have the same I/O standard, input termination, current strength or output termination, data rate, clock frequency, output enable static probability, and capacitive load.

Figure 11. I/O Tab of the Power and Thermal Calculator



	Rail	Voltage (mV)	Dynamic Current (A)
1	VCCP	850	0.228701
2	VCCP	800	0
3	VCCP	735	0
4	VCCPT	1800	0
5	VCCIO_PIO_2A	1200	0
6	VCCIO_PIO_2A	1500	0
7	VCCIO_PIO_2B	1200	0
8	VCCIO_PIO_2B	1500	0
9	VCCIO_PIO_2C	1200	0
10	VCCIO_PIO_2C	1500	0
11	VCCIO_PIO_2D	1200	0
12	VCCIO_PIO_2D	1500	0
13	VCCIO_PIO_3A	1200	0
14	VCCIO_PIO_3A	1500	0
15	VCCIO_PIO_3B	1200	0
16	VCCIO_PIO_3B	1500	0
17	VCCIO_PIO_3C	1200	0

	Module	Application	Data Rate	I/O Standard	Input Termination	Current Strength / Output Termination	Slew Rate	VOD Setting	Programmable De-Emphasis	Pin Direction	# Pins	Data Rate	Registered Pins	Toggle %	OE %	Load (pF)	Pin Clock Freq (MHz)	Periphery Clock Freq (MHz)	VCO Clock Freq (MHz)	Digital Power (W)	Analog Power (W)	Serialization Factor	Data Rate (Mbps)	Mode	# of Channels	User Comments
1		GPIO		1.2 V	Off	Series 34 Ohm	0	N/A	N/A	Bi-directional	0	SDR	NO	12.5%	100%	0	0	0	0	0	0	0	0	N/A	0	
2		GPIO		1.2 V	Off	Series 34 Ohm	0	N/A	N/A	Bi-directional	0	SDR	NO	12.5%	100%	0	0	0	0	0	0	0	0	N/A	0	
3		GPIO		1.2 V	Off	Series 34 Ohm	0	N/A	N/A	Bi-directional	0	SDR	NO	12.5%	100%	0	0	0	0	0	0	0	0	N/A	0	
4		GPIO		1.2 V	Off	Series 34 Ohm	0	N/A	N/A	Bi-directional	0	SDR	NO	12.5%	100%	0	0	0	0	0	0	0	0	N/A	0	
5		GPIO		1.2 V	Off	Series 34 Ohm	0	N/A	N/A	Bi-directional	0	SDR	NO	12.5%	100%	0	0	0	0	0	0	0	0	N/A	0	
6		GPIO		1.2 V	Off	Series 34 Ohm	0	N/A	N/A	Bi-directional	0	SDR	NO	12.5%	100%	0	0	0	0	0	0	0	0	N/A	0	
7		GPIO		1.2 V	Off	Series 34 Ohm	0	N/A	N/A	Bi-directional	0	SDR	NO	12.5%	100%	0	0	0	0	0	0	0	0	N/A	0	

The Power and Thermal Calculator assumes that you are using external termination resistors as recommended for SSTL and high-speed transceiver logic HSTL. If your design does not use external termination resistors, choose the LVTTL/ LVCMOS I/O standard with the same VCCIO and similar current strength as the terminated I/O standard.

To use on-chip termination (OCT), select the **Current Strength/Output Termination** option in the PTC.

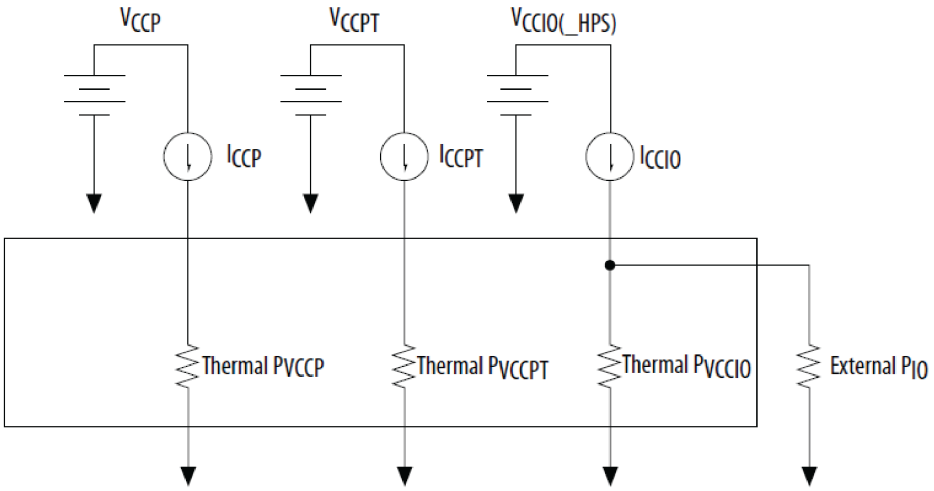
The power reported for the I/O signals includes thermal and external I/O power. The total thermal power is the sum of the thermal power consumed by the device from each power rail, as shown in the following equation.

Figure 12. Total Thermal Power

$$\text{thermal power} = \text{thermal } P_{VCCP} + \text{thermal } P_{VCCPT} + \text{thermal } P_{VCCIO}$$

The following figure shows the I/O power consumption. The I_{CCIO} power rail includes both the thermal P_{IO} and the external P_{IO}.

Figure 13. I/O Power Representation



The VREF pins consume minimal current (typically less than 10 µA), which is negligible when compared with the current consumed by the general purpose I/O (GPIO) pins; therefore, the PTC does not include the current for VREF pins in the calculations.

Table 10. I/O Tab Information

Column Heading	Description
Module	Specify a name for the I/O in this column. This is an optional value.
Application	Specify the application for this I/O row. GPIO and SerDes interfaces can be instantiated using this field. Use the I/O-IP tab to instantiate external memory interface (EMIF) interfaces.
Data Rate	Specifies the clock rate of PHY logic. Determines the clock frequency of PHY logic in relation to the memory clock frequency. For example, if the memory clock sent from the FPGA to the memory device is toggling at 800MHz, a quarter rate interface means that the PHY logic in the FPGA runs at 200MHz.
I/O Standard	Specifies the I/O standard used by the I/O pins in this module.
Input Termination	Specifies the input termination setting for the input and bidirectional pins in this module.
Current Strength/Output Termination	Specifies the current strength or output termination setting for the output and bidirectional pins in this module. Current strength and output termination are mutually exclusive.
Slew Rate	Specifies the slew rate setting for the output and bidirectional pins in this module. Using a lower slew rate setting helps reduce switching noise but may increase delay.
V_{OD} Setting	Specifies the differential output voltage (V_{OD}) for the output and bidirectional pins in the module. A smaller number indicates a smaller VOD which reduces static power.

continued...

Column Heading	Description
Programmable De-Emphasis	Specifies the de-emphasis setting for the output and bidirectional pins in this module. A smaller number indicates a smaller de-emphasis which reduces dynamic power.
Pin Direction	The pin's signal direction. Output, input, or bi-directional.
# Pins	Number of pins used in the specified configuration.
Data Rate	Indicates whether I/O value changes once (Single-Data Rate) or twice (Double-Data Rate) per cycle.
Registered Pin	Indicates whether the pin is registered or not.
Toggle %	Percentage of clock cycles when the I/O signal changes value. This value is multiplied by clock frequency to determine the number of transitions per second. If DDR is selected, the toggle rate is multiplied by an additional factor of two.
OE %	For modules with Input Termination set to **OFF**, enter the average percentage of time that: • Output I/O is enabled • Bidirectional I/O is an output and enabled During the remaining time: • Output I/O is tri-stated • Bidirectional I/O is an input Input Termination cannot be active while the Output I/O is enabled, so for modules with Input Termination not set to **OFF**, enter the average percentage of time that On-Chip Termination is inactive (that is, 1-percentage that the On-Chip Termination is active).This number must be a percentage between 0% and 100%.
Load (pF)	Specifies pin loading external to the chip (in pF). Applies only to outputs and bidirectional pins. Pin and package capacitance is already included in the I/O model. Include only off-chip capacitance.
Pin Clock Frequency (MHz)	Clock frequency (in MHz). 100 MHz with a 12.5% toggle percentage would mean that each I/O pin toggles 12.5 million times per second (100 MHz * 12.5%).
Periphery Clock Freq (MHz)	The I/O subsystem internal PHY clock frequency. This is an output-only field. In SerDes applications, the PHY clock frequency is a function of the SerDes rate and serialization factor. In external memory interface (EMIF) applications, the PHY clock frequency is a function of the memory clock frequency and DDR rate of the EMIF IP.
VCO Clock Freq (MHz)	The internal VCO operating frequency. This is an output-only field. In SerDes applications, VCO frequency is a function of SerDes Data rate. In external memory interface (EMIF) applications, the VCO frequency is a function of the memory clock frequency of the EMIF IP. The VCO frequency is not applicable in GPIO mode.
Digital Power (W)	Power dissipated in the digital domain of the I/O-subsystem including GPIO, EMIF controller and SerDes controller.
Analog Power (W)	Power dissipated in the analog domain of the I/O-subsystem, for example, I/O buffers.
Serialization Factor	Number of parallel data bits for each serial data bit. Used for SerDes-DPA.
Data Rate (Mbps)	The maximum data rate of the SerDes channels in Mbps.
Mode	The DPA mode in which the SerDes channels are operating.
# of Channels	The number of channels running at the data rate of this SerDes domain.
User Comments	Enter any comments. This is an optional entry.

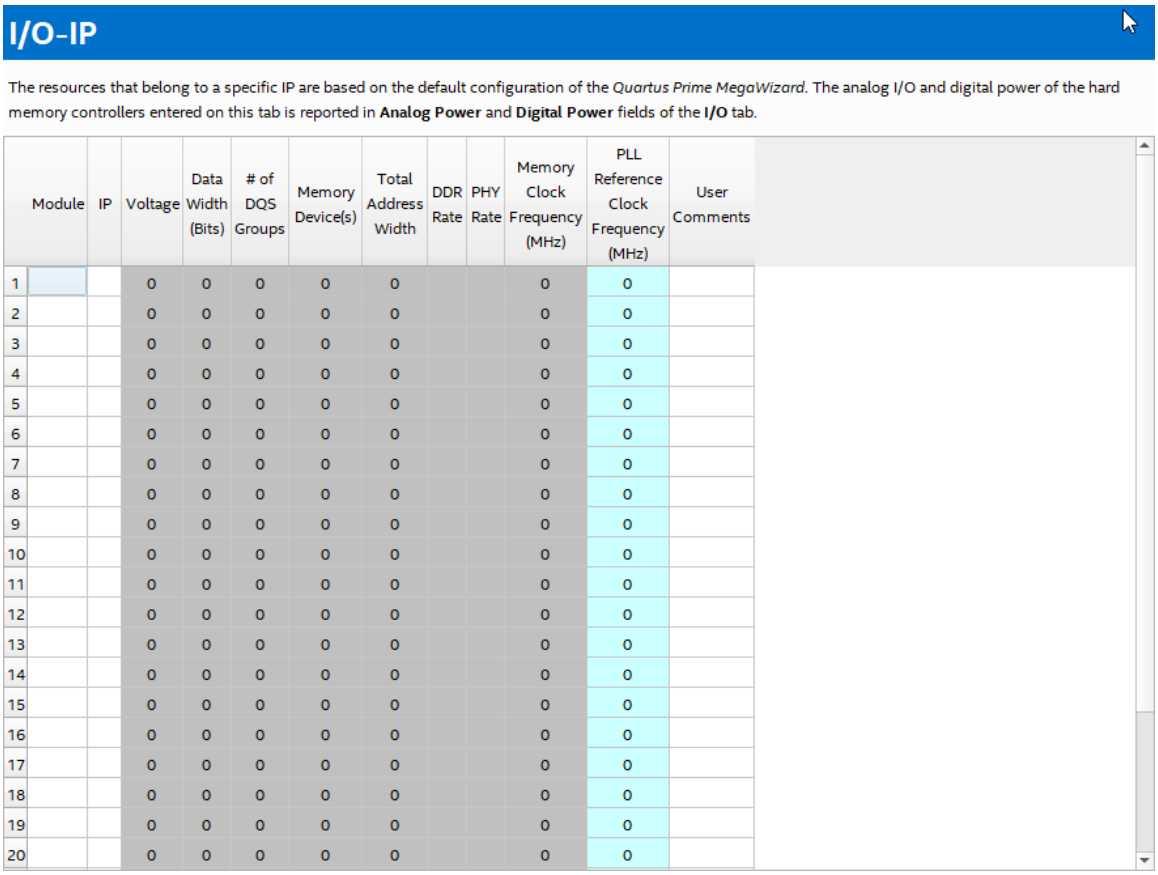
For more information about the I/O standard termination schemes, refer to *I/O and High Speed I/Os in Intel Agilex Devices*.

4.11. Intel FPGA PTC - I/O-IP Tab

Each row in the I/O-IP tab of the Intel FPGA Power and Thermal Calculator (PTC) represents a design module. You can use the I/O-IP tab to instantiate external memory interface and HPS IPs supported in Intel Agilex devices. The I/O-IP tab populates other PTC tabs with resources used by a selected IP.

Analog I/O power and digital power of hard memory controllers and HPS IPs entered on this tab are reported in the Analog Power and Digital Power fields of the I/O tab. If the IP uses other resource types (for example Logic or PLL), the power is reported on the corresponding tab.

Figure 14. I/O-IP Tab of the Power and Thermal Calculator



I/O-IP Tab Information

Column Heading	Description
Module	Specifies a name for the IP in this column. The module name depends on the selected IP type. It helps to cross-reference each IP module and its corresponding auto-populated entries on other tabs. This name is auto-populated when IP type is selected in the IP column and cannot be changed.
IP	Specifies the type of the IP in the design.
Voltage	Specifies the I/O voltage of the signaling between periphery device and interface.
Data Width (Bits)	Specifies the interface data width of the specific IP (in bits).
# of DQS Groups	Specifies the number of DQS groups.
Memory Device(s)	Specifies the number of memory devices connected to the interface.
Total Address Width	Specifies the total address width. This value is used to derive the total number of address pins required.
DDR Rate	Specifies the clock rate of user logic. Determines the clock frequency of user logic in relation to the memory clock frequency. For example, if the memory clock sent from the FPGA to the memory device is toggling at 800MHz, a "Quarter rate" interface means that the user logic in the FPGA runs at 200MHz.
PHY Rate	Specifies the clock rate of PHY logic. Determines the clock frequency of PHY logic in relation to the memory clock frequency. For example, if the memory clock sent from the FPGA to the memory device is toggling at 800MHz, a "Quarter rate" interface means that the PHY logic in the FPGA runs at 200MHz.
Memory Clock Frequency (MHz)	Specifies the frequency of memory clock (in MHz).
PLL Reference Clock Frequency (MHz)	Specifies the PLL Reference Clock Frequency (in MHz).
User Comments	Enter any comments. This is an optional entry.

4.12. Intel FPGA PTC - Transceiver Tab

The Transceiver tab of the Intel FPGA Power and Thermal Calculator (PTC) allows you to enter transceiver resources and their settings for all modules in your design. The power of transceiver I/O pins is included on this tab.

Figure 15. Transceiver tab of the Power and Thermal Calculator

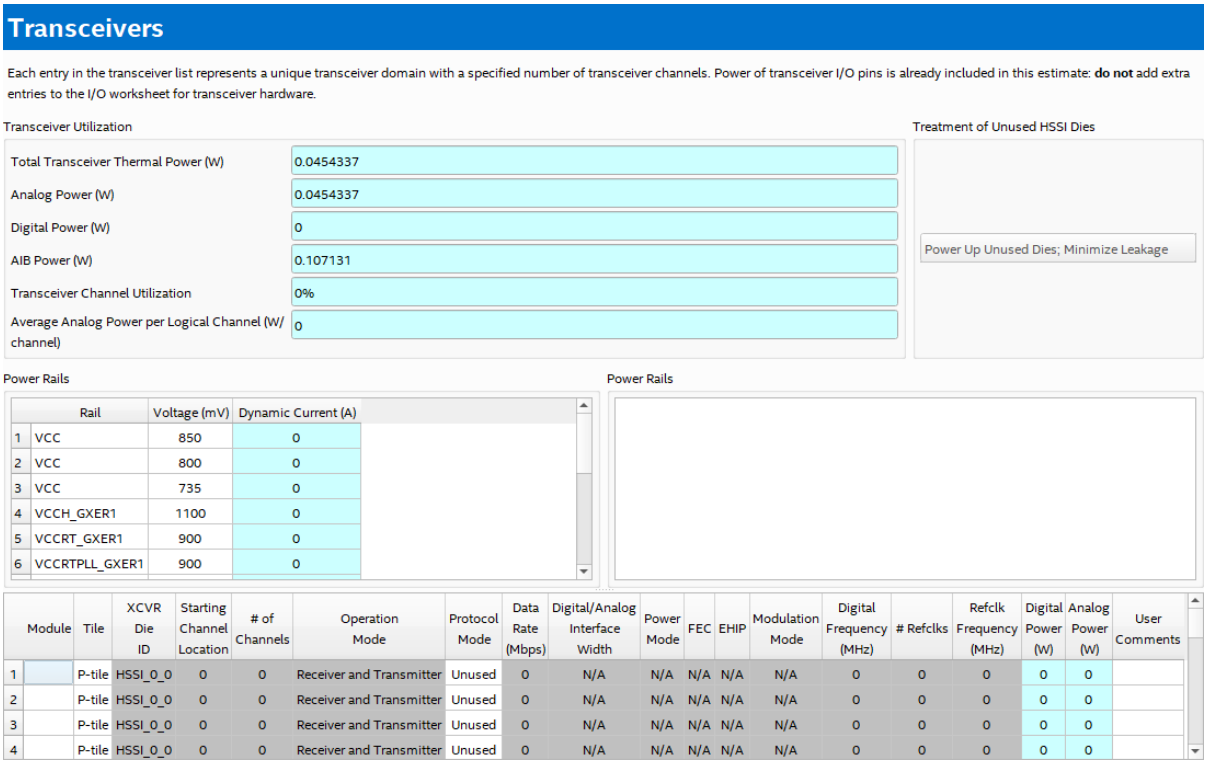


Table 11. General Settings in the Transceiver Tab

Input Parameter	Description
Total Thermal Power (W)	Total power dissipated in all modules on this page (in watts).
Treatment of Unused HSSI Dies	All currently supported transceiver tiles in the Agilex family always have to be powered up. Consequently, this field is currently always set to **Power Up Unused Dies**; **Minimize Leakage**.

Each row in the Transceiver tab represents a separate transceiver domain. Enter the following parameters for each transceiver domain:

Table 12. Transceiver Tab Information

Column Heading	Description
Module	Specifies a name for the module. This is an optional value.
Tile	Specifies the type of transceiver die on which transceiver channels are located. Some devices may include more than one type of transceiver die. This field changes depending on the device options that you choose on the **Main** tab.
XCVR Die ID	Specify the transceiver die on which transceiver channels on this row are located.
Starting Channel Location	Specify the starting location within the die for the channels specified in this row. For example, if a given row contains 3 channels, and starting location is specified to be 12, channels are assumed to be in locations 12, 13, and 14. Location 0 denotes the bottom-most channel on the transceiver die.

continued...

Column Heading	Description
# of Channels	Specifies the number of channels used in this transceiver domain. Each row represents one transceiver domain. These channels are grouped together in one transceiver bank, or two or more adjacent transceiver banks and clocked by one or more common transmitter PLLs. For E-tile transceivers, if the selected modulation mode is *High Data Rate PAM4*, enter 2 physical channels to represent 1 logical channel.
Operation Mode	Specifies whether the hardware is configured in full duplex transceiver mode (receiver and transmitter), Receiver Only mode, or Transmitter Only mode. Allowed values depend on the selected tile and protocol mode.
Protocol Mode	Specifies the protocol mode. Allowed values depend on the selected tile.
Data Rate (Mbps)	Specifies the data rate (in Mbps) for the transceiver. Allowed values depend on the selected protocol mode and selected device.
Digital/Analog Interface Width	Specify the width of the parallel data bus between PCS and PMA. For E-tile PMA Direct, set to PMA parallel data width, even if FPGA FIFO widens the interface. As an example, for 25 Gbps PMA Direct you would typically set this value to 32. When the FEC or EHIP is used, you would set this value to 32 for NRZ mode and 64 for PAM4 mode.
Power Mode	E-tile transceivers can operate at either Normal Power Mode or Low Power Mode. For thermal analysis and regulator sizing, you must set the E-tile transceivers in the Normal Power Mode, because your board design must take into consideration the maximum power conditions. Refer to the E-tile Transceiver PHY User Guide for information on how to switch transceivers from Normal Power Mode to Low Power Mode.
FEC	Specify the Forward Error Correction setting. This field is applicable only to E-tile transceivers.
EHIP	Specify the Ethernet Hard IP protocol. This field is applicable only to E-tile transceivers.
Modulation Mode	Specify the data modulation mode of transceiver channels. This field is applicable only to E-tile transceivers. When you select *High Data Rate PAM4* for this field, 2 physical channels are paired to represent 1 logical channel. When specifying # of Channels, enter the number of physical channels (that is, in multiples of 2).
Digital Frequency (MHz)	Specify the digital frequency at which the digital portion of the transceiver (including FEC and EHIP) operates. This field is applicable only to E-tile transceivers.
# Refclks	Specify the number of reference clocks in use. If another interface on this tile is using the same reference clock, and you have already entered this clock in another row, enter 0 in this row to avoid double counting. This field is applicable only to E-tile transceivers.
Refclk Frequency (MHz)	Specify the reference clock frequency. This field is applicable only to E-tile transceivers.
Digital Power (W)	The total power of all digital circuity associated with the channels specified on this row, such as the Embedded Multi-die Interconnect Bridge (EMIB). It excludes power of blocks whose power may be shared among multiple channels (and therefore multiple rows), such as the FEC and 100G EHIP in the case of E-tile usage.
Analog Power (W)	The total power of all analog circuity associated with the channels specified on this row. It excludes power of blocks whose power may be shared among multiple channels (and therefore multiple rows), such as the clock network.
User Comments	Enter any comments. This is an optional entry.

For more information about the transceiver architecture of the supported device families, refer to the appropriate *Transceiver PHY User Guide* for Intel Agilex devices.

4.13. Intel FPGA PTC - HPS Tab

The HPS tab of the Intel FPGA Power and Thermal Calculator (PTC) applies to devices with HPS.

To enable parameter entry into the HPS tab, first select a device that supports HPS in the **Main** tab or in **Device Selection**, then turn **ON** the **HPS System Switch** in the HPS tab. For Intel Agilex devices, select your peripheral modules in the I/O-IP tab.

Figure 16. HPS Tab of the Power and Thermal Calculator

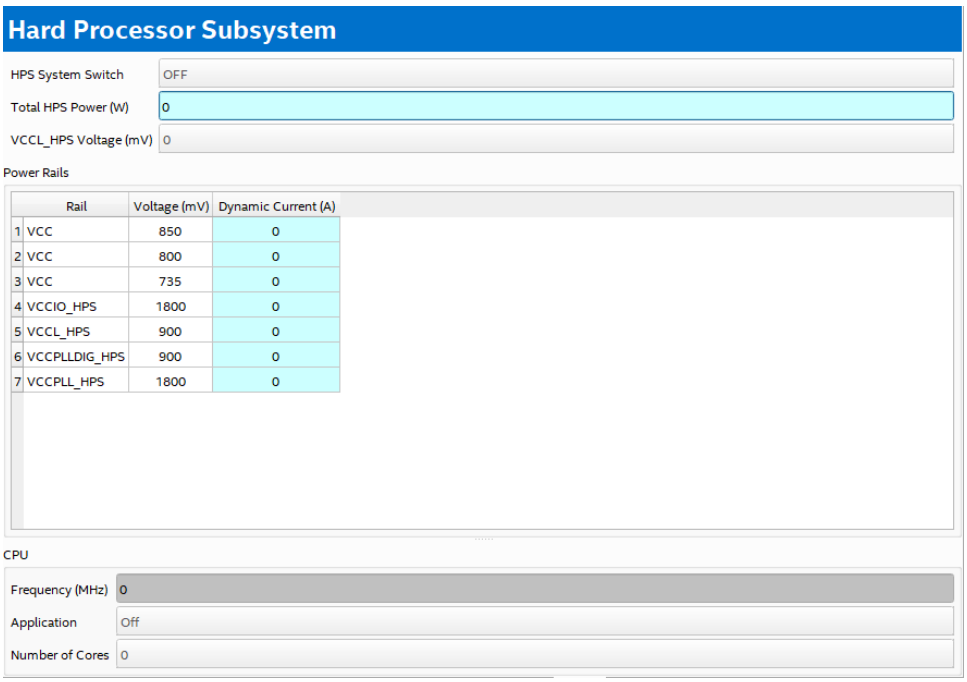


Table 13. HPS Input Parameter Information

Input Parameter	Description
HPS System Switch	Turns the HPS system on or off. This selection affects the static power.
Total HPS Power (W)	Specifies the total power dissipated by the active processors (in W).
VCCL_HPS Voltage (mV)	Specifies the core HPS voltage (in mV).

Table 14. CPU Parameters in the HPS Tab

Parameters	Description
Frequency (MHz)	Specifies the operating frequency of all CPUs (in MHz).
Application	Select a benchmark application representative of the application running on the CPUs.
Number of Cores	Specifies the number of cores in the CPU running the selected application.

4.14. Intel FPGA PTC - Report Tab

The Report tab shows per-rail currents calculated by the Intel FPGA Power and Thermal Calculator (PTC).

Figure 17. Report Tab of the Power and Thermal Calculator

Power and Thermal Calculator Report

	Rail	Voltage (mV)	Static Current (A)	Dynamic Current (A)	Total Current Before SmartVID Savings (A)	Total Current (A)	Margin
1	VCC	850	3.40008	0.998638	4.39871	4.39871	
2	VCC	800					
3	VCC	735					
4	VCCADC	1800	0.0105082	0.00188833	0.0123965	0.0123965	
5	VCCA_PLL	1800	0.0515321		0.0515321	0.0515321	
6	VCCBAT	1800	4.128340E-06		4.128340E-06	4.128340E-06	
7	VCCCLK_GXER1	2500	0.0635746		0.0635746	0.0635746	
8	VCCCLK_GXPL1	1800	0.00159184		0.00159184	0.00159184	
9	VCCFUSEWR_SDM	2400	0.002475		0.002475	0.002475	
10	VCCFUSE_GXP	900	0.00122357	0.0055	0.00672357	0.00672357	
11	VCCH	900	0.00949204	0.0207962	0.0302882	0.0302882	
12	VCCH_GXPL1	1800	0.00121987		0.00121987	0.00121987	
13	VCCH_GXER1	1100	0.0291067		0.0291067	0.0291067	
14	VCCH_SDM	900	3.150000E-04		3.150000E-04	3.150000E-04	
15	VCCIO_HPS	1800					
16	VCCIO_PIO_2A	1200					
17	VCCIO_PIO_2A	1500					
18	VCCIO_PIO_2B	1200	0.37911		0.37911	0.37911	
19	VCCIO_PIO_2B	1500					

The Report tab provides current requirements for each voltage rail, expressed in terms of static current, dynamic current, and total current.

Table 15. Current and Power Regulator Requirements Per Voltage Rail

Column Heading	Description
Rail	Name of the voltage rail.
Voltage (mV)	Rail voltage.
Static Current (A)	Indicates the component of current consumed from the specified power rail whenever the power is applied to the rail, independent of circuit activity (in A). This current is dependent on device size, device grade, power characteristics and junction temperature.
Dynamic Current (A)	Indicates the component of active current drawn from the specified power rail due to signal activity of all modules on all tabs (in A). This current depends on device size, but is independent of device grade, power characteristics and junction temperature.

continued...

Column Heading	Description
Total Current Before SmartVID Savings (A)	Indicates the total current consumed from the specified power rail before SmartVID savings (in A). The sum of static and dynamic currents.
Total Current (A)	Indicates the total current consumed from the specified power rail (in A). For devices and rails supporting SmartVID, this column shows total current after SmartVID power savings; otherwise, the current reported in this column should equal the sum of static and dynamic currents.
Margin	Indicates the recommended margin on total current for regulator sizing. The recommended margin on the V_{cc} rail is calculated based on the ratio of dynamic to static power.

5. Factors Affecting the Accuracy of the Intel FPGA Power and Thermal Calculator

Many factors can affect the estimated values displayed in the Intel FPGA Power and Thermal Calculator (PTC). In particular, the input parameters entered concerning toggle rates and temperature must be accurate to ensure that the system is modeled correctly in the PTC.

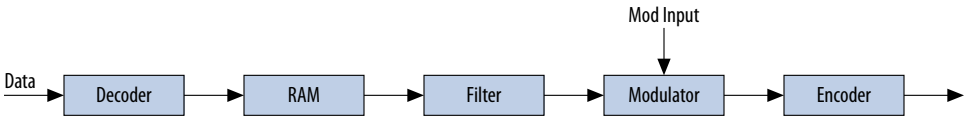
5.1. Toggle Rate

The toggle rates specified in the Power and Thermal Calculator (PTC) can have a large impact on the dynamic power consumption displayed. To obtain an accurate estimate, you must input toggle rates that are realistic. Determining realistic toggle rates requires knowing what kind of input the FPGA is receiving and how often it toggles.

To get an accurate estimate if the design is not complete, isolate the separate modules in the design by function, and estimate the resource usage along with the toggle rates of the resources. The easiest way to accomplish this is to use previous designs to estimate the toggle rates for modules with similar function.

The input data in the following figure is encoded for data transmission and has a roughly 50% toggle rate.

Figure 18. Decoder and Encoder Block Diagram



In this case, you must estimate the following:

- Data toggle rate
- Mod Input toggle rate
- Resource estimate for the Decoder, RAM, Filter, Modulator, and Encoder module
- Toggle rate for the Decoder, RAM, Filter, Modulator, and Encoder module

You can generate these estimates in many ways. If you used similar modules in the past with data inputs of roughly the same toggle rates, you can use that information. If MATLAB* simulations are available for some blocks, you can obtain the toggle rate information from the simulations. If the HDL is available for some of the modules, you can simulate them to obtain toggle rates.

Intel Corporation. All rights reserved. Agilex, Altera, Arria, Cyclone, Enpirion, Intel, the Intel logo, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.
*Other names and brands may be claimed as the property of others.

ISO 9001:2015 Registered

If the HDL is complete, the best way to determine toggle rates is to simulate the design. The accuracy of toggle rate estimates depends on the accuracy of the input vectors. Therefore, determining whether or not the simulation coverage is high gives you a good estimate of how accurate the toggle rate information is.

The Intel Quartus Prime software can determine toggle rates of each resource used in the design if you provide information from simulation tools. Designs can be simulated in many different tools and the information provided to the Intel Quartus Prime software through a Signal Activity File (`.saf`) or Value Change Dump (`.vcd`) file. The Intel Quartus Prime Power Analyzer provides the most accurate power estimate.

6. Document Revision History for the Intel FPGA Power and Thermal Calculator User Guide

Document Version	Intel Quartus Prime Version	Changes
2020.02.14	19.4	Initial release.

Intel Corporation. All rights reserved. Agilex, Altera, Arria, Cyclone, Enpirion, Intel, the Intel logo, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.
*Other names and brands may be claimed as the property of others.

ISO 9001:2015 Registered

A. Measuring Static Power

Follow these steps to measure static power in your design.

1. Verify that the device is properly configured and in user mode. (CONF_DONE, NSTATUS, NCONFIG, and INIT_DONE values should be high.)
2. Wait until a stable junction temperature (thermal equilibrium) is reached.
   - Use of a thermally controlled chamber is recommended.
   - You can measure the junction temperature of the FPGA using the on-chip temperature sensing diode (TSD). Refer to your device documentation for details on using the TSD. Alternatively, you can measure the junction temperature with the Intel Agilex Temperature Sensor IP Core, but with reduced accuracy.
   - If a thermally controlled chamber is not available, use temperature feedback from the on-chip TSD or Intel Agilex Temperature Sensor IP Core to control a heat sink fan to achieve a desired junction temperature.
   - You can also use a heat gun to achieve a desired temperature; however, this method offers less thermal control.
3. Keep all inputs constant and do not toggle any I/Os or any clock signals (except for the clock to the Intel Agilex Temperature Sensor IP Core, if you are using the Intel Agilex Temperature Sensor IP Core to measure temperature.)
4. Depending on the board design, you can measure static current in one of several ways:
   - Use a regulator with the ability to measure voltage drop across a shunt resistor, and query the power measurement through the power management bus (PMBus)/system management bus (SMBus) interface.
   - If a regulator with PMBus/SMBus support is not available, you can measure the voltage drop across the shunt resistor manually for each power supply and calculate the current from the voltage drop.
   - If you use an external power supply, query the current measurement from the power supply according to the manufacturer's specifications.
5. If you want to isolate and understand the static power component of your design's total power consumption, take several current measurements across a range of temperatures and record the junction temperature of each measurement. Refer to the junction temperatures to correlate static power measurements with their corresponding total power measurements.
6. The silicon static power measurements can be compared with the static power estimate from the Intel Quartus Prime Power Analyzer report or the static values shown on the **Report** tab in the PTC.

Intel Corporation. All rights reserved. Agilex, Altera, Arria, Cyclone, Enpirion, Intel, the Intel logo, MAX, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.
*Other names and brands may be claimed as the property of others.

ISO 9001:2015 Registered