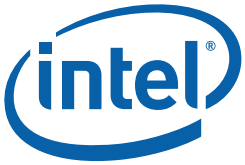

Intel® 3 Series Express Chipset Family

Datasheet

- For the Intel® 82Q35, 82Q33, 82G33 Graphics and Memory Controller Hub (GMCH) and Intel® 82P35 Memory Controller Hub (MCH)

August 2007

Document Number: 316966-002

Contents

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Revision History

Revision Number	Description	Revision Date
-001	• Initial release.	June 2007
-002	• Added Intel 82Q35 GMCH and Intel 82Q33 GMCH specifications	August 2007

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Intel® 3 Series Chipset (G)MCH Features

- Processor/Host Interface (FSB)
  - Supports Intel® Core™2 Duo desktop processor
  - Supports Intel® Core™2 Quad desktop processor
  - 800/1067/1333 MT/s (200/266/333 MHz) FSB
  - Hyper-Threading Technology (HT Technology)
  - FSB Dynamic Bus Inversion (DBI)
  - 36-bit host bus addressing
  - 12-deep In-Order Queue
  - 1-deep Defer Queue
  - GTL+ bus driver with integrated GTL termination resistors
  - Supports cache Line Size of 64 bytes
- System Memory Interface
  - One or two channels (each channel consisting of 64 data lines)
  - Single or Dual Channel memory organization
  - DDR2-800/667 frequencies
  - DDR3-1066/800 frequencies (82G33 GMCH and 82P35 MCH only)
  - Unbuffered, non-ECC DIMMs only
  - Supports 1-Gb, 512-Mb DDR2 or DDR3 technologies for x8 and x16 devices
  - 8 GB maximum memory
- Direct Media Interface (DMI)
  - Chip-to-chip connection interface to Intel ICH9
  - 2 GB/s point-to-point DMI to ICH9 (1 GB/s each direction)
  - 100 MHz reference clock (shared with PCI Express graphics attach)
  - 32-bit downstream addressing
  - Messaging and Error Handling
- PCI Express* Interface
  - One x16 PCI Express port
  - Compatible with the *PCI Express Base Specification, Revision 1.1*
  - Raw bit rate on data pins of 2.5 Gb/s resulting in a real bandwidth per pair of 250 MB/s
- Integrated Graphics Device (82Q35, 82Q33, 82G33 GMCH only)
  - Core frequency of 400 MHz
  - 1.6 GP/s pixel rate
  - High-Quality 3D Setup and Render Engine
  - High-Quality Texture Engine
  - 3D Graphics Rendering Enhancements
  - 2D Graphics
  - Video Overlay
  - Multiple Overlay Functionality
- Analog Display (82Q35, 82Q33, 82G33 GMCH only)
  - 350 MHz Integrated 24-bit RAMDAC
  - Up to 2048x1536 @ 75 Hz refresh
  - Hardware Color Cursor Support
  - DDC2B Compliant Interface
- Digital Display (82Q35, 82Q33, 82G33 GMCH only)
  - SDVO ports in single mode supported
  - 225 MHz dot clock on each 12-bit interface
  - Flat panels up to 2048x1536 @ 60 Hz or digital CRT/HDTV at 1400x1050 @ 85Hz
  - Dual independent display options with digital display
  - Multiplexed digital display channels (supported with ADD2 Card).
  - Supports TMDS transmitters or TV-Out encoders
  - ADD2/MEC card uses PCI Express graphics x16 connector
  - Two channels multiplexed with PCI Express* Graphics port
  - Supports Hot-Plug and Display
- Thermal Sensor
  - Catastrophic Trip Point support
  - Hot Trip Point support for SMI generation
- Power Management
  - PC99 suspend to DRAM support (“STR”, mapped to ACPI state S3)
  - ACPI Revision 2.0 compatible power management
  - Supports processor states: C0, C1, C2
  - Supports System states: S0, S1, S3, and S5
  - Supports processor Thermal Management 2
- Package
  - FC-BGA. 34 mm × 34 mm. The 1226 balls are located in a non-grid pattern

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1 Introduction

The Intel® 3 Series Chipsets are designed for use with the Intel® Core™2 Duo desktop processor and Intel® Core™2 Quad processor based platforms. Each chipset contains two components: GMCH (or MCH) for the host bridge and I/O Controller Hub 9 (ICH9) for the I/O subsystem. The 82Q33 GMCH is part of the Intel® Q35 Express chipset. The 82Q33 GMCH is part of the Intel® Q33 Express chipset. The 82G33 GMCH is part of the Intel® G33 Express chipset. The 82P35 MCH is part of the Intel® P35 Express chipset. The ICH9 is the ninth generation I/O Controller Hub and provides a multitude of I/O related functions. The following figures show example system block diagrams for the Intel® Q35, Q33, G33 and P35 Express chipsets.

This document is the datasheet for the Intel® 82Q35, 82Q33, and 82G33 Graphics and Memory Controller Hub (GMCH) and Intel® 82P35 Memory Controller Hub (MCH). Topics covered include; signal description, system memory map, PCI register description, a description of the (G)MCH interfaces and major functional units, electrical characteristics, ballout definitions, and package characteristics.

The primary difference between the Intel® 82Q35, 82Q33, 82G33 GMCH and 82P35 MCH is that the 82Q35 GMCH, 82Q33 GMCH, and 82G33 GMCH have an integrated graphics device (IGD) plus the associated display interfaces. The 82P35 does not contain an IGD and the associated interfaces.

Note: Unless otherwise specified, the information in this document applies to the Intel® 82Q35, 82Q33, 82G33 Graphics and Memory Controller Hub (GMCH) and Intel® 82P35 Memory Controller Hub (MCH).

Note: The term (G)MCH refers to the 82Q35 GMCH, 82Q33 GMCH, 82G33 GMCH and 82P35 MCH.

Note: Unless otherwise specified, ICH9 refers to the Intel® 82801IB ICH9, Intel® 82801IR ICH9R, and Intel® 82801IH ICH9DH I/O Controller Hub 9 components.

Note: The term ICH9 refers to the ICH9, ICH9R, and ICH9DH components.

The following table provides a high-level component feature summary.

Capability	82Q35 GMCH	82Q33 GMCH	82G33 GMCH	82P35 MCH
Memory Speed	DDR2-800/667	DDR2-800/667	DDR2-800/667 DDR3-1067/800	DDR2-800/667 DDR3-1067/800
Integrated Graphics Device	Yes	Yes	Yes	No
Discrete Graphics	PCI Express x16	PCI Express x16	PCI Express x16	PCI Express x16
PCI Express Interface	Yes (1) x16	Yes (1) x16	Yes (1) x16	Yes (1) x16
SDVO Expansion	ADD2/MEC	ADD2/MEC	ADD2/MEC	—
Dual Independent Display	Yes	Yes	Yes	—
Intel® Active Management Technology (AMT)[1,2]	Yes[1]	No	No	No
Alerting Standard Format (ASF)	Yes[1]	Yes	Yes (DDR2 only)[3]	Yes (DDR2 only)[3]

NOTE:

1. For the 82Q35 GMCH, only one manageability solution can be supported, AMT or ASF.
2. Intel® Active Management Technology requires the platform to have an Intel® AMT-enabled chipset, network hardware and software, connection with a power source and an active LAN port.
3. ASF is available on 82G33 GMCH and 82P35 MCH with DDR2 system memory only. ASF on 82G33 GMCH and 82P35 MCH with DDR3 system memory is not a validated configuration.

Figure 1-1. Intel® Q35/Q33 Express Chipsets System Block Diagram Example

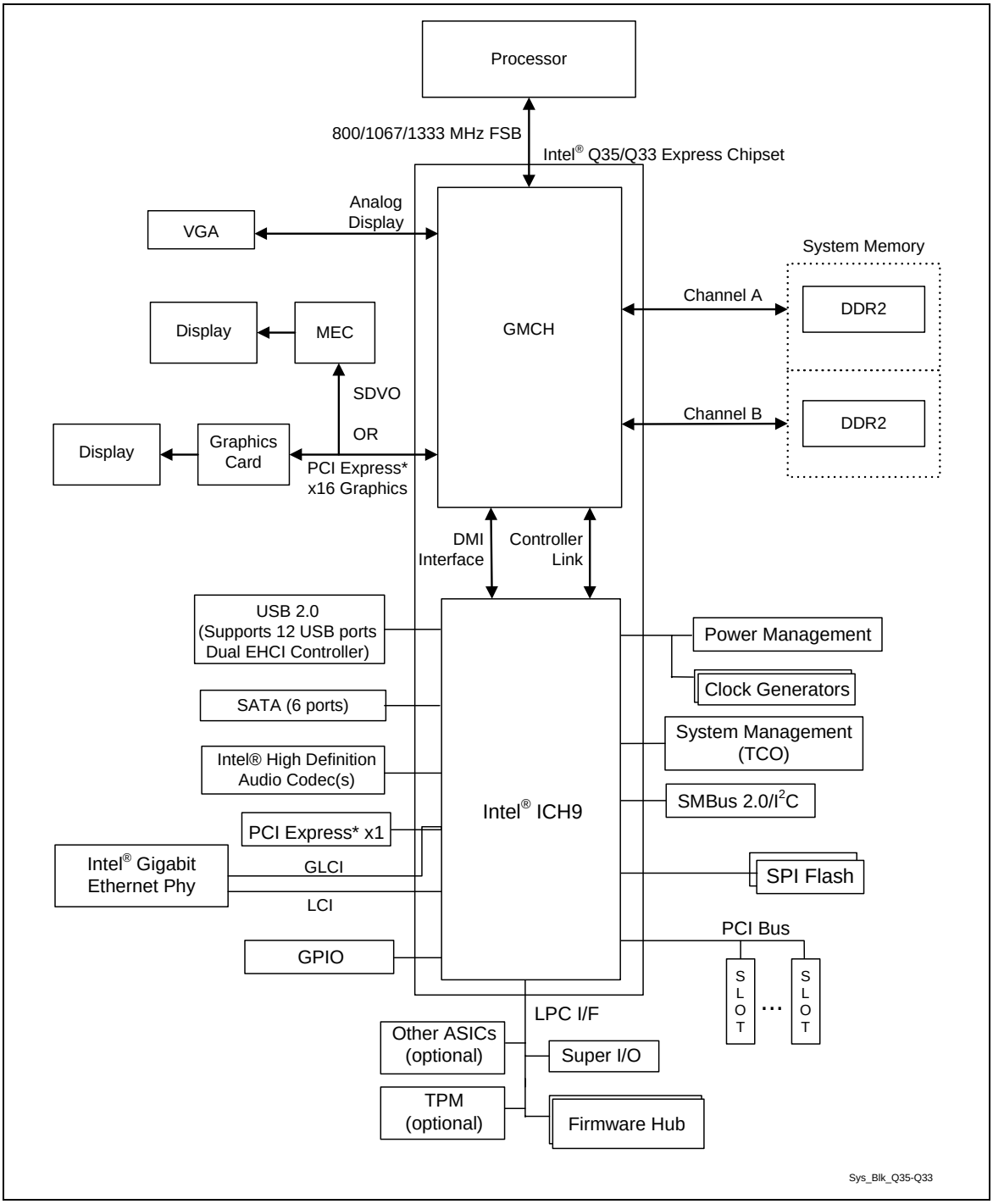


Figure 1-2. Intel® G33 Express Chipset System Block Diagram Example

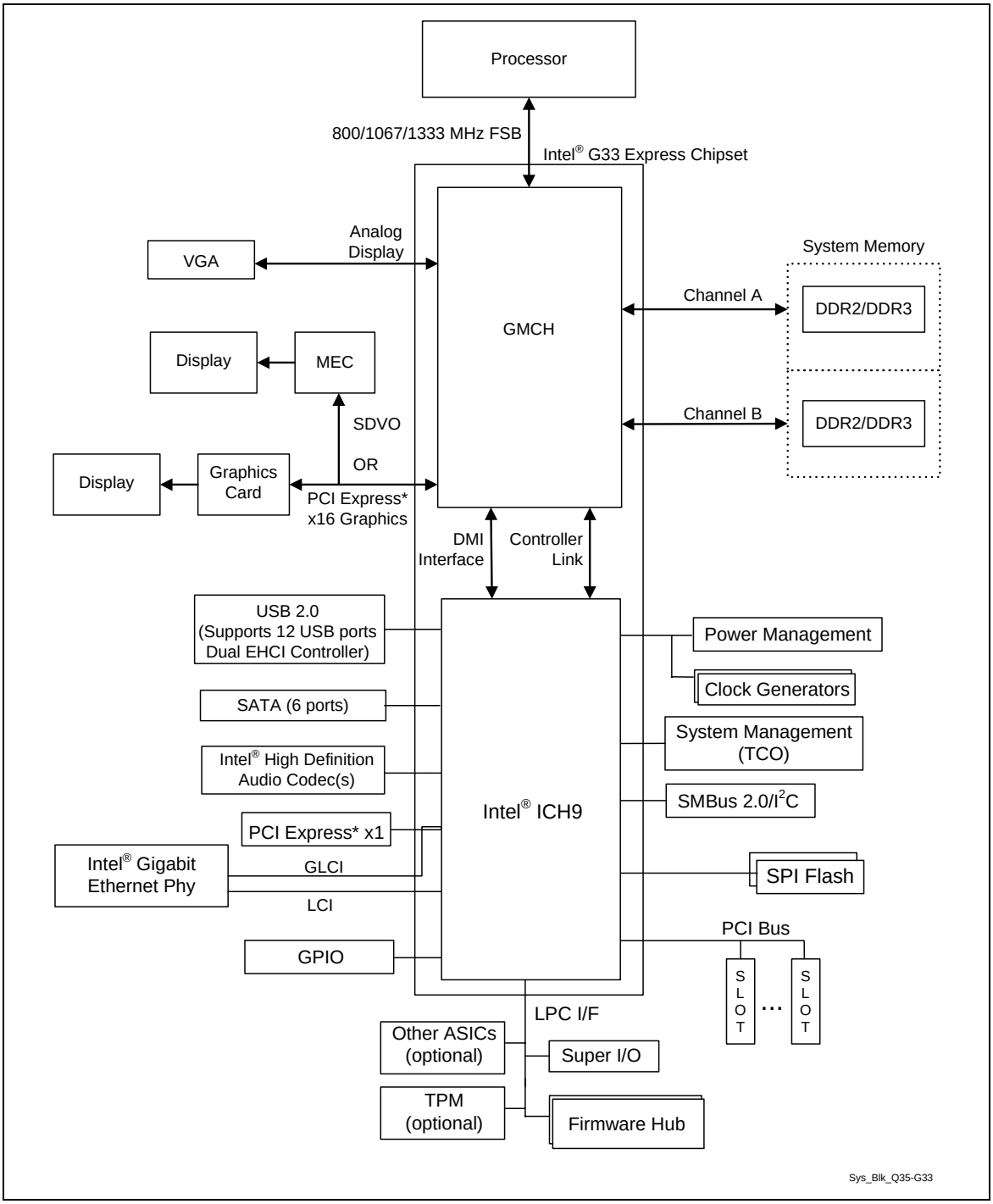
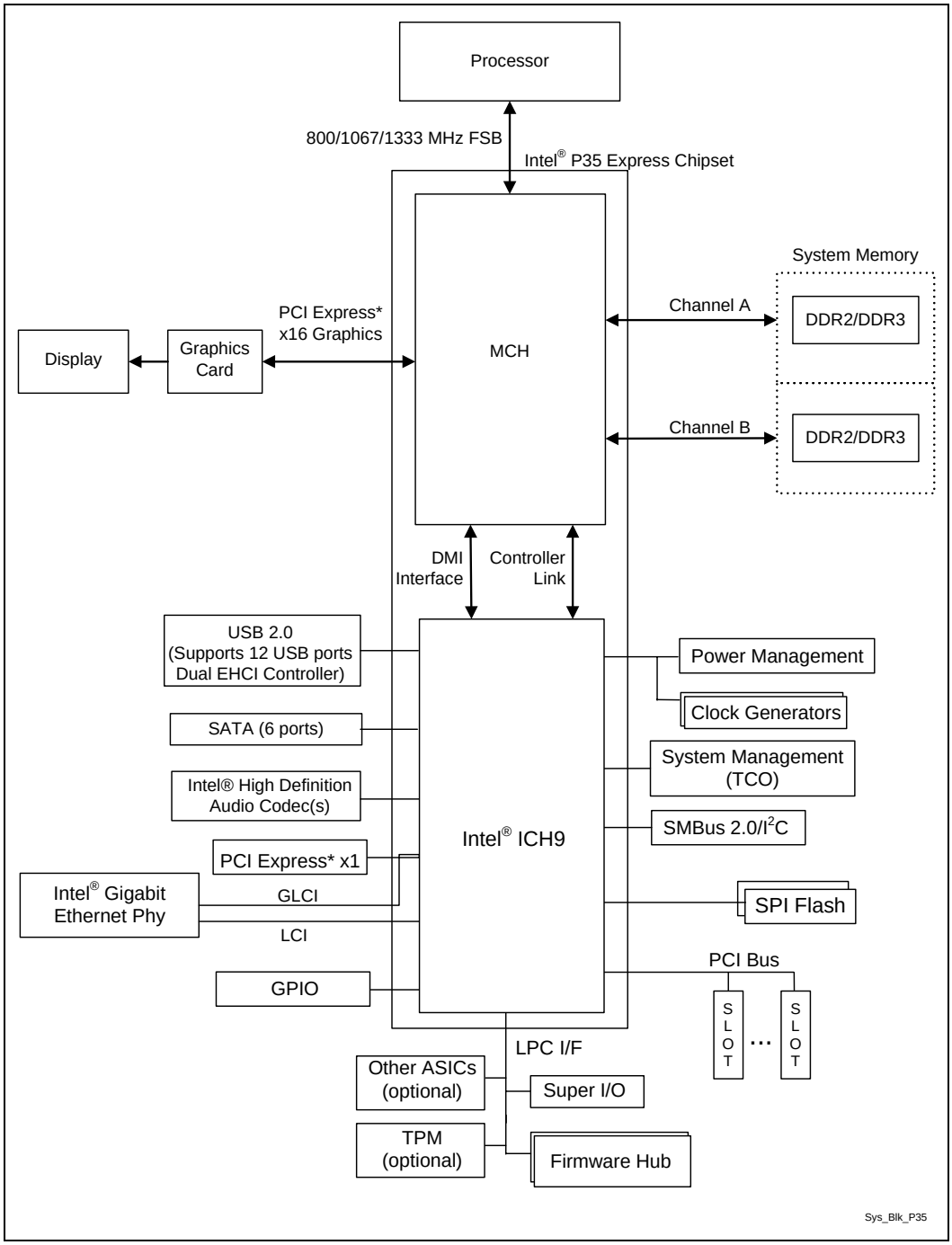


Figure 1-3. Intel® P35 Express Chipset System Block Diagram Example



1.1 Terminology

Term	Description
ADD Card	Advanced Digital Display Card. Provides digital display options for an Intel Graphics Controller that supports ADD cards (have DVOs multiplexed with AGP interface). Keyed like an AGP 4x card and plugs into an AGP connector. Will **not** work with an Intel Graphics Controller that implements Intel® SDVO.
ADD2 Card	Advanced Digital Display Card – **2**nd Generation. Provides digital display options for an Intel graphics controller that supports ADD2 cards. Plugs into an x16 PCI Express* connector but utilizes the multiplexed SDVO interface. Will **not** work with an Intel Graphics Controller that supports Intel® DVO and ADD cards.
Chipset / Root – Complex	Used in this specification to refer to one or more hardware components that connects processor complexes to the I/O and memory subsystems. The chipset may include a variety of integrated devices.
CLink	GMCH-ICH9 Control Link
Core	The internal base logic in the (G)MCH
CRT	Cathode Ray Tube
DBI	Dynamic Bus Inversion
DDR2	A second generation Double Data Rate SDRAM memory technology
DDR3	A third generation Double Data Rate SDRAM memory technology
DMA Remapping	Translating the address in a DMA request (DVA) to a host physical address (HPA)
DMI	(G)MCH-Intel® ICH9 Direct Media Interface
Domain	A collection of physical, logical or virtual resources that are allocated to work together. Domain is used as a generic term for virtual machines, partitions, etc.
DVI	Digital Video Interface. Specification that defines the connector and interface for digital displays.
DVMT	Dynamic Video Memory Technology
FSB	Front Side Bus, synonymous with Host or processor bus
Full Reset	Full reset is when PWROK is de-asserted. Warm reset is when both RSTIN# and PWROK are asserted.
GAW	Guest Address Width. GAW refers to the DMA virtual addressability limit.
GMCH	Graphics and Memory Controller Hub. GMCH is a component that contains the processor interface, DRAM controller, and x16 PCI Express port (typically the external graphics interface). It communicates with the I/O controller hub (Intel® ICH9) over the DMI interconnect. The GMCH contains an embedded graphics controller. Memory Controller Hub. See MCH.
GPA	Guest Physical Address is the view of physical memory from software running in a partition. GPA is also used in this document as an example usage for DMA virtual addresses (DVA)

Term	Description
Media Expansion Card (MEC)	Media Expansion Card. MEC provides digital display options for an Intel Graphics Controller that supports MEC cards. Plugs into an x16 PCI Express connector but uses the multiplexed SDVO interface. Adds Video In capabilities to platform. Will **not** work with an Intel Graphics Controller that supports DVO and ADD cards. MEC Will function as an ADD2 card in an ADD2 supported system, but Video In capabilities will not work.
MCH	Memory Controller Hub. MCH is a component that contains the processor interface, DRAM controller, and x16 PCI Express port (typically the external graphics interface). It communicates with the I/O controller hub (Intel® ICH9) over the DMI interconnect. The MCH does not contain an embedded graphics controller.
MGAW	Maximum Guest Address Width. MGAW refers to the maximum DMA virtual addressability supported by a DMA-remapping hardware implementation.
HAW	Host Address Width. This refers to the maximum host physical address that can be accessed by a given processor / root-complex implementation. The host BIOS typically reports the host system address map.
Host	This term is used synonymously with processor
HPA	Host Physical Address
IGD	Internal Graphics Device
INTx	An interrupt request signal where X stands for interrupts A, B, C and D
Intel® ICH9	Ninth generation I/O Controller Hub component that contains the primary PCI interface, LPC interface, USB2.0, SATA, and other I/O functions. For this GMCH, the term Intel® ICH refers to Intel® ICH9.
Intel® ME	Intel® Management Engine that provides core functionality for Intel® AMT.
IOTLB	I/O Translation Look aside Buffer. IOTLB refers to an address translation cache in a DMA-remapping hardware unit that caches effective translations from DVA (GPA) to HPA.
IOQ	In Order Queue
MVMM	A VMM offering that can be measured for security properties
MSI	Message Signaled Interrupt. A transaction conveying interrupt information to the receiving agent through the same path that normally carries read and write commands.
OOQ	Out of Order Queuing
PDE Cache/ Non-leaf Cache	PDE (non-leaf) cache refers to address translation caches in a DMA-remapping hardware unit that caches page directory entries at the various page-directory levels. These are also referred to as non-leaf caches in this document.
PCI Express*	A high-speed serial interface whose configuration is software compatible with the legacy PCI specifications.
Primary PCI	The physical PCI bus that is driven directly by the Intel® ICH9 component. Communication between Primary PCI and the (G)MCH occurs over DMI. Note that the Primary PCI bus is **not** PCI Bus 0 from a configuration standpoint.
SERR	System Error. An indication that an unrecoverable error has occurred on an I/O bus.
Rank	A unit of DRAM corresponding to eight x8 SDRAM devices in parallel or four x16 SDRAM devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a DIMM.
SCI	System Control Interrupt. Used in ACPI protocol.

Term	Description
SDVO	Serial Digital Video Out (SDVO). Digital display channel that serially transmits digital display data to an external SDVO device. The SDVO device accepts this serialized format and then translates the data into the appropriate display format (i.e. TMDS, LVDS, and TV-Out). This interface is not electrically compatible with the previous digital display channel - DVO.
SDVO Device	Third party codec that uses SDVO as an input. May have a variety of output formats, including DVI, LVDS, HDMI, TV-out, etc.
SMI	System Management Interrupt. Used to indicate any of several system conditions such as thermal sensor events, throttling activated, access to System Management RAM, chassis open, or other system state related activity.
TMDS	Transition Minimized Differential Signaling. Signaling interface from Silicon Image that is used in DVI and HDMI.
Intel® TXT	Intel® Trusted Execution Technology defines platform level enhancements that provide the building blocks for creating trusted platforms.
UMA	Unified Memory Architecture used for system memory. Typically used by IGD or ME functionality.
VCO	Voltage Controlled Oscillator
VMM	Virtual Machine Monitor. A software layer that controls virtualization

1.2 Reference Documents

Document Name	Location
Intel® 3 Series Chipset Family Specification Update	www.intel.com/design/chipsets/specupdt/316967.htm
Intel® Q35/Q33/G33/P35 Express Chipset Family Thermal and Mechanical Design Guide.	www.intel.com/design/chipsets/designex/316968,htm
Intel® Core™2 Duo Processor and Intel® Pentium® Dual Core Thermal and Mechanical Design Guide	www.intel.com/design/processor/designex/317804.htm
Intel® I/O Controller Hub 9 (ICH9) Family Thermal Mechanical Design Guide.	www.intel.com/design/chipsets/designex/316974.htm
Intel® I/O Controller Hub 9 (ICH9) Family Datasheet	www.intel.com/design/chipsets/datashts/316972.htm
Designing for Energy Efficiency White Paper	www.intel.com/design/chipsets/applnots/316970.htm
Intel® Q35/Q33/P35/G33 Express Chipset Memory Technology and Configuration Guide White Paper	www.intel.com/design/chipsets/applnots/316971.htm
Advanced Configuration and Power Interface Specification, Version 2.0	http://www.acpi.info/
Advanced Configuration and Power Interface Specification, Version 1.0b	http://www.acpi.info/
The PCI Local Bus Specification, Version 2.3	http://www.pcisig.com/specifications
PCI Express Specification, Version 1.1*	http://www.pcisig.com/specifications

1.3 (G)MCH Overview

The (G)MCH designed for use with the Intel® Core™2 Duo desktop processors and Intel® Core™2 Quad desktop processors in desktop platforms. The role of a (G)MCH in a system is to manage the flow of information between its four interfaces: the processor interface, the System Memory interface, the External Graphics interface, and the I/O Controller through DMI interface. This includes arbitrating between the four interfaces when each initiates transactions. The 82G33 and 82P35 (G)MCHs support one or two channels of DDR2 or DDR3 SDRAM. The 82Q35 and 82Q33 GMCHs support one or two channels of DDR2 SDRAM. The (G)MCH also supports the PCI Express based external graphics attach. The Q35/Q33/G33/P35 Express chipset platforms support the ninth generation I/O Controller Hub (Intel® ICH9) to provide a multitude of I/O related features.

1.3.1 Host Interface

The (G)MCH can use a single LGA775 socket processor. The (G)MCH supports FSB frequencies of 200/266/333 MHz. Host-initiated I/O cycles are decoded to PCI Express, DMI, or the (G)MCH configuration space. Host-initiated memory cycles are decoded to PCI Express, DMI, or system memory. PCI Express device accesses to non-cacheable system memory are not snooped on the host bus. Memory accesses initiated from PCI Express using PCI semantics and from DMI to system SDRAM will be snooped on the host bus.

Capabilities of the Host Interface include:

- Supports Intel® Core™2 Duo processors and Intel® Core™2 Quad processors
- Supports Front Side Bus (FSB) at 800/1066/1333 MT/s (200/266/333 MHz)
- Supports FSB Dynamic Bus Inversion (DBI)
- Supports 36-bit host bus addressing, allowing the processor to access the entire 64 GB of the host address space
- Has a 12-deep In-Order Queue to support up to twelve outstanding pipelined address requests on the host bus
- Has a 1-deep Defer Queue
- Uses GTL+ bus driver with integrated GTL termination resistors
- Supports a Cache Line Size of 64 bytes

1.3.2 System Memory Interface

The (G)MCH integrates a system memory DDR2 and DDR3 (82G33 GMCH and 82P35 MCH only) controller with two, 64-bit wide interfaces. The buffers support both SSTL_1.8 (Stub Series Terminated Logic for 1.8 V) and SSTL_1.5 (Stub Series Terminated Logic for 1.5 V) signal interfaces. The memory controller interface is fully configurable through a set of control registers.

Capabilities of the system memory interface include:

- Directly supports one or two channels of DDR2 or DDR3 (82G33 GMCH and 82P35 MCH only) memory with a maximum of two DIMMs per channel.
- Supports single and dual channel memory organization modes.
- Supports a data burst length of eight for all memory organization modes.
- Supports memory data transfer rates of 667 MHz and 800 MHz for DDR2, and 800 MHz and 1066 MHz for DDR3.
- I/O Voltage of 1.8 V for DDR2 and 1.5 V for DDR3.
- Supports only un-buffered non-ECC DDR2 or DDR3 DIMMs
- Supports maximum memory bandwidth of 6.4 GB/s in single-channel or dual-channel asymmetric mode, or 12.8 GB/s in dual-channel symmetric mode assuming DDR2 800 MHz.
- Supports maximum memory bandwidth of 8.5 GB/s in single-channel or dual-channel asymmetric mode, or 17 GB/s in dual-channel interleaved mode assuming DDR3 1066 MHz.
- Supports 512 Mb and 1 Gb DDR2 or DDR3 (82G33 GMCH and 82P35 MCH only) DRAM technologies for x8 and x16 devices.
- Using 512 Mb device technologies, the smallest memory capacity possible is 256 MB, assuming Single Channel Mode with a single x16 single sided un-buffered non-ECC DIMM memory configuration.
- Using 1 Gb device technologies, the largest memory capacity possible is 8 GB, assuming Dual Channel Mode with four x8 double sided un-buffered non-ECC DIMM memory configuration.
- Supports up to 32 simultaneous open pages per channel (assuming 4 ranks of 8 bank devices).
- Supports opportunistic refresh scheme. The (G)MCH has an arbitration scheme to refresh memory when the DRAM is idle.
- Supports Partial Writes to memory using Data Mask (DM) signals.
- Supports a memory thermal management scheme to selectively manage reads and/or writes. Memory thermal management can be triggered either by on-die thermal sensor, or by preset limits. Management limits are determined by weighted sum of various commands that are scheduled on the memory interface.

1.3.3 Direct Media Interface (DMI)

Direct Media Interface (DMI) is the chip-to-chip connection between the (G)MCH and ICH9. This high-speed interface integrates advanced priority-based servicing allowing for concurrent traffic and true isochronous transfer capabilities. Base functionality is completely software transparent permitting current and legacy software to operate normally.

To provide for true isochronous transfers and configurable Quality of Service (QoS) transactions, the ICH9 supports two virtual channels on DMI: VC0 and VC1. These two channels provide a fixed arbitration scheme where VC1 is always the highest priority. VC0 is the default conduit of traffic for DMI and is always enabled. VC1 must be specifically enabled and configured at both ends of the DMI link (i.e., the ICH9 and (G)MCH).

- A chip-to-chip connection interface to Intel ICH9
- 2 GB/s point-to-point DMI to ICH9 (1 GB/s each direction)
- 100 MHz reference clock (shared with PCI Express Graphics Attach)
- 32-bit downstream addressing
- APIC and MSI interrupt messaging support. Will send Intel-defined “End Of Interrupt” broadcast message when initiated by the processor.
- Message Signaled Interrupt (MSI) messages
- SMI, SCI, and SERR error indication

1.3.4 PCI Express* Interface

The (G)MCH contains one 16-lane (x16) PCI Express port intended for an external PCI Express graphics card. The PCI Express port is compliant to the *PCI Express* Base Specification* revision 1.1. The x16 port operates at a frequency of 2.5 Gb/s on each lane while employing 8b/10b encoding, and supports a maximum theoretical bandwidth of 40 Gb/s in each direction. The 82Q35/82Q33/82G33 GMCHs multiplex the PCI Express interface with the Intel® SDVO ports.

- One, 16-lane PCI Express port intended for Graphics Attach, compatible to the PCI Express* Base Specification revision 1.1.
- PCI Express frequency of 1.25 GHz resulting in 2.5 Gb/s each direction per lane.
- Raw bit-rate on the data pins of 2.5 Gb/s, resulting in a real bandwidth per pair of 250 MB/s given the 8b/10b encoding used to transmit data across this interface
- Maximum theoretical realized bandwidth on the interface of 4 GB/s in each direction simultaneously, for an aggregate of 8 GB/s when x16.
- PCI Express* Graphics Extended Configuration Space. The first 256 bytes of configuration space alias directly to the PCI Compatibility configuration space. The remaining portion of the fixed 4 KB block of memory-mapped space above that (starting at 100h) is known as extended configuration space.
- PCI Express Enhanced Addressing Mechanism. Accessing the device configuration space in a flat memory mapped fashion.

- Automatic discovery, negotiation, and training of link out of reset
- Supports traditional PCI style traffic (asynchronous snooped, PCI ordering)
- Supports traditional AGP style traffic (asynchronous non-snooped, PCI Express-relaxed ordering)
- Hierarchical PCI-compliant configuration mechanism for downstream devices (i.e., normal PCI 2.3 Configuration space as a PCI-to-PCI bridge)
- Supports “static” lane numbering reversal. This method of lane reversal is controlled by a Hardware Reset strap, and reverses both the receivers and transmitters for all lanes (e.g., TX[15]->TX[0], RX[15]->RX[0]). This method is transparent to all external devices and is different than lane reversal as defined in the PCI Express Specification. In particular, link initialization is not affected by static lane reversal.

1.3.5 Graphics Features (Intel® 82Q35, 82Q33, 82G33 GMCH Only)

The GMCH provides an integrated graphics device (IGD) delivering cost competitive 3D, 2D and video capabilities. The GMCH contains an extensive set of instructions for 3D operations, 2D operations, motion compensation, overlay, and display control. The GMCH’s video engines support video conferencing and other video applications. The GMCH uses a UMA configuration with DVMT for graphics memory. The GMCH also has the capability to support external graphics accelerators via the PCI Express Graphics (PEG) port but cannot work concurrently with the integrated graphics device. High bandwidth access to data is provided through the system memory port.

1.3.6 SDVO and Analog Display Features (Intel® 82Q35, 82Q33, 82G33 GMCH Only)

The GMCH provides interfaces to a progressive scan analog monitor and two SDVO ports. For the GMCH, the SDVO ports are multiplexed with PCI Express x16 graphics port signals. The GMCH supports two multiplexed SDVO ports that each drive pixel clocks up to 225 MHz. The SDVO ports can each support a single-channel SDVO device. If both ports are active in single-channel mode, they can have different display timing and data.

The digital display channels are capable of driving a variety of SDVO devices (e.g., TMDS, TV-Out). Note that SDVO only works with the Integrated Graphics Device (IGD). The GMCH is capable of driving an Advanced Digital Display (ADD2) card or Media Expansion Card. The Media Expansion Card adds video-in capabilities. The GMCH is compliant with DVI Specification 1.0. When combined with a DVI compliant external device and connector, the GMCH has a high-speed interface to a digital display (e.g., flat panel or digital CRT).

The GMCH is compliant with HDMI specification 1.1. When combined with a HDMI compliant external device and connector, the external HDMI device can support standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable.

Capabilities of the SDVO and Analog Display interfaces include:

- SDVO Support
  - SDVO ports in either single modes supported
  - 3x3 Built In full panel scalar
  - 180 degree Hardware screen rotation
  - Multiplexed Digital Display Channels (Supported with ADD2/MEC)
  - Two channels multiplexed with PCI Express* Graphics port
  - 225 MHz dot clock on each 12-bit interface
  - Supports flat panels up to 1920 x 1200 @ 60 Hz or digital CRT/HDTV at 1400 x1050 @ 85 Hz
  - Supports Hot-Plug and Display
  - Supports TMDS transmitters or TV-out encoders
  - ADD2/Media Expansion card utilizes PCI Express Graphics x16 connector
- Analog Display Support
  - 350 MHz Integrated 24-bit RAMDAC
  - Up to 2048x1536 @ 75 Hz refresh
  - Hardware Color Cursor Support
  - DDC2B Compliant Interface
- Dual Independent Display options with digital display

1.3.7 (G)MCH Clocking

- Differential Host clock of 200/266/333 MHz (HCLKP/HCLKN). Supports transfer rates of 800/1066/1333 MT/s.
- Internal and External Memory clocks of 333 MHz, 400 MHz, and 533 MHz generated from one of two (G)MCH PLLs that use the Host clock as a reference.
- The PCI Express* PLL of 100 MHz Serial Reference Clock (GCLKP/GCLKN) generates the PCI Express core clock of 250 MHz
- Display timings are generated from display PLLs that use a 96 MHz differential non-spread spectrum clock as a reference. Display PLLs can also use the SDVO_TVCLKIN[+/-] from an SDVO device as a reference.
- All of the above clocks are capable of tolerating Spread Spectrum clocking.
- Host, Memory, and PCI Express Graphics PLLs and all associated internal clocks are disabled until PWROK is asserted.

1.3.8 Thermal Sensor

(G)MCH Thermal Sensor support includes:

- Catastrophic Trip Point support for emergency clock gating for the (G)MCH at 115 °C.
- Hot Trip Point support for SMI generation between 85 °C and 105 °C.
- The minimal temperature reported by (G)MCH is 66 °C

1.3.9 Power Management

(G)MCH Power Management support includes:

- PC99 suspend to DRAM support (“STR”, mapped to ACPI state S3)
- SMRAM space remapping to A0000h (128 KB)
- Supports extended SMRAM space above 256 MB, additional 1 MB TSEG from the Base of graphics stolen memory (BSM) when enabled, and cacheable (cacheability controlled by processor)
- ACPI Rev 2.0 compatible power management
- Supports processor states: C0, C1, and C2
- Supports System states: S0, S1, S3 and S5
- Supports processor Thermal Management 2 (TM2)
- Supports Manageability states M0, M1-S3, M1-S5, Moff-S3, Moff-S5

1.3.10 Intel® Active Management Technology (Intel® AMT) / Controller Link (Intel® 82Q35 GMCH Only)

The GMCH supports Intel® Active Management Technology that combines hardware and software solutions to provide:

- Asset Management
- OOB diagnostics
- Agent Present and Health Detect
- Network Protection with System Defense

Intel® AMT integrates advanced manageability features into hardware and firmware. Intel® AMT extends the capabilities of existing management solutions by enabling system and software asset information, remote diagnostics, and recovery plus network protection through the OOB (Out-Of-Band) channel (i.e., always available even when the system is in a low-power “off” state or the OS is hung). Controller link is the Intel® Management Engine link between the GMCH and the ICH9.

1.3.11 Intel® Trusted Execution Technology (Intel® 82Q35 GMCH Only)

Intel® Trusted Execution Technology (Intel® TXT) is a security initiative that involves the processor, chipset and platform. Intel® Trusted Execution Technology requires the following support in the chipset:

- FSB encodings for LTMW and LTMR cycles
- Measured launch of a VMM, using a TPM
- Protected path from the processor to the TPM, which is enabled by the processor
- Ranges of memory protected from DMA accesses.

Intel® TXT is only supported by the Intel® Q35 Express chipset.

1.3.12 Intel® Virtualization Technology for Directed I/O (Intel® VT-d) (Intel® 82Q35 GMCH Only)

Intel® Virtualization Technology for Directed I/O comprises technology components to support virtualization of platforms based on Intel architecture microprocessors. This document describes the chipset hardware components supporting I/O virtualization that are in the (G)MCH. Intel® VT-d is only supported by the Intel® Q35 Express chipset.

§

2 Signal Description

This chapter provides a detailed description of (G)MCH signals. The signals are arranged in functional groups according to their associated interface.

The following notations are used to describe the signal type:

Signal Type	Description
PCI Express*	PCI Express interface signals. These signals are compatible with PCI Express 1.1 Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3 V tolerant. Differential voltage spec = (|D+ - D-|) * 2 = 1.2 Vmax. Single-ended maximum = 1.25 V. Single-ended minimum = 0 V.
DMI	Direct Media Interface signals. These signals are compatible with PCI Express 1.1 Signaling Environment AC Specifications, but are DC coupled. The buffers are not 3.3 V tolerant. Differential voltage spec = (|D+ - D-|) * 2 = 1.2 Vmax. Single-ended maximum = 1.25 V. Single-ended minimum = 0 V.
CMOS	CMOS buffers. 1.5 V tolerant.
COD	CMOS Open Drain buffers. 3.3 V tolerant.
HCSL	Host Clock Signal Level buffers. Current mode differential pair. Differential typical swing = (|D+ – D-|) * 2 = 1.4 V. Single ended input tolerant from -0.35 V to 1.2 V. Typical crossing voltage 0.35 V.
HVCMOS	High Voltage CMOS buffers. 3.3 V tolerant.
HVIN	High Voltage CMOS input-only buffers. 3.3 V tolerant.
SSTL_1.8	Stub Series Termination Logic. These are 1.8 V output capable buffers. 1.8 V tolerant.
SSTL_1.5	Stub Series Termination Logic. These are 1.5 V output capable buffers. 1.5 V tolerant
A	Analog reference or output. May be used as a threshold voltage or for buffer compensation.
GTL+	Gunning Transceiver Logic signaling technology. Implements a voltage level as defined by VTT of 1.2 V.

2.1 Host Interface Signals

Note: Unless otherwise noted, the voltage level for all signals in this interface is tied to the termination voltage of the Host Bus (V_{TT}).

Signal Name	Type	Description
FSB_ADSB	I/O GTL+	**Address Strobe:** The processor bus owner asserts FSB_ADSB to indicate the first of two cycles of a request phase. The (G)MCH can assert this signal for snoop cycles and interrupt messages.
FSB_BNRB	I/O GTL+	**Block Next Request:** Used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
FSB_BPRIB	O GTL+	**Priority Agent Bus Request:** The (G)MCH is the only Priority Agent on the processor bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the FSB_LOCKB signal was asserted.
FSB_BREQ0B	O GTL+	**Bus Request 0:** The (G)MCH pulls the processor bus' FSB_BREQ0B signal low during FSB_CPURSTB. The processors sample this signal on the active-to-inactive transition of FSB_CPURSTB. The minimum setup time for this signal is 4 HCLKs. The minimum hold time is 2 HCLKs and the maximum hold time is 20 HCLKs. FSB_BREQ0B should be tri-stated after the hold time requirement has been satisfied.
FSB_CPURSTB	O GTL+	**CPU Reset:** The FSB_CPURSTB signal is an output from the (G)MCH. The (G)MCH asserts FSB_CPURSTB while PWROK (PCIRST# from the ICH) is asserted and for approximately 1 ms after RSTINB is de-asserted. The FSB_CPURSTB allows the processors to begin execution in a known state.
FSB_DBSYB	I/O GTL+	**Data Bus Busy:** This signal is used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
FSB_DEFERB	O GTL+	**Defer:** This signal indicates that the (G)MCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.

Signal Name	Type	Description
FSB_DINVB_3:0	I/O GTL+ 4x	**Dynamic Bus Inversion:** These signals are driven along with the FSB_DB_63:0 signals. They indicate if the associated signals are inverted. FSB_DINVB_3:0 are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16 bit group never exceeds 8. **FSB_DINVB_x** **Data Bits** FSB_DINVB_3 FSB_DB_63:48 FSB_DINVB_2 FSB_DB_47:32 FSB_DINVB_1 FSB_DB_31:16 FSB_DINVB_0 FSB_DB_15:0
FSB_DRDYB	I/O GTL+	**Data Ready:** This signal is asserted for each cycle that data is transferred.
FSB_AB_35:3	I/O GTL+ 2x	**Host Address Bus:** FSB_AB_35:3 connect to the processor address bus. During processor cycles, FSB_AB_35:3 are inputs. The (G)MCH drives FSB_AB_35:3 during snoop cycles on behalf of DMI and PCI-Express-G initiators. FSB_AB_35:3 are transferred at 2x rate. Note that the address is inverted on the processor bus. The values stored in the POC register are driven in these signals by the (G)MCH between PWROK assertion and FSB_CPURSTB de-assertion to allow processor configuration.
FSB_ADSTBB_1:0	I/O GTL+ 2x	**Host Address Strobe:** The source synchronous strobes are used to transfer FSB_AB_31:3 and FSB_REQB_4:0 at the 2x transfer rate. **Strobe** **Address Bits** FSB_ADSTBB_0 FSB_AB_16:3, FSB_REQB_4:0 FSB_ADSTBB_1 FSB_AB_31:17
FSB_DB_63:0	I/O GTL+ 4x	**Host Data:** These signals are connected to the processor data bus. Data on FSB_DB_63:0 is transferred at a 4x rate. Note that the data signals may be inverted on the processor bus, depending on the FSB_DINVB_3:0 signals.

Signal Name	Type	Description
FSB_DSTBPB_3:0 FSB_DSTBNB_3:0	I/O GTL+ 4x	**Differential Host Data Strobes:** The differential source synchronous strobes used to transfer FSB_DB_63:0 and FSB_DINVB_3:0 at the 4x transfer rate. These signals are named this way because they are not level sensitive. Data is captured on the falling edge of both strobes. Hence, they are pseudo-differential, and not true differential. **Strobe** — **Data Bits** FSB_DSTBPB_2, FSB_DSTBNB_2 — FSB_DB_63:48, HDINVB_3 FSB_DSTBPB_2, FSB_DSTBNB_2 — FSB_DB_47:32, HDINVB_2 FSB_DSTBPB_1, FSB_DSTBNB_1 — FSB_DB_31:16, HDINVB_1 FSB_DSTBPB_0, FSB_DSTBNB_0 — FSB_DB_15:0, HDINVB_0
FSB_HITB	I/O GTL+	**Hit:** This signal indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with FSB_HITMB by the target to extend the snoop window.
FSB_HITMB	I/O GTL+	**Hit Modified:** This signal indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with FSB_HITB to extend the snoop window.
FSB_LOCKB	I GTL+	**Host Lock:** All processor bus cycles sampled with the assertion of FSB_LOCKB and FSB_ADSB, until the negation of FSB_LOCKB must be atomic (i.e., *no DMI or PCI-Express access* to DRAM are allowed when FSB_LOCKB is asserted by the processor).
FSB_REQB_4:0	I/O GTL+ 2x	**Host Request Command:** These signals define the attributes of the request. FSB_REQB_4:0 are transferred at 2x rate. Asserted by the requesting agent during both halves of Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type. The transactions supported by the (G)MCH Host Bridge are defined in the Host Interface section of this document.
FSB_TRDYB	O GTL+	**Host Target Ready:** This signal indicates that the target of the processor transaction is able to enter the data transfer phase.

Signal Name	Type	Description
FSB_RSB_2:0	O GTL+	**Response Signals:** These signals indicate type of response according as shown below: 000 = Idle state 001 = Retry response 010 = Deferred response 011 = Reserved (not driven by (G)MCH) 100 = Hard Failure (not driven by (G)MCH) 101 = No data response 110 = Implicit Writeback 111 = Normal data response
FSB_RCOMP	I/O A	**Host RCOMP:** This signal is used to calibrate the Host GTL+ I/O buffers. This signal is powered by the Host Interface termination rail (V_{TT}). Connects to FSB_XRCOMP1IN in the package.
FSB_SCOMP	I/O A	**Slew Rate Compensation:** This signal provides compensation for the Host Interface for Rising edges
FSB_SCOMPB	I/O A	**Slew Rate Compensation:** This signal provides compensation for the Host Interface for falling edges
FSB_SWING	I/O A	**Host Voltage Swing:** These signals provide reference voltages used by the FSB RCOMP circuits. FSB_SWING is used for the signals handled by FSB_RCOMP.
FSB_DVREF	I/O A	**Host Reference Voltage:** Reference voltage input for the Data signals of the Host GTL interface.
FSB_ACCVREF	I/O A	**Host Reference Voltage**: Reference voltage input for the Address, signals of the Host GTL interface.

2.2 System Memory (DDR2/DDR3) Channel A Interface Signals

Note: DDR3 is only supported on the 82G33 GMCH and 82P35 MCH components.

Signal Name	Type	Description
DDR_A_CK_5:0	O SSTL-1.8/1.5	**SDRAM Differential Clocks** • DDR2: Three per DIMM (5:0) • DDR3: Two per DIMM (3:0)
DDR_A_CKB_5:0	O SSTL-1.8/1.5	**SDRAM Inverted Differential Clocks** • DDR2: Three per DIMM (5:0) • DDR3: Two per DIMM (3:0)
DDR_A_CSB_3:0	O SSTL-1.8/1.5	**DDR2/DDR3 Device Rank 3, 2, and 0 chip selects** **DDR2 Device Rank 1 chip select**
DDR3_A_CSB_1	O SSTL-1.5	**DDR3 Device Rank 1 Chip Select**
DDR_A_CKE_3:0	O SSTL-1.8/1.5	**DDR2/DDR3 Clock Enable** (1 per Device Rank)
DDR_A_ODT_3:0	O SSTL-1.8/1.5	**DDR2/DDR3 On Die Termination** (1 per Device Rank)
DDR_A_MA_14:1	O SSTL-1.8/1.5	**DDR2/DDR3 Address Signals 14:1**
DDR_A_MA_0	O SSTL-1.8	**DDR2 Address Signals 0**
DDR3_A_MA_0	O SSTL-1.5	**DDR3 Address Signal 0**
DDR_A_BS_2:0	O SSTL-1.8/1.5	**DDR2/DDR3 Bank Select**
DDR_A_RASB	O SSTL-1.8/1.5	**DDR2/DDR3 RAS signal**
DDR_A_CASB	O SSTL-1.8/1.5	**DDR2/DDR3 CAS signal**
DDR_A_WEB	O SSTL-1.8	**DDR2 Write Enable signal**
DDR3_A_WEB	O SSTL-1.5	**DDR3 Write Enable signal**
DDR_A_DQ_63:0	I/O SSTL-1.8/1.5	**DDR2/DDR3 Data Lines**
DDR_A_DM_7:0	O SSTL-1.8/1.5	**DDR2/DDR3 Data Mask**
DDR_A_DQS_7:0	I/O SSTL-1.8/1.5	**DDR2/DDR3 Data Strobes**
DDR_A_DQSB_7:0	I/O SSTL-1.8/1.5	**DDR2/DDR3 Data Strobe Complements**

2.3 System Memory (DDR2/DDR3) Channel B Interface Signals

Note: DDR3 is only supported on the 82G33 GMCH and 82P35 MCH components.

Signal Name	Type	Description
DDR_B_CK_5:0	O SSTL-1.8/1.5	**SDRAM Differential Clocks** • DDR2: Three per DIMM (5:0) • DDR3: Two per DIMM (3:0)
DDR_B_CKB_5:0	O SSTL-1.8/1.5	**SDRAM Inverted Differential Clocks** • DDR2: Three per DIMM (5:0) • DDR3: Two per DIMM (3:0)
DDR_B_CSB_3:0	O SSTL-1.8/1.5	**DDR2/DDR3 Chip Select** (1 per Device Rank)
DDR_B_CKE_3:0	O SSTL-1.8/1.5	**DDR2/DDR3 Clock Enable** (1 per Device Rank)
DDR_B_ODT_2:0	O SSTL-1.8/1.5	**DDR2/DDR3 Device Rank 2, 1, and 0 On Die Termination**
DDR_B_ODT_3	O SSTL-1.8	**DDR2 Device Rank 3 On Die Termination**
DDR3_B_ODT_3	O SSTL-1.5	**DDR3 Device Rank 3 On Die Termination**
DDR_B_MA_14:0	O SSTL-1.8/1.5	**DDR2/DDR3 Address Signals 14:0**
DDR_B_BS_2:0	O SSTL-1.8/1.5	**DDR2/DDR3 Bank Select**
DDR_B_RASB	O SSTL-1.8/1.5	**DDR2/DDR3 RAS signal**
DDR_B_CASB	O SSTL-1.8/1.5	**DDR2/DDR3 CAS signal**
DDR_B_WEB	O SSTL-1.8/1.5	**DDR2/DDR3 Write Enable**
DDR_B_DQ_63:0	I/O SSTL-1.8/1.5	**DDR2/DDR3 Data Lines**
DDR_B_DM_7:0	O SSTL-1.8/1.5	**DDR2/DDR3 Data Mask**
DDR_B_DQS_7:0	I/O SSTL-1.8/1.5	**DDR2/DDR3 Data Strobes**
DDR_B_DQSB_7:0	I/O SSTL-1.8/1.5	**DDR2/DDR3 Data Strobe Complements**

2.4 System Memory DDR2/DDR3 Miscellaneous Signals

Note: DDR3 is only supported on the 82G33 GMCH and 82P35 MCH components.

Signal Name	Type	Description
DDR_RCOMPXPD	I/O A	**DDR2/DDR3 Pull-down RCOMP**
DDR_RCOMPXPU	I/O A	**DDR2/DDR3 Pull-up RCOMP**
DDR_RCOMPYPD	I/O A	**DDR2/DDR3 Pull-down RCOMP**
DDR_RCOMPYPU	I/O A	**DDR2/DDR3 Pull-up RCOMP**
DDR_VREF	I A	**DDR2/DDR3 Reference Voltage**
DDR3_DRAM_PWROK	I	**DDR3 VCC_DDR Power OK**
DDR3_DRAMRSTB	O SSTL-1.5	**DDR3 Reset**

2.5 PCI Express* Interface Signals

Signal Name	Type	Description
PEG_RXN_15:0 PEG_RXP_15:0	I PCI Express*	**PCI Express Receive Differential Pair**
PEG_TXN_15:0 PEG_TXP_15:0	O PCI Express*	**PCI Express Transmit Differential Pair**
EXP_COMPO	O A	**PCI Express Output Current Compensation**
EXP_COMPI	I A	**PCI Express Input Current Compensation**

2.6 Controller Link Interface Signals

Signal Name	Type	Description
CL_DATA	I/O CMOS	Controller Link Bi Directional Data
CL_CLK	I/O CMOS	Controller Link Bi Directional Clock
CL_VREF	I CMOS	Controller Link External reference voltage
CL_RSTB	I/O CMOS	Controller Link reset Active low (bi-direct)

2.7 Analog Display Signals (Intel® 82Q33, GMCH, 82Q33 GMCH, and 82G33 GMCH Only)

Signal Name	Type	Description
CRT_RED	O A	**RED Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm routing impedance, but the terminating resistor to ground will be 75 ohms (e.g., 75 ohm resistor on the board, in parallel with a 75 ohm CRT load).
CRT_REDB	O A	**RED# Analog Output:** This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
CRT_GREEN	O A	**GREEN Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm routing impedance, but the terminating resistor to ground will be 75 ohms (e.g., 75 ohm resistor on the board, in parallel with a 75 ohm CRT load).
CRT_GREENB	O A	**GREEN# Analog Output:** This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
CRT_BLUE	O A	**BLUE Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC. The DAC is designed for a 37.5 ohm routing impedance, but the terminating resistor to ground will be 75 ohms (e.g., 75 ohm resistor on the board, in parallel with a 75 ohm CRT load).
CRT_BLUEB	O A	**BLUE# Analog Output:** This signal is an analog video output from the internal color palette DAC. It should be shorted to the ground plane.
CRT_IREF	I/O A	**Resistor Set:** Set point resistor for the internal color palette DAC.
CRT_HSYNC	O HVCMOS	**CRT Horizontal Synchronization:** This signal is used as the horizontal sync (polarity is programmable) or “sync interval”, 3.3 V output
CRT_VSYNC	O HVCMOS	**CRT Vertical Synchronization:** This signal is used as the vertical sync (polarity is programmable) 3.3 V output.
CRT_DDC_CLK	I/O COD	**Monitor Control Clock:** This signal may be used as the DDC_CLK for a secondary multiplexed digital display connector.
CRT_DDC_DATA	I/O COD	**Monitor Control Data:** This signal may be used as the DDC_Data for a secondary multiplexed digital display connector.

2.8 Clocks, Reset, and Miscellaneous

Signal Name	Type	Description
HPL_CLKINP HPL_CLKINN	I HCSL	**Differential Host Clock In:** These pins receive a differential host clock from the external clock synthesizer. This clock is used by all of the (G)MCH logic that is in the Host clock domain.
EXP_CLKINP EXP_CLKINN	I HCSL	**Differential PCI-Express Clock In:** These pins receive a differential 100 MHZ Serial Reference clock from the external clock synthesizer. This clock is used to generate the clocks necessary for the support of PCI-Express and DMI.
DPL_REFCLKINN DPL_REFCLKINP	I HCSL	**Display PLL Differential Clock In**
RSTINB	I HVIN	**Reset In:** When asserted, this signal will asynchronously reset the (G)MCH logic. This signal is connected to the PCIRST# output of the ICH9. All PCI-Express Graphics Attach output signals and DMI output signals will also tri-state compliant to PCI Express Rev 1.0 specification. This input should have a Schmitt trigger to avoid spurious resets. This signal is required to be 3.3 V tolerant.
CL_PWROK	I/O CMOS	**CL Power OK:** When asserted, CL_PWROK is an indication to the (G)MCH that 1.25 V VCC_CL power supply (Manageability well) has been stable for at least 10 us.
EXP_SLR	I CMOS	**PCI Express* Static Lane Reversal/Form Factor Selection:** (G)MCH's PCI Express lane numbers are reversed to differentiate BTX and ATX form factors. 0 = (G)MCH PCI Express lane numbers are reversed (BTX) 1 = Normal operation (ATX)
TCEN	I CMOS	**TLS Confidentiality Enable.** Enable/disable TLS Confidentiality. This signal has an internal pull-up. 0 = TLS Confidentiality is disabled. 1 = TLS Confidentiality is enabled.
BSEL2 BSEL1 BSEL0	I CMOS	**Bus Speed Select:** At the assertion of PWROK, the value sampled on these pins determines the expected frequency of the bus. Theses pins must also be routed to probe points or to the XDP connector when applicable.
MTYPE	I CMOS	**Memory Type:** This signal determines DDR2 or DDR3 board 0 = DDR3 (82G33 and 82P35 (G)MCH Only) 1 = DDR2

Signal Name	Type	Description
EXP_EN	I CMOS	**Concurrent PCI Express Port Enable:** This signal selects Concurrent SDVO and PCI Express 0 = Only SDVO or PCI Express is operational. 1 = Both SDVO and PCI Express are operating simultaneously via the PCI Express port. **NOTES:** For the 82P35 MCH, this signal should be pulled low.
PWROK	I/O HVIN	**Power OK:** When asserted, PWROK is an indication to the (G)MCH that core power has been stable for at least 10 us.
ICH_SYNCB	O HVCMOS	**ICH Sync:** Maintains synchronization between (G)MCH and ICH9. This signal is connected to the MCH_SYNC# signal on the ICH.
ALLZTEST/ XORTEST	I/O CMOS	**All Z Test:** ALLZTEST is used for chipset Bed of Nails testing to execute All Z Test. **XOR Chain Test:** XORTEST is used for Chipset Bed of Nails testing to execute XOR Chain Test. **XORTEST (Ball F20) / ALLZTEST (Ball K20) / Description** 0 / 0 / Reserved 0 / 1 / XORTEST. Used for chipset Bed of Nails Testing to execute XOR Chain Test. 1 / 0 / All pins tri-stated. Used for chipset testing. 1 / 1 / Normal
TEST[2:0]	I/O A	**In Circuit Test:** These pins should be connected to test points on the motherboard. They are internally shorted to the package ground and can be used to determine if the corner balls on the (G)MCH are correctly soldered down to the motherboard. These pins should NOT connect to ground on the motherboard. If TEST[2:0] are not going to be used, they should be left as no connects.

2.9 Direct Media Interface

Signal Name	Type	Description
DMI_RXP_3:0 DMI_RXN_3:0	I DMI	**Direct Media Interface:** Receive differential pair (RX). These signals are the (G)MCH-ICH9 serial interface input.
DMI_TXP_3:0 DMI_TXN_3:0	O DMI	**Direct Media Interface:** Transmit differential pair (TX). These signals are the (G)MCH-ICH9 serial interface output.

2.10 Serial DVO Interface (Intel® 82Q35, 82Q33, 82G33 GMCH Only)

Most of these signals are multiplexed with PCI Express signals. SDVO_CTTCLK and SDVO_CTRLDATA are the only unmultiplexed signals on the SDVO interface. SDVO is mapped to lanes 0-7 or lanes 15-8 of the PEG port depending on the PCI Express Static Lane Reversal and SDVO/PCI Express Coexistence straps. The lower 8 lanes are used when **both** straps are either asserted or not asserted. Otherwise, the upper 8 lanes are used.

Signal Name	Type	Description
SDVOB_CLK-	O PCI Express*	**Serial Digital Video Channel B Clock Complement**
SDVOB_CLK+	O PCI Express*	**Serial Digital Video Channel B Clock**
SDVOB_RED-	O PCI Express*	**Serial Digital Video Channel C Red Complement**
SDVOB_RED+	O PCI Express*	**Serial Digital Video Channel C Red**
SDVOB_GREEN-	O PCI Express*	**Serial Digital Video Channel B Green Complement**
SDVOBGREEN+	O PCI Express*	**Serial Digital Video Channel B Green**
SDVOB_BLUE-	O PCI Express*	**Serial Digital Video Channel B Blue Complement**
SDVOB_BLUE+	O PCI Express*	**Serial Digital Video Channel B Blue**
SDVOC_RED-	O PCI Express*	**Serial Digital Video Channel C Red Complement**
SDVOC_RED+	O PCI Express*	**Serial Digital Video Channel C Red Channel B Alpha**
SDVOC_GREEN-	O PCI Express*	**Serial Digital Video Channel C Green Complement**
SDVOC_GREEN+	O PCI Express*	**Serial Digital Video Channel C Green**
SDVOC_BLUE-	O PCI Express*	**Serial Digital Video Channel C Blue Complement**

Signal Name	Type	Description
SDVOC_BLUE+	O PCI Express*	**Serial Digital Video Channel C Blue**
SDVOC_CLK-	O PCI Express*	**Serial Digital Video Channel C Clock Complement**
SDVOC_CLK+	O PCI Express*	**Serial Digital Video Channel C Clock**
SDVO_TVCLKIN-	I PCI Express*	**Serial Digital Video TVOUT Synchronization Clock Complement**
SDVO_TVCLKIN+	I PCI Express*	**Serial Digital Video TVOUT Synchronization Clock**
SDVOB_INT-	I PCI Express*	**Serial Digital Video Input Interrupt Complement**
SDVOB_INT+	I PCI Express*	**Serial Digital Video Input Interrupt**
SDVOC_INT-	I PCI Express*	**Serial Digital Video Input Interrupt Complement**
SDVOC_INT+	I PCI Express*	**Serial Digital Video Input Interrupt**
SDVO_STALL-	I PCI Express*	**Serial Digital Video Field Stall Complement**
SDVO_STALL+	I PCI Express*	**Serial Digital Video Field Stall**
SDVO_CTRLCLK	I/O COD	**Serial Digital Video Device Control Clock**
SDVO_CTRLDATA	I/O COD	**Serial Digital Video Device Control Data**

NOTE: Table 2-1 shows the mapping of SDVO signals to the PCI Express* lanes in the various possible configurations as determined by the strapping configuration. Note that slot-reversed configurations do not apply to the Integrated-graphics only variants.

Table 2-1. SDVO/PCI Express* Signal Mapping

SDVO Signal	Configuration-wise Mapping			
	SDVO Only – Normal	SDVO Only – Reversed	Concurrent SDVO and PCI Express* – Normal	Concurrent SDVO and PCI Express* – Reversed
SDVOB_RED#	PEG_TXN0	PEG_TXN15	PEG_TXN15	PEG_TXN0
SDVOB_RED	PEG_TXP0	PEG_TXP15	PEG_TXP15	PEG_TXP0
SDVOB_GREEN#	PEG_TXN1	PEG_TXN14	PEG_TXN14	PEG_TXN1
SDVOB_GREEN	PEG_TXP1	PEG_TXP14	PEG_TXP14	PEG_TXP1
SDVOB_BLUE#	PEG_TXN2	PEG_TXN13	PEG_TXN13	PEG_TXN2
SDVOB_BLUE	PEG_TXP2	PEG_TXP13	PEG_TXP13	PEG_TXP2
SDVOB_CLKN	PEG_TXN3	PEG_TXN12	PEG_TXN12	PEG_TXN3
SDVOB_CLKP	PEG_TXP3	PEG_TXP12	PEG_TXP12	PEG_TXP3
SDVOC_RED#	PEG_TXN4	PEG_TXN11	PEG_TXN11	PEG_TXN4
SDVOC_RED	PEG_TXP4	PEG_TXP11	PEG_TXP11	PEG_TXP4
SDVOC_GREEN#	PEG_TXN5	PEG_TXN10	PEG_TXN10	PEG_TXN5
SDVOC_GREEN	PEG_TXP5	PEG_TXP10	PEG_TXP10	PEG_TXP5
SDVOC_BLUE#	PEG_TXN6	PEG_TXN9	PEG_TXN9	PEG_TXN6
SDVOC_BLUE	PEG_TXP6	PEG_TXP9	PEG_TXP9	PEG_TXP6
SDVOC_CLKN	PEG_TXN7	PEG_TXN8	PEG_TXN8	PEG_TXN7
SDVOC_CLKP	PEG_TXP7	PEG_TXP8	PEG_TXP8	PEG_TXP7
SDVO_TVCLKIN#	PEG_RXN0	PEG_RXN15	PEG_RXN15	PEG_RXN0
SDVO_TVCLKIN	PEG_RXP0	PEG_RXP15	PEG_RXP15	PEG_RXP0
SDVOB_INT#	PEG_RXN1	PEG_RXN14	PEG_RXN14	PEG_RXN1
SDVOB_INT	PEG_RXP1	PEG_RXP14	PEG_RXP14	PEG_RXP1
SDVOC_INT#	PEG_RXN5	PEG_RXN10	PEG_RXN10	PEG_RXN5
SDVOC_INT	PEG_RXP5	PEG_RXP10	PEG_RXP10	PEG_RXP5
SDVO_FLDSTALL#	PEG_RXN2	PEG_RXN13	PEG_RXN13	PEG_RXN2
SDVO_FLDSTALL	PEG_RXP2	PEG_RXP13	PEG_RXP13	PEG_RXP2

2.11 Power and Grounds

Name	Voltage	Description
VCC	1.25 V	**Core Power**
VTT	1.05V/1.2 V	**Processor System Bus Power**
VCC_EXP	1.25 V	**PCI Express* and DMI Power**
VCC_DDR	1.8V/1.5V	**DDR2/DDR3 System Memory Power**
VCC_CKDDR	1.8V/1.5V	**DDR2/DDR3 System Clock Memory Power**
VCC3_3	3.3 V	**3.3 V CMOS Power**
VCCAPLL_EXP	1.25 V	**PCI Express PLL Analog Power**
VCCA_DPLLA	1.25 V	**Display PLL A Analog Power.**
VCCA_DPLLB	1.25 V	**Display PLL B Analog Power.**
VCCA_HPLL	1.25 V	**Host PLL Analog Power**
VCCA_MPL	1.25 V	**System Memory PLL Analog Power**
VCCA_DAC	3.3 V	**Display DAC Analog Power**
VCCD_CRT	1.5/1.8 V	**Display Digital Supply Power**
VCCDQ_CRT	1.5/1.8V	**CRTDAC Power**
VCC_CL	1.25 V	**Controller Link Aux Power**
VSS	0 V	**Ground**

§

3 System Address Map

The (G)MCH supports 64 GB (36 bit) of host address space and 64 KB+3 of addressable I/O space. There is a programmable memory address space under the 1 MB region that is divided into regions which can be individually controlled with programmable attributes such as Disable, Read/Write, Write Only, or Read Only. Attribute programming is described in the Register Description section. This section focuses on how the memory space is partitioned and what the separate memory regions are used for. I/O address space has a simpler mapping and is explained in Section 3.10.

Note: Address mapping information for the Integrated Graphics Device applies to the 82Q35, 82Q33, and 82G33 GMCH only. The 82P35 MCH does not have an IGD.

The (G)MCH supports PEG port upper pre-fetchable base/limit registers. This allows the PEG unit to claim IO accesses above 36 bit, complying with the PCI Express Specification. Addressing of greater than 8 GB is allowed on either the DMI Interface or PCI Express interface. The (G)MCH supports a maximum of 8 GB of DRAM. No DRAM memory will be accessible above 8 GB.

When running in internal graphics mode (82Q35/82Q33/82G33 GMCH only), writes to GMADR range linear range are supported. Write accesses to linear regions are supported from DMI only. Write accesses to tileX and tileY regions are not supported from DMI or the PEG port. GMADR read accesses are not supported from either DMI or PEG.

In the following sections, it is assumed that all of the compatibility memory ranges reside on the DMI Interface. The exception to this rule is VGA ranges, which may be mapped to PCI-Express, DMI, or to the internal graphics device (IGD). In the absence of more specific references, cycle descriptions referencing PCI should be interpreted as the DMI Interface/PCI, while cycle descriptions referencing PCI Express or IGD are related to the PCI Express bus or the internal graphics device respectively. The (G)MCH does not remap APIC or any other memory spaces above TOLUD (Top of Low Usable DRAM). The TOLUD register is set to the appropriate value by BIOS. The reclaim base/reclaim limit registers remap logical accesses bound for addresses above 4 GB onto physical addresses that fall within DRAM.

The Address Map includes a number of programmable ranges:

- Device 0
  - PXPEPBAR – Express port registers. Necessary for setting up VC1 as an isochronous channel using time based weighted round robin arbitration. (4 KB window)
  - MCHBAR – Memory mapped range for internal (G)MCH registers. For example, memory buffer register controls. (16 KB window)
  - PCIEXBAR – Flat memory-mapped address spaced to access device configuration registers. This mechanism can be used to access PCI configuration space (0-FFh) and Extended configuration space (100h–FFFh) for PCI Express devices. This enhanced configuration access mechanism is defined in the PCI Express specification. (64 MB, 128 MB, or 256 MB window).
  - DMIBAR –This window is used to access registers associated with the Direct Media Interface (DMI) register memory range. (4 KB window)
  - GGCGMS (82Q35/82Q33/82G33 GMCH only) – GMCH graphics control register, Graphics Mode Select. GGCGMS is used to select the amount of main memory that is pre-allocated to support the internal graphics device in VGA (non-linear) and Native (linear) modes.
    (0–256 MB options).
  - GGCGGMS (82Q35/82Q33/82G33 GMCH only) – GMCH graphics control register, GTT Graphics Memory Size. GGCGGMS is used to select the amount of main memory that is pre-allocated to support the Internal Graphics Translation Table. (0–2 MB options).
- Device 1
  - MBASE1/MLIMIT1 – PCI Express port non-prefetchable memory access window.
  - PMBASE1/PMLIMIT1 – PCI Express port prefetchable memory access window.
  - PMUBASE/PMULIMIT – PCI Express port upper prefetchable memory access window
  - IOBASE1/IOLIMIT1 – PCI Express port IO access window.
- Device 2, Function 0 (82Q35/82Q33/82G33 GMCH only)
  - MMADR – IGD registers and internal graphics instruction port. (512 KB window)
  - IOBAR – IO access window for internal graphics. Though this window address/data register pair, using I/O semantics, the IGD and internal graphics instruction port registers can be accessed. Note, this allows accessing the same registers as MMADR. In addition, the IOBAR can be used to issue writes to the GTTADR table.
  - GMADR – Internal graphics translation window. (128 MB, 256 MB or 512 MB window).
  - GTTADR – Internal graphics translation table location. (1 MB window). Note that the Base of GTT stolen Memory register (Device 0 A8) indicates the physical address base which is 1 MB aligned.
- Device 2, Function 1 (82Q35/82Q33/82G33 GMCH only)
  - MMADR – Function 1 IGD registers and internal graphics instruction port. (512 KB window)
- Device 3, Function 0
  - EPHECIBAR – Function 0 HECI memory-mapped registers.
    (16 B window)

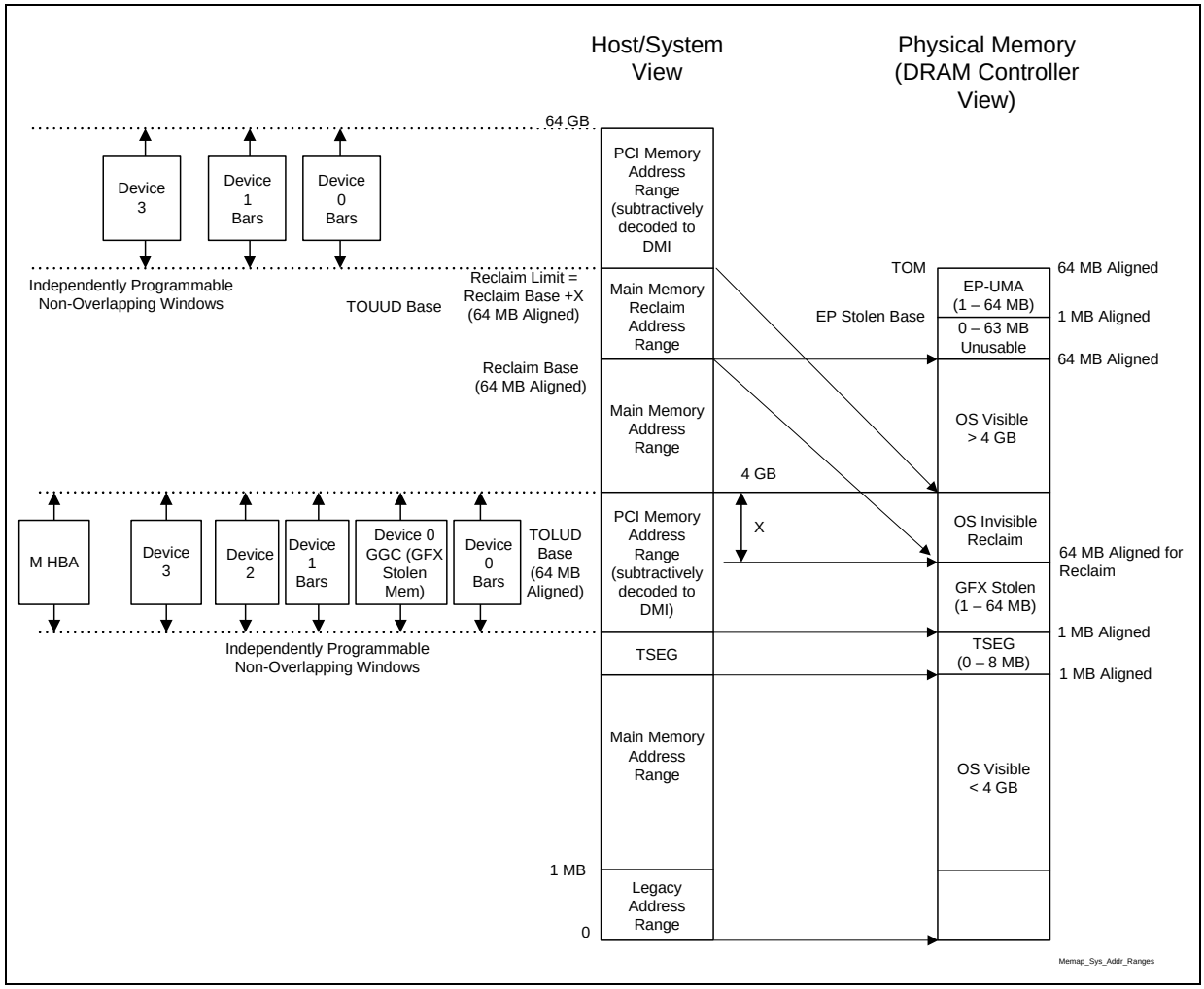
- MCHBAR
  - GFXVTBAR – Memory-mapped window to Graphics VT remap engine registers. (4 KB window)
  - DMIVC1BAR – Memory-mapped window to DMI VC1 VT remap engine registers. (4 KB window)
  - VTMEBAR – Memory-mapped window to ME VT remap engine registers (4 KB window)
  - VTDPVC0BAR – Memory-mapped window to PEG/DMI VC0 VT remap engine registers. (4 KB window)

The rules for the above programmable ranges are:

1. ALL of these ranges MUST be unique and NON-OVERLAPPING. It is the BIOS or system designers' responsibility to limit memory population so that adequate PCI, PCI Express, High BIOS, PCI Express Memory Mapped space, and APIC memory space can be allocated.
2. In the case of overlapping ranges with memory, the memory decode will be given priority. This is an Intel® TXT requirement. It is necessary to get Intel® TXT protection checks, avoiding potential attacks.
3. There are NO Hardware Interlocks to prevent problems in the case of overlapping ranges.
4. Accesses to overlapped ranges may produce indeterminate results.
5. The only peer-to-peer cycles allowed below the top of Low Usable memory (register TOLUD) are DMI Interface to PCI Express VGA range writes. Note that peer-to-peer cycles to the Internal Graphics VGA range are not supported.

Figure 3-1 represents system memory address map in a simplified form.

Figure 3-1. System Address Ranges



NOTE:

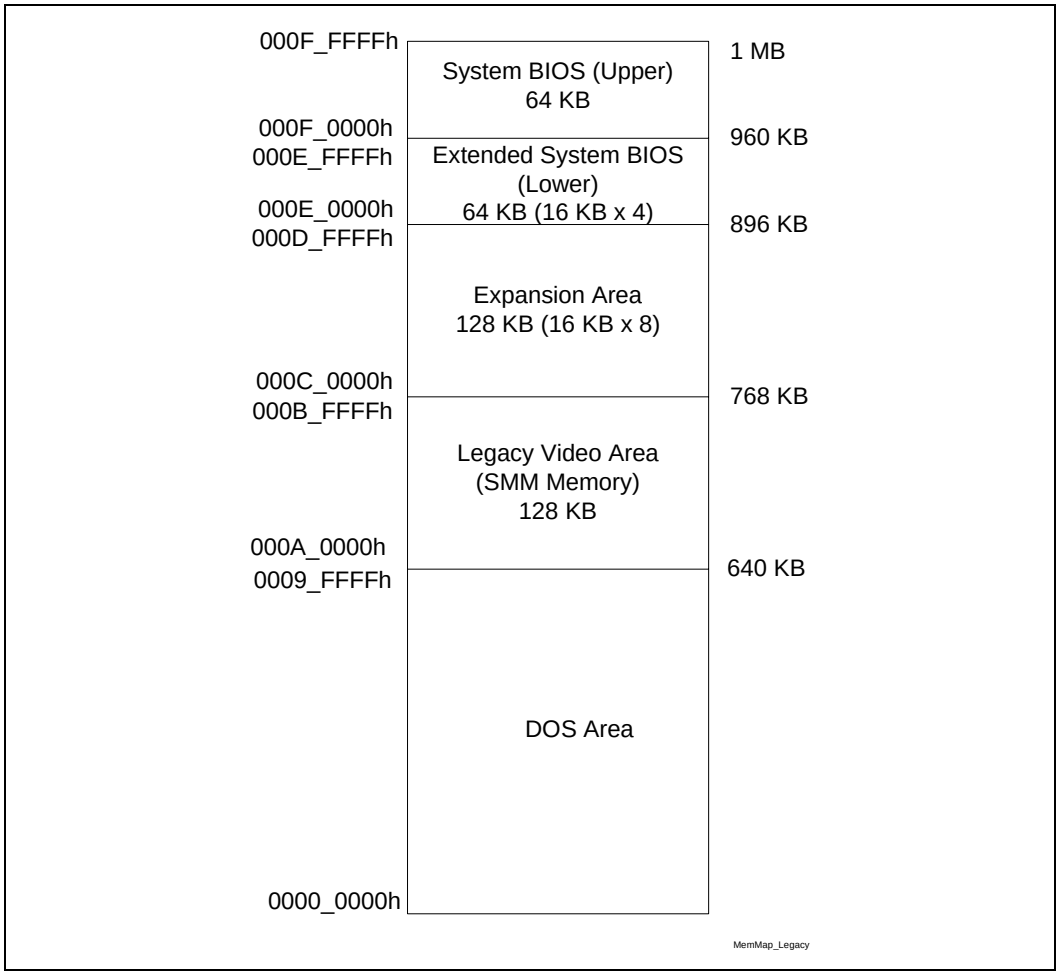
1. References to Internal Graphics Device address ranges are for the 82Q35/82Q33/82G33 GMCH only.

3.1 Legacy Address Range

This area is divided into the following address regions:

- 0 – 640 KB – DOS Area
- 640 – 768 KB – Legacy Video Buffer Area
- 768 – 896 KB in 16 KB sections (total of 8 sections) – Expansion Area
- 896 – 960 KB in 16 KB sections (total of 4 sections) – Extended System BIOS Area
- 960 KB – 1 MB Memory – System BIOS Area

Figure 3-2. DOS Legacy Address Range



3.1.1 DOS Range (0h – 9_FFFFh)

The DOS area is 640 KB (0000_0000h – 0009_FFFFh) in size and is always mapped to the main memory controlled by the (G)MCH.

3.1.2 Legacy Video Area (A_0000h – B_FFFFh)

The legacy 128 KB VGA memory range, frame buffer, (000A_0000h – 000B_FFFFh) can be mapped to IGD (Device 2), to PCI Express (Device 1), and/or to the DMI Interface. The appropriate mapping depends on which devices are enabled and the programming of the VGA steering bits. Based on the VGA steering bits, priority for VGA mapping is constant. The (G)MCH always decodes internally mapped devices first. Internal to the GMCH, decode precedence is always given to IGD. The (G)MCH always positively decodes internally mapped devices, namely the IGD and PCI-Express. Subsequent decoding of regions mapped to PCI Express or the DMI Interface depends on the Legacy VGA configuration bits (VGA Enable and MDAP). This region is also the default for SMM space.

Compatible SMRAM Address Range (A_0000h – B_FFFFh)

When compatible SMM space is enabled, SMM-mode processor accesses to this range are routed to physical system DRAM at 000A 0000h – 000B FFFFh. Non-SMM-mode processor accesses to this range are considered to be to the Video Buffer Area as described above. PCI Express and DMI originated cycles to enabled SMM space are not allowed and are considered to be to the Video Buffer Area if IGD is not enabled as the VGA device. PCI Express and DMI initiated cycles are attempted as Peer cycles, and will master abort on PCI if no external VGA device claims them.

Monochrome Adapter (MDA) Range (B_0000h – B_7FFFh)

Legacy support requires the ability to have a second graphics controller (monochrome) in the system. Accesses in the standard VGA range are forwarded to IGD, PCI Express, or the DMI Interface (depending on configuration bits). Since the monochrome adapter may be mapped to anyone of these devices, the (G)MCH must decode cycles in the MDA range (000B_0000h – 000B_7FFFh) and forward either to IGD, PCI Express, or the DMI Interface. This capability is controlled by a VGA steering bits and the legacy configuration bit (MDAP bit). In addition to the memory range B0000h to B7FFFh, the (G)MCH decodes I/O cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3BAh and 3BFh and forwards them to the either IGD, PCI-Express, and/or the DMI Interface.

PEG 16-bit VGA Decode

The *PCI to PCI Bridge Architecture Specification Revision 1.2* requires that 16-bit VGA decode be a feature.

3.1.3 Expansion Area (C_0000h – D_FFFFh)

This 128 KB ISA Expansion region (000C_0000h – 000D_FFFFh) is divided into eight 16 KB segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through (G)MCH and are subtractive decoded to ISA space. Memory that is disabled is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 3-1. Expansion Area Memory Segments

Memory Segments	Attributes	Comments
0C0000h – 0C3FFFh	WE RE	Add-on BIOS
0C4000h – 0C7FFFh	WE RE	Add-on BIOS
0C8000h – 0CBFFFh	WE RE	Add-on BIOS
0CC000h – 0CFFFFh	WE RE	Add-on BIOS
0D0000hH – 0D3FFFh	WE RE	Add-on BIOS
0D4000h – 0D7FFFh	WE RE	Add-on BIOS
0D8000h – 0DBFFFh	WE RE	Add-on BIOS
0DC000h – 0DFFFFh	WE RE	Add-on BIOS

3.1.4 Extended System BIOS Area (E_0000h-E_FFFFh)

This 64 KB area (000E_0000h – 000E_FFFFh) is divided into four 16 KB segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to DMI Interface. Typically, this area is used for RAM or ROM. Memory segments that are disabled are not remapped elsewhere.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 3-2. Extended System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
0E0000h – 0E3FFFh	WE RE	BIOS Extension
0E4000h – 0E7FFFh	WE RE	BIOS Extension
0E8000h – 0EBFFFh	WE RE	BIOS Extension
0EC000h – 0EFFFFh	WE RE	BIOS Extension

3.1.5 System BIOS Area (F_0000h-F_FFFFh)

This area is a single 64 KB segment (000F_0000h – 000F_FFFFh). This segment can be assigned read and write attributes. It is by default (after reset) read/write disabled and cycles are forwarded to DMI Interface. By manipulating the read/write attributes, the (G)MCH can “shadow” BIOS into the main DRAM. When disabled, this segment is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 3-3. System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
0F0000h – 0FFFFFh	WE RE	BIOS Area

3.1.6 PAM Memory Area Details

The 13 sections from 768 KB to 1 MB comprise what is also known as the PAM memory area.

The (G)MCH does not handle IWB (Implicit Write-Back) cycles targeting DMI. Since all memory residing on DMI should be set as non-cacheable, there will normally not be IWB cycles targeting DMI. However, DMI becomes the default target for processor and DMI originated accesses to disabled segments of the PAM region. If the MTRRs covering the PAM regions are set to WB or RD it is possible to get IWB cycles targeting DMI. This may occur for processor originated cycles and for DMI originated cycles to disabled PAM regions.

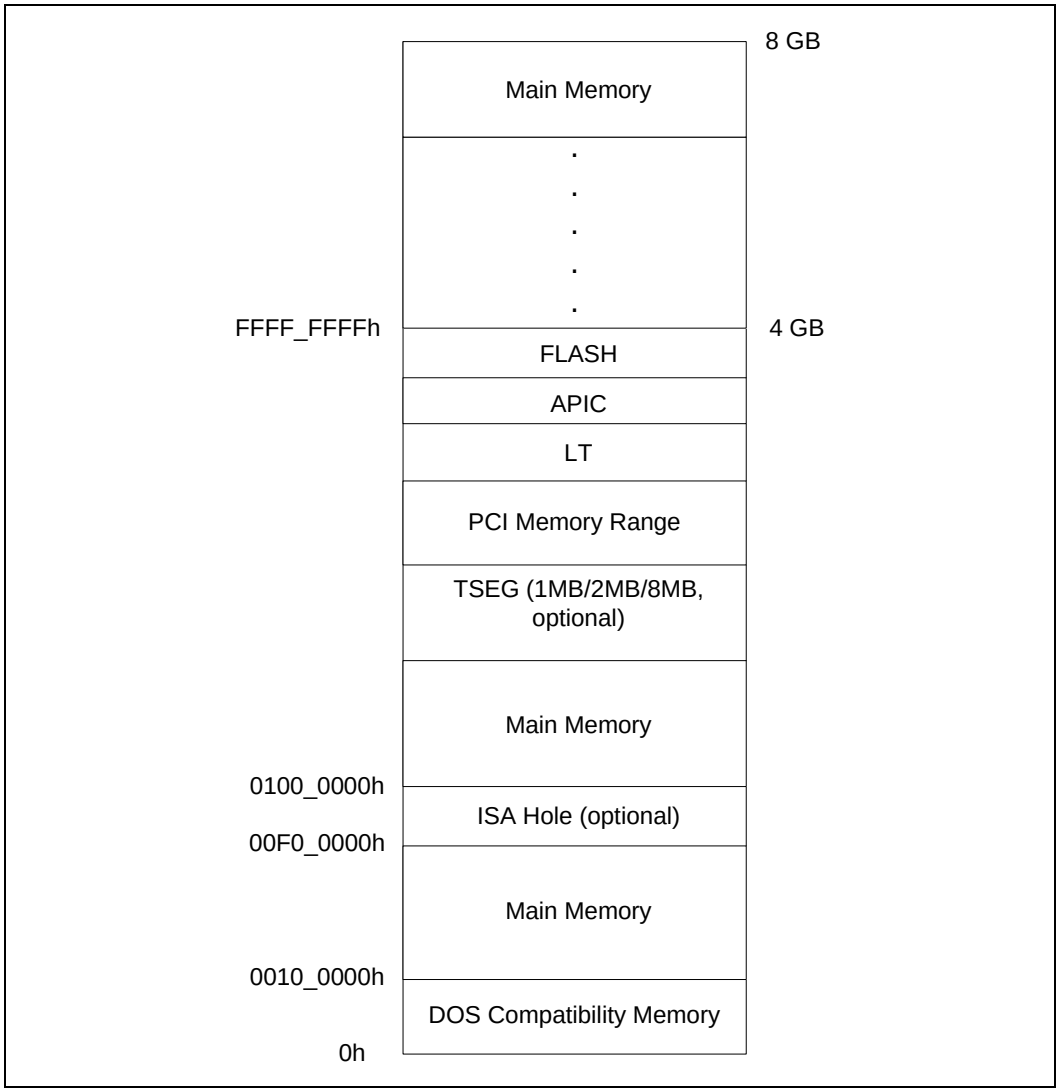
For example, say that a particular PAM region is set for “Read Disabled” and the MTRR associated with this region is set to WB. A DMI master generates a memory read targeting the PAM region. A snoop is generated on the FSB and the result is an IWB. Since the PAM region is “Read Disabled” the default target for the Memory Read becomes DMI. The IWB associated with this cycle will cause the (G)MCH to hang.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

3.2 Main Memory Address Range (1MB – TOLUD)

This address range extends from 1 MB to the top of Low Usable physical memory that is permitted to be accessible by the (G)MCH (as programmed in the TOLUD register). All accesses to addresses within this range will be forwarded by the (G)MCH to the DRAM unless it falls into the optional TSEG, optional ISA Hole, or optional IGD stolen VGA memory.

Figure 3-3. Main Memory Address Range



3.2.1 ISA Hole (15 MB-16 MB)

A hole can be created at 15 MB – 16 MB as controlled by the fixed hole enable in Device 0 space. Accesses within this hole are forwarded to the DMI Interface. The range of physical DRAM memory disabled by opening the hole is not remapped to the top of the memory – that physical DRAM space is not accessible. This 15 MB – 16 MB hole is an optionally enabled ISA hole.

Video accelerators originally used this hole. It is also used by validation and customer SV teams for some of their test cards. That is why it is being supported. There is no inherent BIOS request for the 15 MB – 16 MB window.

3.2.2 TSEG

TSEG is optionally 1 MB, 2 MB, or 8 MB in size. TSEG is below IGD stolen memory, which is at the top of Low Usable physical memory (TOLUD). SMM-mode processor accesses to enabled TSEG access the physical DRAM at the same address. Non-processor originated accesses are not allowed to SMM space. PCI Express, DMI, and Internal Graphics originated cycle to enabled SMM space are handled as invalid cycle type with reads and writes to location 0 and byte enables turned off for writes. When the extended SMRAM space is enabled, processor accesses to the TSEG range without SMM attribute or without WB attribute are also forwarded to memory as invalid accesses (see table 8). Non-SMM-mode Write Back cycles that target TSEG space are completed to DRAM for cache coherency. When SMM is enabled the maximum amount of memory available to the system is equal to the amount of physical DRAM minus the value in the TSEG register which is fixed at 1 MB, 2 MB, or 8 MB.

3.2.3 Pre-allocated Memory

Voids of physical addresses that are not accessible as general system memory and reside within system memory address range (< TOLUD) are created for SMM-mode, legacy VGA graphics compatibility, and GFX GTT stolen memory. **It is the responsibility of BIOS to properly initialize these regions**. The following table details the location and attributes of the regions. Enabling/Disabling these ranges are described in the (G)MCH Control Register Device 0 (GCC).

Table 3-4. Pre-allocated Memory Example for 64 MB DRAM, 1 MB VGA, 1 MB GTT stolen and 1 MB TSEG

Memory Segments	Attributes	Comments
0000_0000h – 03CF_FFFFh	R/W	Available System Memory 61 MB
03D0_0000h – 03DF_FFFFh	SMM Mode Only - processor Reads	TSEG Address Range & Pre-allocated Memory
03E0_0000h – 03EF_FFFFh	R/W	Pre-allocated Graphics VGA memory. 1 MB (or 4/8/16/32/64/128/256 MB) when IGD is enabled on the 82Q35/82Q33/82G33 GMCH.
03F0_0000h – 03FF_FFFFh	R/W	Pre-allocated Graphics GTT stolen memory. 1 MB (or 2 MB) when IGD is enabled on the 82Q35/82Q33/82G33 GMCH.

3.3 PCI Memory Address Range (TOLUD – 4GB)

This address range, from the top of low usable DRAM (TOLUD) to 4 GB is normally mapped to the DMI Interface.

Device 0 exceptions are:

- Addresses decoded to the Express port registers (PXPEPBAR)
- Addresses decoded to the memory mapped range for internal (G)MCH registers (MCHBAR)
- Addresses decoded to the flat memory-mapped address spaced to access device configuration registers (PCIEXBAR)
- Addresses decoded to the registers associated with the Direct Media Interface (DMI) register memory range. (DMIBAR)

With PCI Express port, there are two exceptions to this rule.

- Addresses decoded to the PCI Express Memory Window defined by the MBASE1 and MLIMIT1 registers are mapped to PCI Express.
- Addresses decoded to the PCI Express prefetchable Memory Window defined by the PMBASE1 and PMLIMIT1 registers are mapped to PCI Express.

In integrated graphics configurations, there are exceptions to this rule:

- Addresses decoded to the IGD registers and internal graphics instruction port (Function 0 MMADR, Function 1 MMADR)
- Addresses decode to the internal graphics translation window (GMADR)
- Addresses decode to the Internal graphics translation table (GTTADR)

In an Intel ME configuration, there are exceptions to this rule:

- Addresses decoded to the ME Keyboard and Text MMIO range (EPKTBAR)
- Addresses decoded to the ME HECI MMIO range (EPHECIBAR)
- Addresses decoded to the ME HECI2 MMIO range (EPHECI2BAR)

In a VT enable configuration, there are exceptions to this rule:

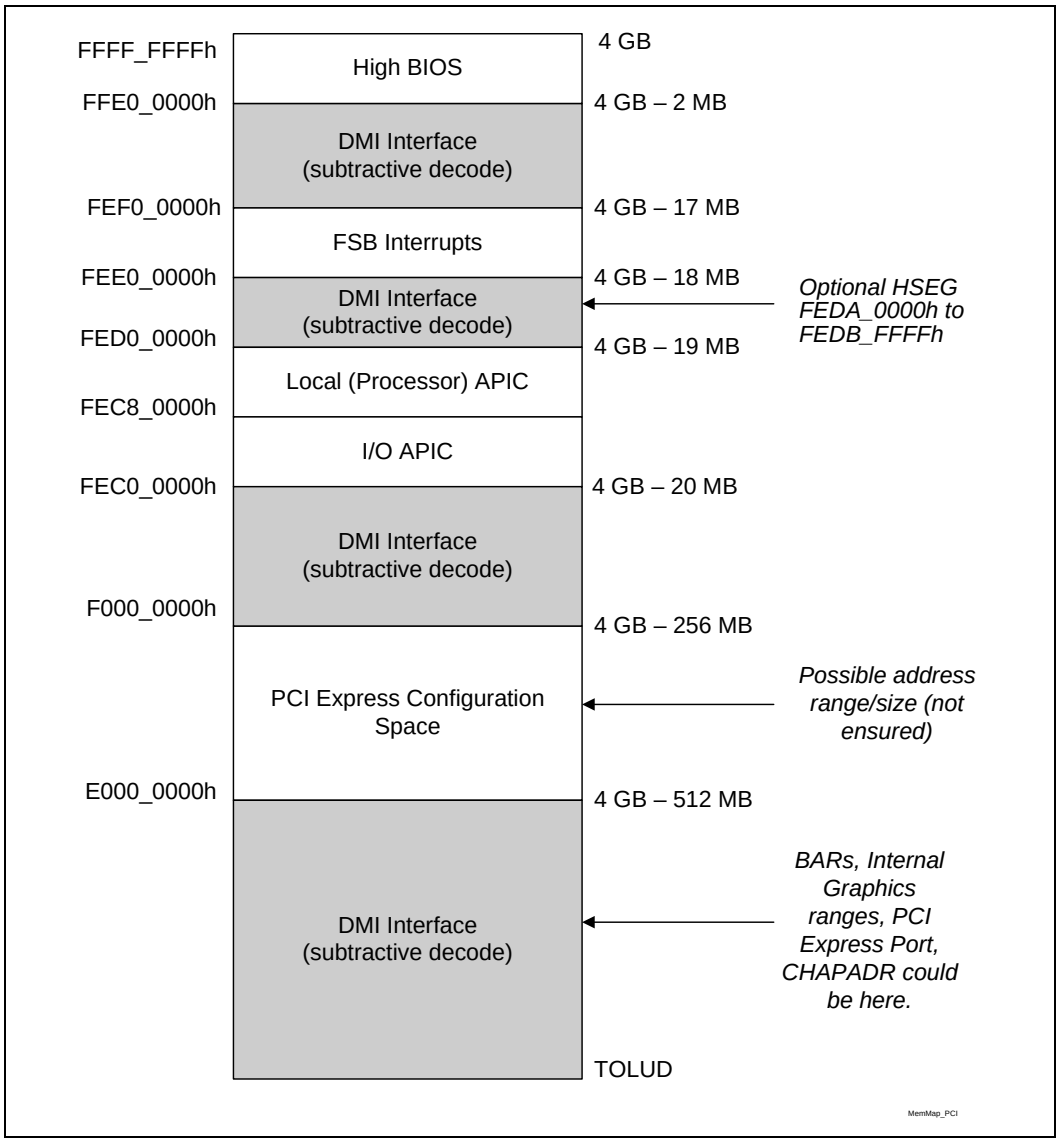
- Addresses decoded to the memory mapped window to Graphics VT remap engine registers (GFXVTBAR)
- Addresses decoded to the memory mapped window to DMI VC1 VT remap engine registers (DMIVC1BAR)
- Addresses decoded to the memory mapped window to ME VT remap engine registers (VTMEBAR)

Addresses decoded to the memory-mapped window to PEG/DMI VC0 VT remap engine registers (VTDPVC0BAR)

Some of the MMIO Bars may be mapped to this range or to the range above TOUUD.

There are sub-ranges within the PCI Memory address range defined as APIC Configuration Space, FSB Interrupt Space, and High BIOS Address Range. The exceptions listed above for internal graphics and the PCI Express ports ***MUST NOT*** *overlap with these ranges.*

Figure 3-4. PCI Memory Address Range



3.3.1 APIC Configuration Space (FEC0_0000h–FECF_FFFFh)

This range is reserved for APIC configuration space. The I/O APIC(s) usually reside in the ICH9 portion of the chipset, but may also exist as stand-alone components like PXH.

The IOAPIC spaces are used to communicate with IOAPIC interrupt controllers that may be populated in the system. Since it is difficult to relocate an interrupt controller using plug-and-play software, fixed address decode regions have been allocated for them. Processor accesses to the default IOAPIC region (FEC0_0000h to FEC7_FFFFh) are always forwarded to DMI.

The (G)MCH optionally supports additional I/O APICs behind the PCI Express "Graphics" port. When enabled via the PCI Express Configuration register (Device 1 Offset 200h), the PCI Express port will positively decode a subset of the APIC configuration space – specifically FEC8_0000h thru FECF_FFFFh. Memory request to this range would then be forwarded to the PCI Express port. This mode is intended for the entry Workstation/Server SKU of the (G)MCH, and would be disabled in typical Desktop systems. When disabled, any access within entire APIC Configuration space (FEC0_0000h to FECF_FFFFh) is forwarded to DMI.

3.3.2 HSEG (FEDA_0000h–FEDB_FFFFh)

This optional segment from FEDA_0000h to FEDB_FFFFh provides a remapping window to SMM Memory. It is sometimes called the High SMM memory space. SMM-mode processor accesses to the optionally enabled HSEG are remapped to 000A_0000h – 000B_FFFFh. Non-SMM-mode processor accesses to enabled HSEG are considered invalid and are terminated immediately on the FSB. The exceptions to this rule are Non-SMM-mode Write Back cycles which are remapped to SMM space to maintain cache coherency. PCI Express and DMI originated cycles to enabled SMM space are not allowed. Physical DRAM behind the HSEG transaction address is not remapped and is not accessible. All cacheline writes with WB attribute or Implicit write backs to the HSEG range are completed to DRAM like an SMM cycle.

3.3.3 FSB Interrupt Memory Space (FEE0_0000–FEEF_FFFF)

The FSB Interrupt space is the address used to deliver interrupts to the FSB. Any device on PCI Express or DMI may issue a Memory Write to 0FEEx_xxxxh. The (G)MCH will forward this Memory Write along with the data to the FSB as an Interrupt Message Transaction. The (G)MCH terminates the FSB transaction by providing the response and asserting HTRDYB. This memory write cycle does not go to DRAM.

3.3.4 High BIOS Area

The top 2 MB (FFE0_0000h – FFFF_FFFFh) of the PCI Memory Address Range is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The processor begins execution from the High BIOS after reset. This region is mapped to DMI Interface so that the upper subset of this region aliases to 16 MB – 256 KB range. The actual address space required for the BIOS is

less than 2 MB but the minimum processor MTRR range for this region is 2 MB so that full 2 MB must be considered.

3.4 Main Memory Address Space (4 GB to TOUUD)

The (G)MCH supports 36 bit addressing. The maximum main memory size supported is 8 GB total DRAM memory. A hole between TOLUD and 4 G occurs when main memory size approaches 4 GB or larger. As a result, TOM, and TOUUD registers and RECLAIMBASE/RECLAIMLIMIT registers become relevant.

The new reclaim configuration registers exist to reclaim lost main memory space. The greater than 32 bit reclaim handling will be handled similar to other (G)MCHs.

Upstream read and write accesses above 36-bit addressing will be treated as invalid cycles by PEG and DMI.

Top of Memory

The “Top of Memory” (TOM) register reflects the total amount of populated physical memory. This is NOT necessarily the highest main memory address (holes may exist in main memory address map due to addresses allocated for memory-mapped I/O above TOM). TOM is used to allocate the Intel Management Engine's stolen memory. The Intel ME stolen size register reflects the total amount of physical memory stolen by the Intel ME. The ME stolen memory is located at the top of physical memory. The ME stolen memory base is calculated by subtracting the amount of memory stolen by the Intel ME from TOM.

The Top of Upper Usable DRAM (TOUUD) register reflects the total amount of addressable DRAM. If reclaim is disabled, TOUUD will reflect TOM minus Intel ME stolen size. If reclaim is enabled, then it will reflect the reclaim limit. Also, the reclaim base will be the same as TOM minus ME stolen memory size to the nearest 64 MB alignment.

TOLUD register is restricted to 4 GB memory (A[31:20]), but the (G)MCH can support up to 16 GB, limited by DRAM pins. For physical memory greater than 4 GB, the TOUUD register helps identify the address range in between the 4 GB boundary and the top of physical memory. This identifies memory that can be directly accessed (including reclaim address calculation) which is useful for memory access indication, early path indication, and trusted read indication. When reclaim is enabled, TOLUD must be 64 MB aligned, but when reclaim is disabled, TOLUD can be 1 MB aligned.

C1DRB3 cannot be used directly to determine the effective size of memory as the values programmed in the DRBs depend on the memory mode (stacked, interleaved). The Reclaim Base/Limit registers also can not be used because reclaim can be disabled. The C0DRB3 register is used for memory channel identification (channel 0 vs. channel 1) in the case of stacked memory.

3.4.1 Memory Re-claim Background

The following are examples of Memory Mapped IO devices are typically located below 4 GB:

- High BIOS
- HSEG
- TSEG
- Graphics stolen
- XAPIC
- Local APIC
- FSB Interrupts
- Mbase/Mlimit
- Memory-mapped I/O space that supports only 32 B addressing

The (G)MCH provides the capability to re-claim the physical memory overlapped by the Memory Mapped IO logical address space. The (G)MCH re-maps physical memory from the Top of Low Memory (TOLUD) boundary up to the 4 GB boundary to an equivalent sized logical address range located just below the Intel ME's stolen memory.

3.4.2 Memory Reclaiming

An incoming address (referred to as a logical address) is checked to see if it falls in the memory re-map window. The bottom of the re-map window is defined by the value in the RECLAIMBASE register. The top of the re-map window is defined by the value in the RECLAIMLIMIT register. An address that falls within this window is reclaimed to the physical memory starting at the address defined by the TOLUD register. The TOLUD register must be 64 MB aligned when RECLAIM is enabled, but can be 1 MB aligned when reclaim is disabled.

3.5 PCI Express* Configuration Address Space

There is a device 0 register, PCIEXBAR, that defines the base address for the configuration space associated with all devices and functions that are potentially a part of the PCI Express root complex hierarchy. The size of this range is programmable for the (G)MCH. BIOS must assign this address range such that it will not conflict with any other address ranges. See Chapter 6 for more details.

3.6 PCI Express* Graphics Attach (PEG)

The (G)MCH can be programmed to direct memory accesses to the PCI Express interface when addresses are within either of two ranges specified via registers in (G)MCH's Device 1 configuration space.

- The first range is controlled via the Memory Base Register (MBASE) and Memory Limit Register (MLIMIT) registers.
- The second range is controlled via the Pre-fetchable Memory Base (PMBASE) and Pre-fetchable Memory Limit (PMLIMIT) registers.

Conceptually, address decoding for each range follows the same basic concept. The top 12 bits of the respective Memory Base and Memory Limit registers correspond to address bits A[31:20] of a memory address . For the purpose of address decoding, the (G)MCH assumes that address bits A[19:0] of the memory base are zero and that address bits A[19:0] of the memory limit address are FFFFFh. This forces each memory address range to be aligned to 1MB boundary and to have a size granularity of 1 MB.

The (G)MCH positively decodes memory accesses to PCI Express memory address space as defined by the following equations:

Memory_Base_Address ≤ Address ≤ Memory_Limit_Address

Prefetchable_Memory_Base_Address ≤ Address ≤ Prefetchable_Memory_Limit_Address

The window size is programmed by the plug-and-play configuration software. The window size depends on the size of memory claimed by the PCI Express device. Normally these ranges will reside above the Top-of-Low Usable-DRAM and below High BIOS and APIC address ranges. They MUST reside above the top of low memory (TOLUD) if they reside below 4 GB and MUST reside above top of upper memory (TOUUD) if they reside above 4 GB or they will steal physical DRAM memory space.

It is essential to support a separate Pre-fetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

Note that the (G)MCH Device 1 memory range registers described above are used to allocate memory address space for any PCI Express devices sitting on PCI Express that require such a window.

The PCICMD1 register can override the routing of memory accesses to PCI Express. In other words, the memory access enable bit must be set in the device 1 PCICMD1 register to enable the memory base/limit and pre-fetchable base/limit windows.

The upper PMUBASE1/PMULIMIT1 registers have been implemented for PCI Express Specification compliance. The (G)MCH locates MMIO space above 4 GB using these registers.

3.7 Graphics Memory Address Ranges (Intel® 82Q35, 82Q33, and 82G33 (G)MCH Only)

The (G)MCH can be programmed to direct memory accesses to IGD when addresses are within any of five ranges specified via registers in (G)MCH's Device 2 configuration space.

- The Memory Map Base Register (MMADR) is used to access graphics control registers.
- The Graphics Memory Aperture Base Register (GMADR) is used to access graphics memory allocated via the graphics translation table.
- The Graphics Translation Table Base Register (GTTADR) is used to access the translation table.

These ranges can reside above the Top-of-Low-DRAM and below High BIOS and APIC address ranges. They MUST reside above the top of memory (TOLUD) and below 4 GB so they do not steal any physical DRAM memory space.

GMADR is a Prefetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

3.8 System Management Mode (SMM)

System Management Mode uses main memory for System Management RAM (SMM RAM). The (G)MCH supports: Compatible SMRAM (C_SMRAM), High Segment (HSEG), and Top of Memory Segment (TSEG). System Management RAM space provides a memory area that is available for the SMI handlers and code and data storage. This memory resource is normally hidden from the system OS so that the processor has immediate access to this memory space upon entry to SMM. The (G)MCH provides three SMRAM options:

- Below 1 MB option that supports compatible SMI handlers.
- Above 1 MB option that allows new SMI handlers to execute with write-back cacheable SMRAM.
- Optional TSEG area of 1 MB, 2 MB, or 8 MB in size. For the 82Q35/82Q33/82G33, the TSEG area lies below IGD stolen memory.

The above 1 MB solutions require changes to compatible SMRAM handlers code to properly execute above 1 MB.

Note: DMI Interface and PCI Express masters are not allowed to access the SMM space.

3.8.1 SMM Space Definition

SMM space is defined by its **addressed** SMM space and its DRAM SMM space. The addressed SMM space is defined as the range of bus addresses used by the processor to access SMM space. DRAM SMM space is defined as the range of physical DRAM memory locations containing the SMM code. SMM space can be accessed at one of three transaction address ranges: Compatible, High and TSEG. The Compatible and TSEG SMM space is not remapped and therefore the addressed and DRAM SMM space is the same address range. Since the High SMM space is remapped the addressed and DRAM SMM space is a different address range. Note that the High DRAM space is the same as the Compatible Transaction Address space. Table 3-5 describes three unique address ranges.

Table 3-5. Pre-Allocated Memory Example for 64-MB DRAM, 1-MB VGA and 1-MB TSEG

SMM Space Enabled	Transaction Address Space	DRAM Space (DRAM)
Compatible	000A_0000h to 000B_FFFFh	000A_0000h to 000B_FFFFh
High	FEDA_0000h to FEDB_FFFFh	000A_0000h to 000B_FFFFh
TSEG	(TOLUD-STOLEN-TSEG) to TOLUD-STOLEN	(TOLUD-STOLEN-TSEG) to TOLUD-STOLEN

NOTES:
1. STOLEN memory is only for the 82Q35/82Q33/82G33 GMCH.

3.8.2 SMM Space Restrictions

If any of the following conditions are violated the results of SMM accesses are unpredictable and may cause the system to hang:

1. The Compatible SMM space **must not** be set-up as cacheable.
2. High or TSEG SMM transaction address space **must not** overlap address space assigned to system DRAM, or to any “PCI” devices (including DMI Interface, PCI-Express, and graphics devices). This is a BIOS responsibility.
3. Both D_OPEN and D_CLOSE **must not** be set to 1 at the same time.
4. When TSEG SMM space is enabled, the TSEG space **must not** be reported to the OS as available DRAM. This is a BIOS responsibility.
5. Any address translated through the GMADR TLB must not target DRAM from A_0000–F_FFFFh.

3.8.3 SMM Space Combinations

When High SMM is enabled (G_SMRAME=1 and H_SMRAM_EN=1) the Compatible SMM space is effectively disabled. Processor-originated accesses to the Compatible SMM space are forwarded to PCI Express if VGAEN=1 (also depends on MDAP); otherwise, they are forwarded to the DMI Interface. PCI Express and DMI Interface originated accesses are **never** allowed to access SMM space.

Table 3-6. SMM Space

Global Enable G_SMRAME	High Enable H_SMRAM_EN	TSEG Enable TSEG_EN	Compatible (C) Range	High (H) Range	TSEG (T) Range
0	X	X	Disable	Disable	Disable
1	0	0	Enable	Disable	Disable
1	0	1	Enable	Disable	Enable
1	1	0	Disabled	Enable	Disable
1	1	1	Disabled	Enable	Enable

3.8.4 SMM Control Combinations

The G_SMRAME bit provides a global enable for all SMM memory. The D_OPEN bit allows software to write to the SMM ranges without being in SMM mode. BIOS software can use this bit to initialize SMM code at powerup. The D_LCK bit limits the SMM range access to only SMM mode accesses. The D_CLS bit causes SMM (both CSEG and TSEG) data accesses to be forwarded to the DMI Interface or PCI Express. The SMM software can use this bit to write to video memory while running SMM code out of DRAM.

3.8.5 SMM Space Decode and Transaction Handling

Only the processor is allowed to access SMM space. PCI Express and DMI Interface originated transactions are not allowed to SMM space.

3.8.6 Processor WB Transaction to an Enabled SMM Address Space

Processor Writeback transactions (REQa[1]# = 0) to enabled SMM Address Space must be written to the associated SMM DRAM even though D_OPEN=0 and the transaction is not performed in SMM mode. This ensures SMM space cache coherency when cacheable extended SMM space is used.

3.8.7 SMM Access through GTT TLB (Intel® 82Q35, 82Q33, 82G33 GMCH Only)

Accesses through GTT TLB address translation to enabled SMM DRAM space are not allowed. Writes will be routed to memory address 000C_0000h with byte enables de-asserted and reads will be routed to memory address 000C_0000h. If a GTT TLB translated address hits enabled SMM DRAM space, an error is recorded.

PCI Express and DMI Interface originated accesses are **never** allowed to access SMM space directly or through the GTT TLB address translation. If a GTT TLB translated address hits enabled SMM DRAM space, an error is recorded.

PCI Express and DMI Interface write accesses through GMADR range will be snooped. Assesses to GMADR linear range (defined via fence registers) are supported. PCI Express and DMI Interface tileY and tileX writes to GMADR are not supported. If, when translated, the resulting physical address is to enabled SMM DRAM space, the request will be remapped to address 000C_0000h with de-asserted byte enables.

PCI Express and DMI Interface read accesses to the GMADR range are not supported therefore will have no address translation concerns. PCI Express and DMI Interface reads to GMADR will be remapped to address 000C_0000h. The read will complete with UR (unsupported request) completion status.

GTT fetches are always decoded (at fetch time) to ensure not in SMM (actually, anything above base of TSEG or 640 KB – 1 MB). Thus, they will be invalid and go to address 000C_0000h, but that is not specific to PCI Express or DMI; it applies to processor or internal graphics engines. Also, since the GMADR snoop would not be directly to the SMM space, there would not be a writeback to SMM. In fact, the writeback would also be invalid (because it uses the same translation) and go to address 000C_0000h.

3.9 Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be “shadowed” into (G)MCH DRAM memory. Typically this is done to allow ROM code to execute more rapidly out of main DRAM. ROM is used as a read-only during the copy process while DRAM at the same time is designated write-only. After copying, the DRAM is designated read-only so that ROM is shadowed. Processor bus transactions are routed accordingly.

3.10 I/O Address Space

The (G)MCH does not support the existence of any other I/O devices beside itself on the processor bus. The (G)MCH generates either DMI Interface or PCI Express bus cycles for all processor I/O accesses that it does not claim. Within the host bridge, the (G)MCH contains two internal registers in the processor I/O space: Configuration Address Register (CONFIG_ADDRESS) and the Configuration Data Register (CONFIG_DATA). These locations are used to implement configuration space access mechanism.

The processor allows 64 K+3 bytes to be addressed within the I/O space. The (G)MCH propagates the processor I/O address without any translation on to the destination bus and therefore provides addressability for 64K+3 byte locations. Note that the upper 3 locations can be accessed only during I/O address wrap-around when processor bus HAB_16 address signal is asserted. HAB_16 is asserted on the processor bus whenever an I/O access is made to 4 bytes from address 0FFFDh, 0FFFEh, or 0FFFFh. HAB_16 is also asserted when an I/O access is made to 2 bytes from address 0FFFFh.

A set of I/O accesses (other than ones used for configuration space access) are consumed by the internal graphics device if it is enabled. The mechanisms for internal graphics I/O decode and the associated control is explained later.

The I/O accesses (other than ones used for configuration space access) are forwarded normally to the DMI Interface bus unless they fall within the PCI Express I/O address range as defined by the mechanisms explained below. I/O writes are NOT posted. Memory writes to ICH9 or PCI Express are posted. The PCICMD1 register can disable the routing of I/O cycles to the PCI Express.

The (G)MCH responds to I/O cycles initiated on PCI Express or DMI with an UR status. Upstream I/O cycles and configuration cycles should never occur. If one does occur, the request will route as a read to memory address 000C_0000h so a completion is naturally generated (whether the original request was a read or write). The transaction will complete with an UR completion status.

For Pentium® 4 processors, I/O reads that lie within 8-byte boundaries but cross 4-byte boundaries are issued from the processor as 1 transaction. The (G)MCH breaks this into 2 separate transactions. I/O writes that lie within 8-byte boundaries but cross 4-byte boundaries are assumed to be split into 2 transactions by the processor.

3.10.1 PCI Express* I/O Address Mapping

The (G)MCH can be programmed to direct non-memory (I/O) accesses to the PCI Express bus interface when processor initiated I/O cycle addresses are within the PCI Express I/O address range. This range is controlled via the I/O Base Address (IOBASE) and I/O Limit Address (IOLIMIT) registers in (G)MCH Device 1 configuration space.

Address decoding for this range is based on the following concept. The top 4 bits of the respective I/O Base and I/O Limit registers correspond to address bits A[15:12] of an I/O address. For the purpose of address decoding, the (G)MCH assumes that lower 12 address bits A[11:0] of the I/O base are zero and that address bits A[11:0] of the I/O limit address are FFFh. This forces the I/O address range alignment to 4 KB boundary and produces a size granularity of 4 KB.

The (G)MCH positively decodes I/O accesses to PCI Express I/O address space as defined by the following equation:

$$I/O\_Base\_Address \leq Processor\ I/O\ Cycle\ Address \leq I/O\_Limit\_Address$$

The effective size of the range is programmed by the plug-and-play configuration software and it depends on the size of I/O space claimed by the PCI Express device.

The (G)MCH also forwards accesses to the Legacy VGA I/O ranges according to the settings in the Device 1 configuration registers BCTRL (VGA Enable) and PCICMD1

(IOAE1), unless a second adapter (monochrome) is present on the DMI Interface/PCI (or ISA). The presence of a second graphics adapter is determined by the MDAP configuration bit. When MDAP is set, the (G)MCH will decode legacy monochrome I/O ranges and forward them to the DMI Interface. The IO ranges decoded for the monochrome adapter are 3B4h, 3B5h, 3B8h, 3B9h, 3Bah and 3BFh.

Note that the (G)MCH Device 1 I/O address range registers defined above are used for all I/O space allocation for any devices requiring such a window on PCI Express.

The PCICMD1 register can disable the routing of I/O cycles to PCI Express.

3.11 (G)MCH Decode Rules and Cross-Bridge Address Mapping

VGAA = 000A_0000 – 000A_FFFF
MDA = 000B_0000 – 000B_7FFF
VGAB = 000B_8000 – 000B_FFFF

MAINMEM = 0100_0000 to TOLUD

HIGHMEM = 4 GB to TOM

RECLAIMMEM = RECLAIMBASE to RECLAIMLIMIT

3.11.1 Legacy VGA and I/O Range Decode Rules

The legacy 128 KB VGA memory range 000A_0000h-000B_FFFFh can be mapped to IGD (Device 2), to PCI Express (Device 1), and/or to the DMI Interface depending on the programming of the VGA steering bits. Priority for VGA mapping is constant in that the (G)MCH always decodes internally mapped devices first. Internal to the GMCH, decode precedence is always given to IGD. The GMCH always positively decodes internally mapped devices, namely the IGD and PCI-Express. Subsequent decoding of regions mapped to PCI Express or the DMI Interface depends on the Legacy VGA configurations bits (VGA Enable and MDAP).

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4 (G)MCH Register Description

The (G)MCH contains two sets of software accessible registers, accessed via the Host processor I/O address space: Control registers and internal configuration registers.

- Control registers are I/O mapped into the processor I/O space, which control access to PCI and PCI Express configuration space (see section entitled I/O Mapped Registers).
- Internal configuration registers residing within the (G)MCH are partitioned into three logical device register sets (“logical” since they reside within a single physical device). The first register set is dedicated to Host Bridge functionality (i.e. DRAM configuration, other chip-set operating parameters and optional features). The second register block is dedicated to Host-PCI Express Bridge functions (controls PCI Express interface configurations and operating parameters). For the 82Q35/82Q33/82G33 GMCH, there is a third register block for the internal graphics functions.

The (G)MCH internal registers (I/O Mapped, Configuration and PCI Express Extended Configuration registers) are accessible by the Host processor. The registers that reside within the lower 256 bytes of each device can be accessed as Byte, Word (16 bit), or DWord (32 bit) quantities, with the exception of CONFIG_ADDRESS, which can only be accessed as a DWord. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field). Registers which reside in bytes 256 through 4095 of each device may only be accessed using memory mapped transactions in DWord (32 bit) quantities.

Some of the (G)MCH registers described in this section contain reserved bits. These bits are labeled "Reserved”. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note the software does not need to perform read, merge, and write operation for the Configuration Address Register.

In addition to reserved bits within a register, the (G)MCH contains address locations in the configuration space of the Host Bridge entity that are marked either "Reserved" or “Intel Reserved”. The (G)MCH responds to accesses to “Reserved” address locations by completing the host cycle. When a “Reserved” register location is read, a zero value is returned. (“Reserved” registers can be 8-, 16-, or 32 bits in size). Writes to “Reserved” registers have no effect on the (G)MCH. Registers that are marked as “Intel Reserved” must not be modified by system software. Writes to “Intel Reserved” registers may cause system failure. Reads from “Intel Reserved” registers may return a non-zero value.

Upon a Full Reset, the (G)MCH sets its entire set of internal configuration registers to predetermined default states. Some register values at reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bringing up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program the (G)MCH registers accordingly.

4.1 Register Terminology

The following table shows the register-related terminology that is used.

Item	Definition
RO	Read Only bit(s). Writes to these bits have no effect. This may be a status bit or a static value.
RO/S	Read Only / Sticky bit(s). Writes to these bits have no effect. These are status bits only. Bits are not returned to their default values by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is “Power Good Reset” as defined in the PCI Express spec).
RS/WC	Read Set / Write Clear bit(s). The first time the bit is read with an enabled byte, it returns the value 0, but a side-effect of the read is that the value changes to 1. Any subsequent reads with enabled bytes return a 1 until a 1 is written to the bit. When the bit is read, but the byte is not enabled, the state of the bit does not change, and the value returned is irrelevant, but will match the state of the bit. When a 0 is written to the bit, there is no effect. When a 1 is written to the bit, its value becomes 0, until the next byte-enabled read. When the bit is written, but the byte is not enabled, there is no effect.
RW	Read / Write bit(s). These bits can be read and written by software. Hardware may only change the state of this bit by reset.
RWC	Read / Write Clear bit(s). These bits can be read. Internal events may set this bit. A software write of ‘1’ clears (sets to ‘0’) the corresponding bit(s) and a write of ‘0’ has no effect.
RWC/L	Read / Write Clear / Lockable bit(s). These bits can be read. Internal events may set this bit. A software write of ‘1’ clears (sets to ‘0’) the corresponding bit(s) and a write of ‘0’ has no effect. Additionally there is a Key bit (which is marked R/W/K or R/W/L/K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
RWC/S	Read / Write Clear / Sticky bit(s). These bits can be read. Internal events may set this bit. A software write of ‘1’ clears (sets to ‘0’) the corresponding bit(s) and a write of ‘0’ has no effect. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is “Power Good Reset” as defined in the PCI Express spec).
RW/B	Read / Write / Blind bit(s). These bits can be read and written by software. Additionally there is a selector bit which, when set, changes what may be read from these bits. The value written is always stored in a hidden register. When the selector bit indicates that the written value should not be read, some other status is read from this bit. When the selector bit indicates that the written value should be read, the value in the hidden register is read from this bit.
RW/B/L	Read / Write / Blind / Lockable bit(s). These bits can be read and written by software. Additionally there is a selector bit which, when set, changes what may be read from these bits. The value written is always stored in a hidden register. When the selector bit indicates that the written value should not be read, some other status is read from this bit. When the selector bit indicates that the written value should be read, the value in the hidden register is read from this bit. Additionally there is a Key bit (which is marked R/W/K or R/W/L/K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).

Item	Definition
RW/K	Read / Write / Key bit(s). These bits can be read and written by software. Additionally this bit, when set, prohibits some other bit field(s) from being writeable (bit fields become Read Only).
RW/L	Read / Write / Lockable bit(s). These bits can be read and written by software. Additionally there is a Key bit (which is marked R/W/K or R/W/L/K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
RW/L/K	Read / Write / Lockable / Key bit(s). These bits can be read and written by software. Additionally this bit is a Key bit that, when set, prohibits this bit field and/or some other specified bit fields from being writeable (bit fields become Read Only).
RW/S	Read / Write / Sticky bit(s). These bits can be read and written by software. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is “Power Good Reset” as defined in the PCI Express spec).
RW/S/B	Read / Write / Sticky / Blind bit(s). These bits can be read and written by software. Additionally there is a selector bit which, when set, changes what may be read from these bits. The value written is always stored in a hidden register. When the selector bit indicates that the written value should not be read, some other status is read from this bit. When the selector bit indicates that the written value should be read, the value in the hidden register is read from this bit. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is “Power Good Reset” as defined in the PCI Express spec).
RW/SC	Read / Write / Self Clear bit(s). These bits can be read and written by software. When the bit is ‘1’, hardware may clear the bit to ‘0’ based upon internal events, possibly sooner than any subsequent software read could retrieve a ‘1’.
RW/SC/L	Read / Write / Self Clear / Lockable bit(s). These bits can be read and written by software. When the bit is ‘1’, hardware may clear the bit to ‘0’ based upon internal events, possibly sooner than any subsequent software read could retrieve a ‘1’. Additionally there is a bit (which is marked R/W/K or R/W/L/K) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
RWO	Write Once bit(s). Once written by software, bits with this attribute become Read Only. These bits can only be cleared by a Reset. If there are multiple R/WO fields within a DWORD, they should be written all at once (atomically) to avoid capturing an incorrect value.
WO	Write Only. These bits may be written by software, but will always return zeros when read. They are used for write side-effects. Any data written to these registers cannot be retrieved.

4.2 Configuration Process and Registers

4.2.1 Platform Configuration Structure

The DMI physically connects the (G)MCH and the Intel ICH9; so, from a configuration standpoint, the DMI is logically PCI bus 0. As a result, all devices internal to the (G)MCH and the Intel ICH9 appear to be on PCI bus 0.

Note: The ICH9 internal LAN controller does not appear on bus 0 – it appears on the external PCI bus (whose number is configurable).

The system's primary PCI expansion bus is physically attached to the Intel ICH9 and, from a configuration perspective, appears to be a hierarchical PCI bus behind a PCI-to-PCI bridge and therefore has a programmable PCI Bus number. The PCI Express Graphics Attach appears to system software to be a real PCI bus behind a PCI-to-PCI bridge that is a device resident on PCI bus 0.

Note: A physical PCI bus 0 does not exist and that DMI and the internal devices in the (G)MCH and Intel ICH9 logically constitute PCI Bus 0 to configuration software.

The (G)MCH contains four PCI devices within a single physical component. The configuration registers for the four devices are mapped as devices residing on PCI bus 0.

- **Device 0: Host Bridge / DRAM Controller**. Logically this appears as a PCI device residing on PCI bus #0. Device 0 contains the standard PCI header registers, PCI Express base address register, DRAM control (including thermal/throttling control), configuration for the DMI, and other (G)MCH specific registers.
- **Device 1: Host-PCI Express Bridge**. Logically this appears as a "virtual" PCI-to-PCI bridge residing on PCI bus #0 and is compliant with PCI Express Specification rev 1.0. Device 1 contains the standard PCI-to-PCI bridge registers and the standard PCI Express/PCI configuration registers (including the PCI Express memory address mapping). It also contains Isochronous and Virtual Channel controls in the PCI Express extended configuration space.
- **Device 2: Internal Graphics Control** (82Q35, 82Q33 ,82G33 GMCH only). Logically, this appears as a PCI device residing on PCI bus #0. Physically, device 2 contains the configuration registers for 3D, 2D, and display functions.
- **Device 3: Manageability Engine Device.** ME Control.

4.3 Configuration Mechanisms

The processor is the originator of configuration cycles so the FSB is the only interface in the platform where these mechanisms are used. Internal to the (G)MCH transactions received through both configuration mechanisms are translated to the same format.

4.3.1 Standard PCI Configuration Mechanism

The following is the mechanism for translating processor I/O bus cycles to configuration cycles.

The PCI specification defines a slot based "configuration space" that allows each device to contain up to 8 functions with each function containing up to 256 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the processor. Configuration space is supported by a mapping mechanism implemented within the (G)MCH.

The configuration access mechanism makes use of the CONFIG_ADDRESS Register (at I/O address 0CF8h though 0CFBh) and CONFIG_DATA Register (at I/O address 0CFCh though 0CFFh). To reference a configuration register a DWord I/O write cycle is used to place a value into CONFIG_ADDRESS that specifies the PCI bus, the device on that bus, the function within the device and a specific configuration register of the device function being accessed. CONFIG_ADDRESS[31] must be 1 to enable a configuration cycle. CONFIG_DATA then becomes a window into the four bytes of configuration space specified by the contents of CONFIG_ADDRESS. Any read or write to CONFIG_DATA will result in the (G)MCH translating the CONFIG_ADDRESS into the appropriate configuration cycle.

The (G)MCH is responsible for translating and routing the processor's I/O accesses to the CONFIG_ADDRESS and CONFIG_DATA registers to internal (G)MCH configuration registers, DMI or PCI Express.

4.3.2 PCI Express* Enhanced Configuration Mechanism

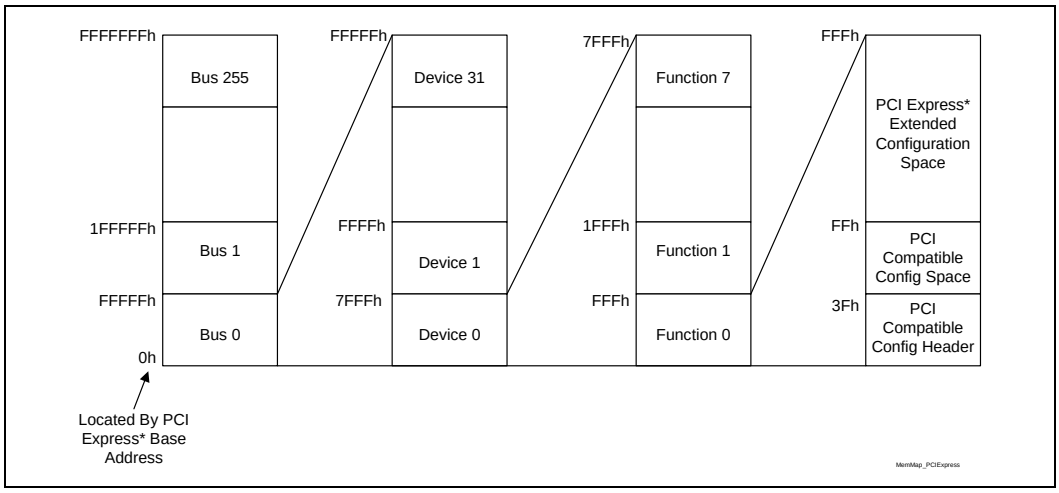
PCI Express extends the configuration space to 4096 bytes per device/function as compared to 256 bytes allowed by PCI Specification Revision 2.3. PCI Express configuration space is divided into a PCI 2.3 compatible region, which consists of the first 256B of a logical device's configuration space and a PCI Express extended region which consists of the remaining configuration space.

The PCI compatible region can be accessed using either the Standard PCI Configuration Mechanism or using the PCI Express Enhanced Configuration Mechanism described in this section. The extended configuration registers may only be accessed using the PCI Express Enhanced Configuration Mechanism. To maintain compatibility with PCI configuration addressing mechanisms, system software must access the extended configuration space using 32-bit operations (32-bit aligned) only. These 32-bit operations include byte enables allowing only appropriate bytes within the DWord to be accessed. Locked transactions to the PCI Express memory mapped configuration address space are not supported. All changes made using either access mechanism are equivalent.

The PCI Express Enhanced Configuration Mechanism utilizes a flat memory-mapped address space to access device configuration registers. This address space is reported by the system firmware to the operating system. There is a register, PCIEXBAR, that defines the base address for the block of addresses below 4GB for the configuration space associated with busses, devices and functions that are potentially a part of the PCI Express root complex hierarchy. In the PCIEXBAR register there exists controls to limit the size of this reserved memory mapped space. 256MB is the amount of address space required to reserve space for every bus, device, and function that could possibly exist. Options for 128MB and 64MB exist in order to free up those addresses for other uses. In these cases the number of busses and all of their associated devices and functions are limited to 128 or 64 busses respectively.

The PCI Express Configuration Transaction Header includes an additional 4 bits (ExtendedRegisterAddress[3:0]) between the Function Number and Register Address fields to provide indexing into the 4 KB of configuration space allocated to each potential device. For PCI Compatible Configuration Requests, the Extended Register Address field must be all zeros.

Figure 4-1. Memory Map to PCI Express* Device Configuration Space



Just the same as with PCI devices, each device is selected based on decoded address information that is provided as a part of the address portion of Configuration Request packets. A PCI Express device will decode all address information fields (bus, device, function and extended address numbers) to provide access to the correct register.

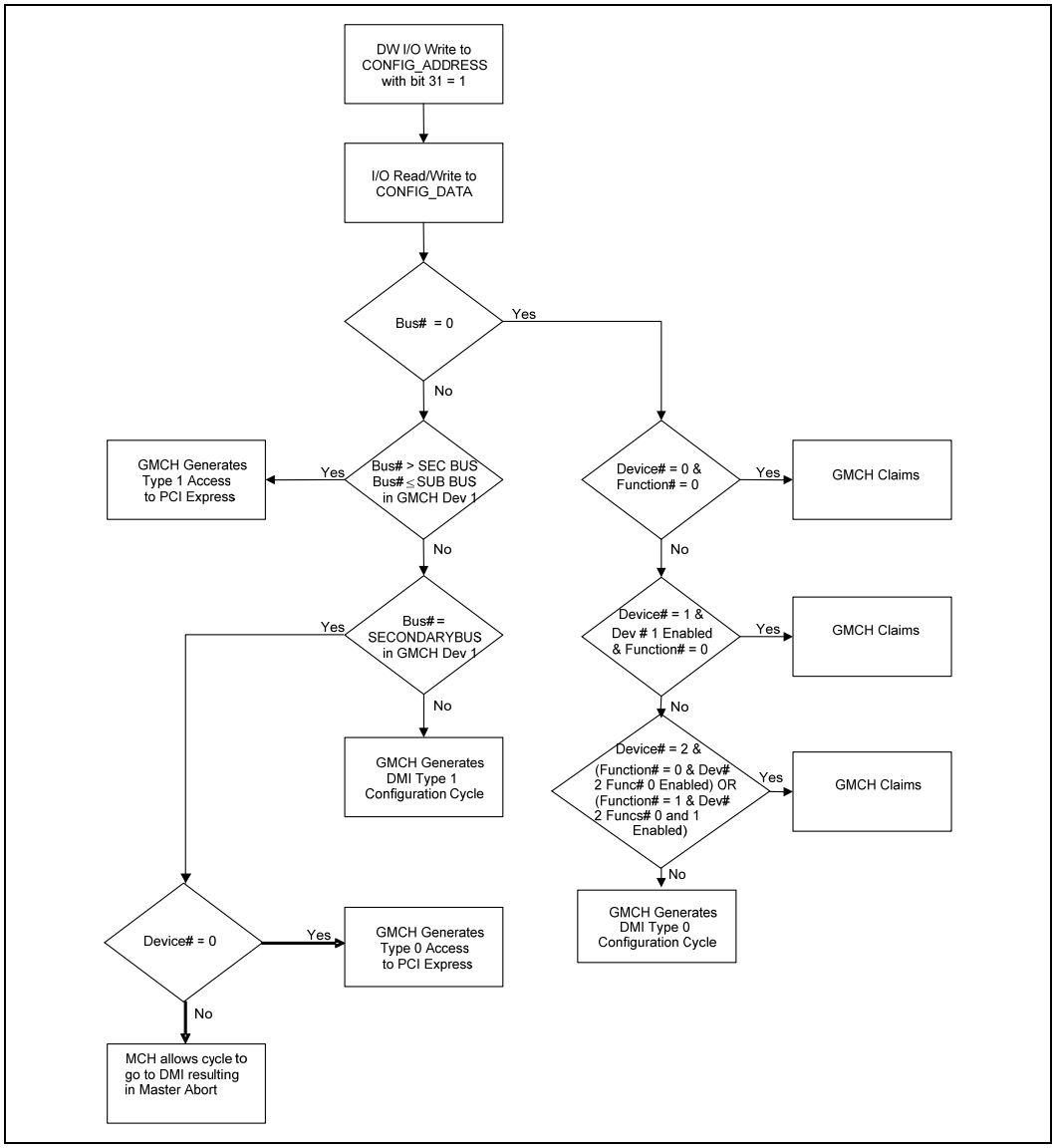
To access this space (steps 1, 2, 3 are done only once by BIOS),

1. use the PCI compatible configuration mechanism to enable the PCI Express enhanced configuration mechanism by writing 1 to bit 0 of the PCIEXBAR register.
2. use the PCI compatible configuration mechanism to write an appropriate PCI Express base address into the PCIEXBAR register
3. calculate the host address of the register you wish to set using (PCI Express base + (bus number * 1 MB) + (device number * 32KB) + (function number * 4 KB) + (1 B * offset within the function) = host address)
4. use a memory write or memory read cycle to the calculated host address to write or read that register.

4.4 Routing Configuration Accesses

The (G)MCH supports two PCI related interfaces: DMI and PCI Express. The (G)MCH is responsible for routing PCI and PCI Express configuration cycles to the appropriate device that is an integrated part of the (G)MCH or to one of these two interfaces. Configuration cycles to the ICH9 internal devices and Primary PCI (including downstream devices) are routed to the ICH9 via DMI. Configuration cycles to both the PCI Express Graphics PCI compatibility configuration space and the PCI Express Graphics extended configuration space are routed to the PCI Express Graphics port device or associated link.

Figure 4-2. GMCH Configuration Cycle Flow Chart



4.4.1 Internal Device Configuration Accesses

The (G)MCH decodes the Bus Number (bits 23:16) and the Device Number fields of the CONFIG_ADDRESS register. If the Bus Number field of CONFIG_ADDRESS is 0 the configuration cycle is targeting a PCI Bus #0 device.

If the targeted PCI Bus #0 device exists in the (G)MCH and is not disabled, the configuration cycle is claimed by the appropriate device.

4.4.2 Bridge Related Configuration Accesses

Configuration accesses on PCI Express or DMI are PCI Express Configuration TLPs.

- Bus Number [7:0] is Header Byte 8 [7:0]
- Device Number [4:0] is Header Byte 9 [7:3]
- Function Number [2:0] is Header Byte 9 [2:0]

And special fields for this type of TLP:

- Extended Register Number [3:0] is Header Byte 10 [3:0]
- Register Number [5:0] is Header Byte 11 [7:2]

See the PCI Express specification for more information on both the PCI 2.3 compatible and PCI Express Enhanced Configuration Mechanism and transaction rules.

4.4.2.1 PCI Express* Configuration Accesses

When the Bus Number of a type 1 Standard PCI Configuration cycle or PCI Express Enhanced Configuration access matches the Device #1 Secondary Bus Number a PCI Express Type 0 Configuration TLP is generated on the PCI Express link targeting the device directly on the opposite side of the link. This should be Device #0 on the bus number assigned to the PCI Express link (likely Bus #1).

The device on other side of link must be Device #0. The (G)MCH will Master Abort any Type 0 Configuration access to a non-zero Device number. If there is to be more than one device on that side of the link there must be a bridge implemented in the downstream device.

When the Bus Number of a type 1 Standard PCI Configuration cycle or PCI Express Enhanced Configuration access is within the claimed range (between the upper bound of the bridge device's Subordinate Bus Number register and the lower bound of the bridge device's Secondary Bus Number register) but doesn't match the Device #1 Secondary Bus Number, a PCI Express Type 1 Configuration TLP is generated on the secondary side of the PCI Express link.

PCI Express Configuration Writes:

- Internally the host interface unit will translate writes to PCI Express extended configuration space to configuration writes on the backbone.
- Writes to extended space are posted on the FSB, but non-posted on the PCI Express or DMI (i.e., translated to configuration writes)

4.4.2.2 DMI Configuration Accesses

Accesses to disabled (G)MCH internal devices, bus numbers not claimed by the Host-PCI Express bridge, or PCI Bus #0 devices not part of the (G)MCH will subtractively decode to the ICH9 and consequently be forwarded over the DMI via a PCI Express configuration TLP.

If the Bus Number is zero, the (G)MCH will generate a Type 0 Configuration Cycle TLP on DMI. If the Bus Number is non-zero, and falls outside the range claimed by the Host-PCI Express bridge, the (G)MCH will generate a Type 1 Configuration Cycle TLP on DMI.

The ICH9 routes configurations accesses in a manner similar to the (G)MCH. The ICH9 decodes the configuration TLP and generates a corresponding configuration access. Accesses targeting a device on PCI Bus #0 may be claimed by an internal device. The ICH7 compares the non-zero Bus Number with the Secondary Bus Number and Subordinate Bus Number registers of its P2P bridges to determine if the configuration access is meant for Primary PCI, or some other downstream PCI bus or PCI Express link.

Configuration accesses that are forwarded to the ICH9, but remain unclaimed by any device or bridge will result in a master abort.

4.5 I/O Mapped Registers

The (G)MCH contains two registers that reside in the processor I/O address space – the Configuration Address (CONFIG_ADDRESS) Register and the Configuration Data (CONFIG_DATA) Register. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

4.5.1 CONFIG_ADDRESS—Configuration Address Register

I/O Address:	0CF8h Accessed as a DW
Default Value:	00000000h
Access:	RW
Size:	32 bits

CONFIG_ADDRESS is a 32-bit register that can be accessed only as a DW. A Byte or Word reference will "pass through" the Configuration Address Register and DMI onto the Primary PCI bus as an I/O cycle. The CONFIG_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Access & Default	Description
31	RW 0b	**Configuration Enable (CFGE).** 0 = Disable 1 = Enable
30:24		Reserved
23:16	RW 00h	**Bus Number.** If the Bus Number is programmed to 00h the target of the Configuration Cycle is a PCI Bus 0 agent. If this is the case and the (G)MCH is not the target (i.e., the device number is ≥ 2), then a DMI Type 0 Configuration Cycle is generated. If the Bus Number is non-zero, and does not fall within the ranges enumerated by device 1's Secondary Bus Number or Subordinate Bus Number Register, then a DMI Type 1 Configuration Cycle is generated. If the Bus Number is non-zero and matches the value programmed into the Secondary Bus Number Register of device 1, a Type 0 PCI configuration cycle will be generated on PCI Express-G. If the Bus Number is non-zero, greater than the value in the Secondary Bus Number register of device 1 and less than or equal to the value programmed into the Subordinate Bus Number Register of device 1 a Type 1 PCI configuration cycle will be generated on PCI Express-G. This field is mapped to byte 8 [7:0] of the request header format during PCI Express Configuration cycles and A[23:16] during the DMI Type 1 configuration cycles.
15:11	RW 00h	**Device Number.** This field selects one agent on the PCI bus selected by the Bus Number. When the Bus Number field is "00" the (G)MCH decodes the Device Number field. The (G)MCH is always Device Number 0 for the Host bridge entity, Device Number 1 for the Host-PCI Express entity. Therefore, when the Bus Number =0 and the Device Number equals 0, 1, or 2 the internal (G)MCH devices are selected. This field is mapped to byte 6 [7:3] of the request header format during PCI Express Configuration cycles and A [15:11] during the DMI configuration cycles.
10:8	RW 000b	**Function Number.** This field allows the configuration registers of a particular function in a multi-function device to be accessed. The (G)MCH ignores configuration cycles to its internal devices if the function number is not equal to 0 or 1. This field is mapped to byte 6 [2:0] of the request header format during PCI Express Configuration cycles and A[10:8] during the DMI configuration cycles.
7:2	RW 00h	**Register Number.** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. This field is mapped to byte 7 [7:2] of the request header format during PCI Express Configuration cycles and A[7:2] during the DMI Configuration cycles.
1:0		Reserved

4.5.2 CONFIG_DATA—Configuration Data Register

I/O Address: 0CFCh
Default Value: 00000000h
Access: RW
Size: 32 bits

CONFIG_DATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFIG_DATA is determined by the contents of CONFIG_ADDRESS.

Bit	Access & Default	Description
31:0	RW 0000 0000h	**Configuration Data Window (CDW).** If bit 31 of CONFIG_ADDRESS is 1, any I/O access to the CONFIG_DATA register will produce a configuration transaction using the contents of CONFIG_ADDRESS to determine the bus, device, function, and offset of the register to be accessed.

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5 DRAM Controller Registers (D0:F0)

5.1 DRAM Controller (D0:F0)

The DRAM Controller registers are in Device 0 (D0), Function 0 (F0).

Warning: Address locations that are not listed are considered Intel Reserved registers locations. Reads to Reserved registers may return non-zero values. Writes to reserved locations may cause system failures.

All registers that are defined in the PCI 2.3 specification, but are not necessary or implemented in this component are simply not included in this document. The reserved/unimplemented space in the PCI configuration header space is not documented as such in this summary.

Table 5-1. DRAM Controller Register Address Map (D0:F0)

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	29C0h	RO
04–05h	PCICMD	PCI Command	0006h	RO, RW
06–07h	PCISTS	PCI Status	0090h	RWC, RO
08h	RID	Revision Identification	00h	RO
09–0Bh	CC	Class Code	060000h	RO
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HDR	Header Type	00h	RO
2C–2Dh	SVID	Subsystem Vendor Identification	0000h	RWO
2E–2Fh	SID	Subsystem Identification	0000h	RWO
34h	CAPPTR	Capabilities Pointer	E0h	RO
40–47h	PXPEPBAR	PCI Express Port Base Address	0000000000 000000h	RW/L, RO
48–4Fh	MCHBAR	(G)MCH Memory Mapped Register Range Base	0000000000 000000h	RW/L, RO
52–53h	GGC	GMCH Graphics Control Register	0030h	RO, RW/L
54–57h	DEVEN	Device Enable	000003DBh	RO, RW/L

Address Offset	Register Symbol	Register Name	Default Value	Access
60–67h	PCIEXBAR	PCI Express Register Range Base Address	00000000E0000000h	RO, RW/L, RW/L/K
68–6Fh	DMIBAR	Root Complex Register Range Base Address	0000000000000000h	RO, RW/L
90h	PAM0	Programmable Attribute Map 0	00h	RO, RW/L
91h	PAM1	Programmable Attribute Map 1	00h	RO, RW/L
92h	PAM2	Programmable Attribute Map 2	00h	RO, RW/L
93h	PAM3	Programmable Attribute Map 3	00h	RO, RW/L
94h	PAM4	Programmable Attribute Map 4	00h	RO, RW/L
95h	PAM5	Programmable Attribute Map 5	00h	RO, RW/L
96h	PAM6	Programmable Attribute Map 6	00h	RO, RW/L
97h	LAC	Legacy Access Control	00h	RW/L, RO, RW
98–99h	REMAPBASE	Remap Base Address Register	03FFh	RO, RW/L
9A–9Bh	REMAPLIMIT	Remap Limit Address Register	0000h	RO, RW/L
9Dh	SMRAM	System Management RAM Control	02h	RO, RW/L, RW, RW/L/K
9Eh	ESMRAMC	Extended System Management RAM Control	38h	RW/L, RWC, RO
A0–A1h	TOM	Top of Memory	0001h	RO, RW/L
A2–A3h	TOUUD	Top of Upper Usable Dram	0000h	RW/L
A4–A7h	GBSM	Graphics Base of Stolen Memory	00000000h	RW/L ,RO
A8–ABh	BGSM	Base of GTT stolen Memory	00000000h	RW/L ,RO
AC–AFh	TSEGMB	TSEG Memory Base	00000000h	RW/L, RO
B0–B1h	TOLUD	Top of Low Usable DRAM	0010h	RW/L RO
C8–C9h	ERRSTS	Error Status	0000h	RO, RWC/S
CA–CBh	ERRCMD	Error Command	0000h	RO, RW
CC–CDh	SMICMD	SMI Command	0000h	RO, RW
DC–DFh	SKPD	Scratchpad Data	00000000h	RW
E0–EAh	CAPID0	Capability Identifier	0000010000000010B0009h	RO

5.1.1 VID—Vendor Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 0–1h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 8086h	**Vendor Identification Number (VID):** PCI standard identification for Intel.

5.1.2 DID—Device Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 02–03h
Default Value: See table below
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO	**Device Identification Number (DID):**
	29B0h	29B0h = Intel® 82Q35 GMCH
	29C0h	29C0h = Intel® 82G33/82P35 (G)MCH
	29D0h	29D0h = Intel® 82Q33 GMCH

5.1.3 PCICMD—PCI Command

B/D/F/Type: 0/0/0/PCI
Address Offset: 4–5h
Default Value: 0006h
Access: RO, RW
Size: 16 bits

Since (G)MCH Device 0 does not physically reside on PCI_A many of the bits are not implemented.

Bit	Access & Default	Description
15:10	RO 00h	Reserved
9	RO 0b	**Fast Back-to-Back Enable (FB2B):** This bit controls whether or not the master can do fast back-to-back write. Since device 0 is strictly a target, this bit is not implemented and is hardwired to 0.
8	RW 0b	**SERR Enable (SERRE):** This bit is a global enable bit for Device 0 SERR messaging. The (G)MCH does not have an SERR signal. The (G)MCH communicates the SERR condition by sending an SERR message over DMI to the ICH. 1= The (G)MCH is enabled to generate SERR messages over DMI for specific Device 0 error conditions that are individually enabled in the ERRCMD and DMIUEMSK registers. The error status is reported in the ERRSTS, PCISTS, and DMIUEST registers. 0 = The SERR message is not generated by the (G)MCH for Device 0. Note that this bit only controls SERR messaging for the Device 0. Device 1 has its own SERRE bits to control error reporting for error conditions occurring in that device. The control bits are used in a logical OR manner to enable the SERR DMI message mechanism.
7	RO 0b	**Address/Data Stepping Enable (ADSTEP):** Address/data stepping is not implemented in the (G)MCH, and this bit is hardwired to 0.
6	RW 0b	**Parity Error Enable (PERRE):** This bit controls whether or not the Master Data Parity Error bit in the PCI Status register can bet set. 0= Master Data Parity Error bit in PCI Status register can NOT be set. 1 = Master Data Parity Error bit in PCI Status register CAN be set.
5	RO 0b	**VGA Palette Snoop Enable (VGASNOOP):** The (G)MCH does not implement this bit and it is hardwired to a 0.
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** The (G)MCH will never issue memory write and invalidate commands. This bit is therefore hardwired to 0.
3	RO 0b	**Special Cycle Enable (SCE):** The (G)MCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
2	RO 1b	**Bus Master Enable (BME):** The (G)MCH is always enabled as a master on the backbone. This bit is hardwired to a 1.
1	RO 1b	**Memory Access Enable (MAE):** The (G)MCH always allows access to main memory. This bit is not implemented and is hardwired to 1.
0	RO 0b	**I/O Access Enable (IOAE):** This bit is not implemented in the (G)MCH and is hardwired to a 0.

5.1.4 PCISTS—PCI Status

B/D/F/Type: 0/0/0/PCI
Address Offset: 6–7h
Default Value: 0090h
Access: RWC, RO
Size: 16 bits

This status register reports the occurrence of error events on Device 0's PCI interface. Since the (G)MCH Device 0 does not physically reside on PCI_A many of the bits are not implemented.

Bit	Access & Default	Description
15	RWC 0b	**Detected Parity Error (DPE):** 1= Device received a Poisoned TLP.
14	RWC 0b	**Signaled System Error (SSE):** Software clears this bit by writing a 1 to it. 1= The (G)MCH Device 0 generated a SERR message over DMI for any enabled Device 0 error condition. Device 0 error conditions are enabled in the PCICMD, ERRCMD, and DMIUEMSK registers. Device 0 error flags are read/reset from the PCISTS, ERRSTS, or DMIUEST registers.
13	RWC 0b	**Received Master Abort Status (RMAS):** Software clears this bit by writing a 1 to it. 1 = (G)MCH generated a DMI request that receives an Unsupported Request completion packet.
12	RWC 0b	**Received Target Abort Status (RTAS):** Software clears this bit by writing a 1 to it. 1 = (G)MCH generated a DMI request that receives a Completer Abort completion packet.
11	RO 0b	**Signaled Target Abort Status (STAS):** The (G)MCH will not generate a Target Abort DMI completion packet or Special Cycle. This bit is not implemented in the (G)MCH and is hardwired to a 0.
10:9	RO 00b	**DEVSEL Timing (DEVT):** These bits are hardwired to "00". Writes to these bit positions have no affect. Device 0 does not physically connect to PCI_A. These bits are set to "00" (fast decode) so that optimum DEVSEL timing for PCI_A is not limited by the (G)MCH.
8	RWC 0b	**Master Data Parity Error Detected (DPD):** 1 = This bit is set when DMI received a Poisoned completion from the ICH. **NOTE:** This bit can only be set when the Parity Error Enable bit in the PCI Command register is set.
7	RO 1b	**Fast Back-to-Back (FB2B):** This bit is hardwired to 1. Device 0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for PCI_A is not limited by the (G)MCH.

Bit	Access & Default	Description
6	RO 0b	Reserved
5	RO 0b	**66 MHz Capable:** Does not apply to PCI Express. Hardwired to 0.
4	RO 1b	**Capability List (CLIST):** This bit is hardwired to 1 to indicate to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h. Register CAPPTR contains an offset pointing to the start address within configuration space of this device where the Capability Identification register resides.
3:0	RO 0h	Reserved

5.1.5 RID—Revision Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 8h
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the revision number of the (G)MCH Device #0. These bits are read only and writes to this register have no effect.

Bit	Access & Default	Description
7:0	RO 00h	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the (G)MCH Device 0. Refer to the *Intel® 3 Series Express Chipset Family Specification Update* for the value of the Revision ID register.

5.1.6 CC—Class Code

B/D/F/Type: 0/0/0/PCI
Address Offset: 09–0Bh
Default Value: 060000h
Access: RO
Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register-specific programming interface.

Bit	Access & Default	Description
23:16	RO 06h	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the (G)MCH. 06h = Bridge device.
15:8	RO 00h	**Sub-Class Code (SUBCC):** This is an 8-bit value that indicates the category of Bridge into which the (G)MCH falls. 00h = Host Bridge.
7:0	RO 00h	**Programming Interface (PI):** This is an 8-bit value that indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

5.1.7 MLT—Master Latency Timer

B/D/F/Type: 0/0/0/PCI
Address Offset: 0Dh
Default Value: 00h
Access: RO
Size: 8 bits

Device 0 in the (G)MCH is not a PCI master. Therefore this register is not implemented.

Bit	Access & Default	Description
7:0	RO 00h	Reserved

5.1.8 HDR—Header Type

B/D/F/Type: 0/0/0/PCI
Address Offset: Eh
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Access & Default	Description
7:0	RO 00h	**PCI Header (HDR):** This field always returns 0 to indicate that the (G)MCH is a single function device with standard header layout. Reads and writes to this location have no effect.

5.1.9 SVID—Subsystem Vendor Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 2C–2Dh
Default Value: 0000h
Access: RWO
Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bit	Access & Default	Description
15:0	RWO 0000h	**Subsystem Vendor ID (SUBVID):** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.

5.1.10 SID—Subsystem Identification

B/D/F/Type: 0/0/0/PCI
Address Offset: 2E–2Fh
Default Value: 0000h
Access: RWO
Size: 16 bits

This value is used to identify a particular subsystem.

Bit	Access & Default	Description
15:0	RWO 0000h	**Subsystem ID (SUBID):** This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.

5.1.11 CAPPTR—Capabilities Pointer

B/D/F/Type: 0/0/0/PCI
Address Offset: 34h
Default Value: E0h
Access: RO
Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Access & Default	Description
7:0	RO E0h	**Capabilities Pointer (CAPPTR):** Pointer to the offset of the first capability ID register block. In this case the first capability is the product-specific Capability Identifier (CAPID0).

5.1.12 PXPEPBAR—PCI Express* Egress Port Base Address

B/D/F/Type: 0/0/0/PCI
Address Offset: 40–47h
Default Value: 0000000000000000h
Access: RW/L, RO
Size: 64 bits

This is the base address for the PCI Express Egress Port MMIO Configuration space. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the Egress port MMIO configuration space is disabled and must be enabled by writing a 1 to PXPEPBAREN [Dev 0, offset 40h, bit 0]

All the bits in this register are locked in Intel® TXT mode.

Bit	Access & Default	Description
63:36	RO 0000000h	Reserved
35:12	RW/L 000000h	**PCI Express Egress Port MMIO Base Address (PXPEPBAR):** This field corresponds to bits 35:12 of the base address PCI Express Egress Port MMIO configuration space. BIOS will program this register resulting in a base address for a 4 KB block of contiguous memory address space. This register ensures that a naturally aligned 4 KB space is allocated within the first 64 GB of addressable memory space. System Software uses this base address to program the (G)MCH MMIO register set. All the bits in this register are locked in Intel® TXT mode.
11:1	RO 000h	Reserved
0	RW/L 0b	**PXPEPBAR Enable (PXPEPBAREN):** 0 = PXPEPBAR is disabled and does not claim any memory 1 = PXPEPBAR memory mapped accesses are claimed and decoded appropriately This register is locked by Intel® TXT.

5.1.13 MCHBAR—(G)MCH Memory Mapped Register Range Base

B/D/F/Type: 0/0/0/PCI
Address Offset: 48–4Fh
Default Value: 0000000000000000h
Access: RW/L, RO
Size: 64 bits

This is the base address for the (G)MCH Memory Mapped Configuration space. There is no physical memory within this 16 KB window that can be addressed. The 16 KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the (G)MCH MMIO Memory Mapped Configuration space is disabled and must be enabled by writing a 1 to MCHBAREN [Dev 0, offset48h, bit 0]

All the bits in this register are locked in Intel® Execution Technology mode.

The register space contains memory control, initialization, timing, and buffer strength registers; clocking registers; and power and thermal management registers. The 16 KB space reserved by the MCHBAR register is not accessible during Intel® Execution Technology mode of operation or if the ME security lock is asserted (MESMLCK.ME_SM_lock at PCI device 0, function 0, offset F4h) except for the following offset ranges.

02B8h to 02BFh: Channel 0 Throttle Counter Status Registers

06B8h to 06BFh: Channel 1 Throttle Counter Status Registers

0CD0h to 0CFFh: Thermal Sensor Control Registers

3000h to 3FFFh: Unlocked registers for future expansion

Bit	Access & Default	Description
63:36	RO 0000000h	Reserved
35:14	RW/L 000000h	**GMCH Memory Mapped Base Address (MCHBAR):** This field corresponds to bits 35:14 of the base address (G)MCH Memory Mapped configuration space. BIOS will program this register resulting in a base address for a 16 KB block of contiguous memory address space. This register ensures that a naturally aligned 16 KB space is allocated. System Software uses this base address to program the (G)MCH Memory Mapped register set. All the bits in this register are locked in Intel® TXT mode.
13:1	RO 0000h	Reserved
0	RW/L 0b	**MCHBAR Enable (MCHBAREN):** 0= MCHBAR is disabled and does not claim any memory 1 = MCHBAR memory mapped accesses are claimed and decoded appropriately This register is locked by Intel® TXT.

5.1.14 GGC—GMCH Graphics Control Register (Intel® 82Q35, 82Q33, 82G33 GMCH Only)

B/D/F/Type: 0/0/0/PCI
Address Offset: 52–53h
Default Value: 0030h
Access: RO, RW/L
Size: 16 bits

All the bits in this register are Intel® TXT lockable.

Bit	Access & Default	Description
15:10	RO 00h	Reserved
9:8	RW/L 0h	**GTT Graphics Memory Size (GGMS):** This field is used to select the amount of main memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. 00 = No memory pre-allocated. GTT cycles (Memory and I/O) are not claimed. 01 = No VT mode, 1 MB of memory pre-allocated for GTT. 10 = VT mode, 2 MB of memory pre-allocated for GTT. 11 = Reserved **Note:** This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.

Bit	Access & Default	Description
7:4	RW/L 0011b	**Graphics Mode Select (GMS):** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. 0000 = No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Memory and I/O), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80h. 0001 = DVMT (UMA) mode, 1 MB of memory pre-allocated for frame buffer. 0010 = DVMT (UMA) mode, 4 MB of memory pre-allocated for frame buffer. 0011 = DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer. 0100 = DVMT (UMA) mode, 16 MB of memory pre-allocated for frame buffer. 0101 = DVMT (UMA) mode, 32 MB of memory pre-allocated for frame buffer. 0110 = DVMT (UMA) mode, 48 MB of memory pre-allocated for frame buffer. 0111 = DVMT (UMA) mode, 64 MB of memory pre-allocated for frame buffer. 1000 = DVMT (UMA) mode, 128 MB of memory pre-allocated for frame buffer. 1001 = DVMT (UMA) mode, 256 MB of memory pre-allocated for frame buffer. **Note:** This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set. **BIOS Requirement:** BIOS must not set this field to 000 if IVD (bit 1 of this register) is 0.
3:2	RO 00b	Reserved
1	RW/L 0b	**IGD VGA Disable (IVD):** 0 = Enable. Device 2 (IGD) claims VGA memory and I/O cycles, the Sub-Class Code within Device 2 Class Code register is 00h. 1 = Disable. Device 2 (IGD) does not claim VGA cycles (Memory and I/O), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80h. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field (bits 6:4 of this register) pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0[46] = 1) or via a register (DEVEN[3] = 0). This register is locked by Intel® TXT or ME stolen Memory lock.
0	RO 0b	Reserved

5.1.15 DEVEN—Device Enable

B/D/F/Type: 0/0/0/PCI
Address Offset: 54–57h
Default Value: 000003DBh
Access: RO, RW/L
Size: 32 bits

This register allows for enabling/disabling of PCI devices and functions that are within the (G)MCH. All the bits in this register are Intel® TXT Lockable.

Bit	Access & Default	Description
31:10	RO 00000h	Reserved
9	RW/L 1b	**EP Function 3 (D3F3EN):** 0 = Bus 0 Device 3 Function 3 is disabled and hidden 1 = Bus 0 Device 3 Function 3 is enabled and visible If Device 3, Function 0 is disabled and hidden, then Device 3, Function 3 is also disabled and hidden independent of the state of this bit. If this (G)MCH does not have ME capability (CAPID0[57] = 1 or CAPID0[56] = 1), then Device 3, Function 3 is disabled and hidden independent of the state of this bit.
8	RW/L 1b	**EP Function 2 (D3F2EN):** 0 = Bus 0 Device 3 Function 2 is disabled and hidden 1 = Bus 0 Device 3 Function 2 is enabled and visible If Device 3, Function 0 is disabled and hidden, then Device 3, Function 2 is also disabled and hidden independent of the state of this bit. If this (G)MCH does not have ME capability (CAPID0[57] = 1 or CAPID0[56] = 1), then Device 3, Function 2 is disabled and hidden independent of the state of this bit.
7	RW/L 1b	**EP Function 1 (D3F1EN):** 0 = Bus 0, Device 3, Function 1 is disabled and hidden 1 = Bus 0, Device 3, Function 1 is enabled and visible. If Device 3, Function 0 is disabled and hidden, then Device 3, Function 1 is also disabled and hidden independent of the state of this bit. If this (G)MCH does not have ME capability (CAPID0[57] = 1), then Device 3, Function 1 is disabled and hidden independent of the state of this bit.
6	RW/L 1b	**EP Function 0 (D3F0EN):** 0 = Bus 0, Device 3, Function 0 is disabled and hidden 1 = Bus 0, Device 3, Function 0 is enabled and visible. If this (G)MCH does not have ME capability (CAPID0[57] = 1), then Device 3, Function 0 is disabled and hidden independent of the state of this bit.

Bit	Access & Default	Description
5	RO 0b	Reserved
4	RW/L 1b	**82Q35, 82Q33, 82G33 GMCH** **Internal Graphics Engine Function 1 (D2F1EN):** 0 = Bus 0, Device 2, Function 1 is disabled and hidden 1 = Bus 0, Device 2, Function 1 is enabled and visible If Device 2, Function 0 is disabled and hidden, then Device 2, Function 1 is also disabled and hidden independent of the state of this bit. If this component is not capable of Dual Independent Display (CAPID0[78] = 1), then this bit is hardwired to 0b to hide Device 2, Function 1. **82P35 MCH** Reserved
3	RW/L 1b	**82Q35, 82Q33, 82G33 GMCH** **Internal Graphics Engine Function 0 (D2F0EN):** 0 = Bus 0, Device 2, Function 0 is disabled and hidden 1 = Bus 0, Device 2, Function 0 is enabled and visible If this GMCH does not have internal graphics capability (CAPID0[46] = 1), then Device 2, Function 0 is disabled and hidden independent of the state of this bit. **82P35 MCH** Reserved
2	RO 0b	Reserved
1	RW/L 1b	**PCI Express Port (D1EN):** 0 = Bus 0, Device 1, Function 0 is disabled and hidden. 1 = Bus 0, Device 1, Function 0 is enabled and visible. Default value is determined by the device capabilities (see CAPID0 [44]), SDVO Presence hardware strap and the SDVO/PCI Express Concurrent hardware strap. Device 1 is Disabled on Reset if the SDVO Presence strap was sampled high, and the SDVO/PCI Express Concurrent strap was sampled low at the last assertion of PWROK, and is enabled by default otherwise.
0	RO 1b	**Host Bridge (D0EN):** Bus 0, Device 0, Function 0 may not be disabled and is therefore hardwired to 1.

5.1.16 PCIEXBAR—PCI Express* Register Range Base Address

B/D/F/Type:	0/0/0/PCI
Address Offset:	60–67h
Default Value:	00000000E0000000h
Access:	RO, RW/L, RW/L/K
Size:	64 bits

This is the base address for the PCI Express configuration space. This window of addresses contains the 4 KB of configuration space for each PCI Express device that can potentially be part of the PCI Express Hierarchy associated with the (G)MCH. There is not actual physical memory within this window of up to 256 MB that can be addressed. The actual length is determined by a field in this register. Each PCI Express Hierarchy requires a PCI Express BASE register. The (G)MCH supports one PCI Express hierarchy. The region reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. For example, MCHBAR reserves a 16 KB space and PXPEPBAR reserves a 4 KB space both outside of PCIEXBAR space. They cannot be overlayed on the space reserved by PCIEXBAR for devices 0.

On reset, this register is disabled and must be enabled by writing a 1 to the enable field in this register. This base address shall be assigned on a boundary consistent with the number of buses (defined by the Length field in this register), above TOLUD and still within 64 bit addressable memory space. All other bits not decoded are read only 0. The PCI Express Base Address cannot be less than the maximum address written to the Top of physical memory register (TOLUD). Software must ensure that these ranges do not overlap with known ranges located above TOLUD. Software must ensure that the sum of Length of enhanced configuration region + TOLUD + (other known ranges reserved above TOLUD) is not greater than the 36-bit addressable limit of 64 GB. In general system implementation and number of PCI/PCI Express/PCI-X buses supported in the hierarchy will dictate the length of the region.

All the Bits in this register are locked in Intel® TXT mode.

Bit	Access & Default	Description
63:36	RO 0000000h	Reserved

Bit	Access & Default	Description
35:28	RW/L 0Eh	**PCI Express Base Address (PCIEXBAR):** This field corresponds to bits 35:28 of the base address for PCI Express enhanced configuration space. BIOS will program this register resulting in a base address for a contiguous memory address space; size is defined by bits 2:1 of this register. This Base address shall be assigned on a boundary consistent with the number of buses (defined by the Length field in this register) above TOLUD and still within 64-bit addressable memory space. The address bits decoded depend on the length of the region defined by this register. This register is locked by Intel® TXT. The address used to access the PCI Express configuration space for a specific device can be determined as follows: PCI Express Base Address + Bus Number * 1 MB + Device Number * 32 KB + Function Number * 4 KB The address used to access the PCI Express configuration space for Device 1 in this component would be PCI Express Base Address + 0 * 1 MB + 1 * 32 KB + 0 * 4 KB = PCI Express Base Address + 32 KB. Remember that this address is the beginning of the 4KB space that contains both the PCI compatible configuration space and the PCI Express extended configuration space. All the Bits in this register are locked in Intel® TXT mode.
27	RW/L 0b	**128 MB Base Address Mask (128ADMSK):** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits 2:1 in this register.
26	RW/L 0b	**64 MB Base Address Mask (64ADMSK):** This bit is either part of the PCI Express Base Address (R/W) or part of the Address Mask (RO, read 0b), depending on the value of bits 2:1 in this register.
25:3	RO 000000h	Reserved
2:1	RW/L/K 00b	**Length (LENGTH):** This Field describes the length of this region. Enhanced Configuration Space Region/Buses Decoded 00 = 256 MB (buses 0–255). Bits 31:28 are decoded in the PCI Express Base Address Field 01 = 128 MB (Buses 0–127). Bits 31:27 are decoded in the PCI Express Base Address Field. 10 = 64 MB (Buses 0–63). Bits 31:26 are decoded in the PCI Express Base Address Field. 11 = Reserved This register is locked by Intel® TXT.

Bit	Access & Default	Description
0	RW/L 0b	**PCIEXBAR Enable (PCIEXBAREN):** 0 = The PCIEXBAR register is disabled. Memory read and write transactions proceed as if there were no PCIEXBAR register. PCIEXBAR bits 35:26 are R/W with no functionality behind them. 1 = The PCIEXBAR register is enabled. Memory read and write transactions whose address bits 35:26 match PCIEXBAR will be translated to configuration reads and writes within the (G)MCH. These Translated cycles are routed as shown in the table above. This register is locked by Intel® TXT.

5.1.17 DMIBAR—Root Complex Register Range Base Address

B/D/F/Type: 0/0/0/PCI
Address Offset: 68–6Fh
Default Value: 0000000000000000h
Access: RO, RW/L
Size: 64 bits

This is the base address for the Root Complex configuration space. This window of addresses contains the Root Complex Register set for the PCI Express Hierarchy associated with the (G)MCH. There is no physical memory within this 4 KB window that can be addressed. The 4 KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the Root Complex configuration space is disabled and must be enabled by writing a 1 to DMIBAREN [Dev 0, offset 68h, bit 0] All the Bits in this register are locked in Intel® TXT mode.

Bit	Access	Description
63:36	RO 0000000h	Reserved
35:12	RW/L 000000h	**DMI Base Address (DMIBAR):** This field corresponds to bits 35:12 of the base address DMI configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4 KB space is allocated within the first 64 GB of addressable memory space. System Software uses this base address to program the DMI register set.
11:1	RO 000h	Reserved
0	RW/L 0b	**DMIBAR Enable (DMIBAREN):** 0 = DMIBAR is disabled and does not claim any memory 1 = DMIBAR memory mapped accesses are claimed and decoded appropriately This register is locked by Intel® TXT.

5.1.18 PAM0—Programmable Attribute Map 0

B/D/F/Type:	0/0/0/PCI
Address Offset:	90h
Default Value:	00h
Access:	RO, RW/L
Size:	8 bits

This register controls the read, write, and shadowing attributes of the BIOS area from 0F0000h–0FFFFFh. The (G)MCH allows programmable memory attributes on 13 Legacy memory segments of various sizes in the 768 KB to 1 MB address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Cacheability of these areas is controlled via the MTRR registers in the P6 processor. Two bits are used to specify memory attributes for each memory segment. These bits apply to both host accesses and PCI initiator accesses to the PAM areas. These attributes are:

RE – Read Enable. When RE = 1, the processor read accesses to the corresponding memory segment are claimed by the (G)MCH and directed to main memory. Conversely, when RE = 0, the host read accesses are directed to PCI_A.

WE – Write Enable. When WE = 1, the host write accesses to the corresponding memory segment are claimed by the (G)MCH and directed to main memory. Conversely, when WE = 0, the host write accesses are directed to PCI_A.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is Read Only. Each PAM Register controls two regions, typically 16 KB in size.

Note that the (G)MCH may hang if a PCI Express Graphics Attach or DMI originated access to Read Disabled or Write Disabled PAM segments occur (due to a possible IWB to non-DRAM).

For these reasons the following critical restriction is placed on the programming of the PAM regions: At the time that a DMI or PCI Express Graphics Attach accesses to the PAM region may occur, the targeted PAM segment must be programmed to be both readable and writeable.

Bit	Access & Default	Description
7:6	RO 00b	Reserved
5:4	RW/L 00b	**0F0000h–0FFFFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0F0000h to 0FFFFFh. 00 = DRAM Disabled: All accesses are directed to DMI. 01 = Read Only: All reads are sent to DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM. This register is locked by Intel® TXT.
3:0	RO 0h	Reserved

5.1.19 PAM1—Programmable Attribute Map 1

B/D/F/Type: 0/0/0/PCI
Address Offset: 91h
Default Value: 00h
Access: RO, RW/L
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C0000h–0C7FFFh.

Bit	Access & Default	Description
7:6	RO 00b	Reserved
5:4	RW/L 00b	**0C4000h–0C7FFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C4000 to 0C7FFF. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM. This register is locked by Intel® TXT.
3:2	RO 00b	Reserved
1:0	RW/L 00b	**0C0000h–0C3FFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C0000h to 0C3FFFh. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM. This register is locked by Intel® TXT.

5.1.20 PAM2—Programmable Attribute Map 2

B/D/F/Type: 0/0/0/PCI
Address Offset: 92h
Default Value: 00h
Access: RO, RW/L
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C8000h–0CFFFFh.

Bit	Access & Default	Description
7:6	RO 00b	Reserved
5:4	RW/L 00b	**0CC000h–0CFFFFh Attribute (HIENABLE):** 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM. This register is locked by Intel® TXT.
3:2	RO 00b	Reserved
1:0	RW/L 00b	**0C8000h–0CBFFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C8000h to 0CBFFFh. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM. This register is locked by Intel® TXT.

5.1.21 PAM3—Programmable Attribute Map 3

B/D/F/Type: 0/0/0/PCI
Address Offset: 93h
Default Value: 00h
Access: RO, RW/L
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D0000h–0D7FFFh.

Bit	Access & Default	Description
7:6	RO 00b	Reserved
5:4	RW/L 00b	**0D4000h–0D7FFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D4000h to 0D7FFFh. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM. This register is locked by Intel® TXT.
3:2	RO 00b	Reserved
1:0	RW/L 00b	**0D0000–0D3FFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D0000h to 0D3FFFh. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM. This register is locked by Intel® TXT.

5.1.22 PAM4—Programmable Attribute Map 4

B/D/F/Type: 0/0/0/PCI
Address Offset: 94h
Default Value: 00h
Access: RO, RW/L
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D8000h–0DFFFFh.

Bit	Access & Default	Description
7:6	RO 00b	Reserved
5:4	RW/L 00b	**0DC000h–0DFFFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0DC000h to 0DFFFFh. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM. This register is locked by Intel® TXT.
3:2	RO 00b	Reserved
1:0	RW/L 00b	**0D8000h–0DBFFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D8000h to 0DBFFFh. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM. This register is locked by Intel® TXT.

5.1.23 PAM5—Programmable Attribute Map 5

B/D/F/Type: 0/0/0/PCI
Address Offset: 95h
Default Value: 00h
Access: RO, RW/L
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E0000h–0E7FFFh.

Bit	Access & Default	Description
7:6	RO 00b	Reserved
5:4	RW/L 00b	**0E4000h–0E7FFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E4000h to 0E7FFFh. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM. This register is locked by Intel® TXT.
3:2	RO 00b	Reserved
1:0	RW/L 00b	**0E0000h–0E3FFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E0000h to 0E3FFFh. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM. This register is locked by Intel® TXT.

5.1.24 PAM6—Programmable Attribute Map 6

B/D/F/Type: 0/0/0/PCI
Address Offset: 96h
Default Value: 00h
Access: RO, RW/L
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E8000h–0EFFFFh.

Bit	Access & Default	Description
7:6	RO 00b	Reserved
5:4	RW/L 00b	**0EC000h–0EFFFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E4000h to 0E7FFFh. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM. This register is locked by Intel® TXT.
3:2	RO 00b	Reserved
1:0	RW/L 00b	**0E8000h–0EBFFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E0000h to 0E3FFFh. 00 = DRAM Disabled: Accesses are directed to DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM. This register is locked by Intel® TXT.

5.1.25 LAC—Legacy Access Control

B/D/F/Type: 0/0/0/PCI
Address Offset: 97h
Default Value: 00h
Access: RW/L, RO, RW
Size: 8 bits

This 8-bit register controls a fixed DRAM hole from 15–16 MB.

Bit	Access & Default	Description
7	RW/L 0b	**Hole Enable (HEN):** This field enables a memory hole in DRAM space. The DRAM that lies "behind" this space is not remapped. 0 = No memory hole. 1 = Memory hole from 15 MB to 16 MB. This bit is Intel® TXT lockable.
6:1	RO 00000b	Reserved
0	RW 0b	**MDA Present (MDAP): T**his bit works with the VGA Enable bits in the BCTRL register of Device 1 to control the routing of processor initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if device 1's VGA Enable bit is not set. If device 1's VGA enable bit is not set, then accesses to IO address range x3BCh–x3BFh are forwarded to DMI. If the VGA enable bit is set and MDA is not present, then accesses to IO address range x3BCh–x3BFh are forwarded to PCI Express if the address is within the corresponding IOBASE and IOLIMIT, otherwise they are forwarded to DMI. MDA resources are defined as the following: Memory: 0B0000h – 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to the DMI even if the reference includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: **VGAEN / MDAP / Description** 0 / 0 / All References to MDA and VGA space are routed to DMI 0 / 1 / Invalid combination 1 / 0 / All VGA and MDA references are routed to PCI Express Graphics Attach. 1 / 1 / All VGA references are routed to PCI Express Graphics Attach. MDA references are routed to DMI. VGA and MDA memory cycles can only be routed across the PEG when MAE (PCICMD1[1]) is set. VGA and MDA I/O cycles can only be routed across the PEG if IOAE (PCICMD1[0]) is set.

5.1.26 REMAPBASE—Remap Base Address Register

B/D/F/Type: 0/0/0/PCI
Address Offset: 98–99h
Default Value: 03FFh
Access: RO, RW/L
Size: 16 bits

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	RW/L 3FFh	**Remap Base Address [35:26] (REMAPBASE):** The value in this register defines the lower boundary of the Remap window. The Remap window is inclusive of this address. In the decoder A[25:0] of the Remap Base Address are assumed to be 0s. Thus, the bottom of the defined memory range will be aligned to a 64 MB boundary. When the value in this register is greater than the value programmed into the Remap Limit register, the Remap window is disabled. These bits are Intel® TXT lockable or ME stolen Memory lockable.

5.1.27 REMAPLIMIT—Remap Limit Address Register

B/D/F/Type: 0/0/0/PCI
Address Offset: 9A–9Bh
Default Value: 0000h
Access: RO, RW/L
Size: 16 bits

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	RW/L 000h	**Remap Limit Address [35:26] (REMAPLMT):** The value in this register defines the upper boundary of the Remap window. The Remap window is inclusive of this address. In the decoder A[25:0] of the remap limit address are assumed to be Fhs. Thus the top of the defined range will be one less than a 64 MB boundary. When the value in this register is less than the value programmed into the Remap Base register, the Remap window is disabled. These Bits are Intel® TXT lockable or ME stolen Memory lockable.

5.1.28 SMRAM—System Management RAM Control

B/D/F/Type: 0/0/0/PCI
Address Offset: 9Dh
Default Value: 02h
Access: RO, RW/L, RW, RW/L/K
Size: 8 bits

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. The Open, Close, and Lock bits function only when G_SMRAME bit is set to a 1. Also, the OPEN bit must be reset before the LOCK bit is set.

Bit	Access & Default	Description
7	RO 0b	Reserved
6	RW/L 0b	**SMM Space Open (D_OPEN):** When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.
5	RW 0b	**SMM Space Closed (D_CLS):** When D_CLS = 1 SMM space DRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DRAM. This will allow SMM software to reference through SMM space to update the display even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.
4	RW/L/K 0b	**SMM Space Locked (D_LCK):** When D_LCK is set to 1 then D_OPEN is reset to 0 and D_LCK, D_OPEN, C_BASE_SEG, H_SMRAM_EN, TSEG_SZ and TSEG_EN become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a Full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to "lock down" SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	RW/L 0b	**Global SMRAM Enable (G_SMRAME):** If set to a 1, then Compatible SMRAM functions are enabled, providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADSB with SMM decode). To enable Extended SMRAM function this bit has be set to 1. Refer to the section on SMM for more details. Once D_LCK is set, this bit becomes read only.
2:0	RO 0b	**Compatible SMM Space Base Segment (C_BASE_SEG):** This field indicates the location of SMM space. SMM DRAM is not remapped. It is simply made visible if the conditions are right to access SMM space, otherwise the access is forwarded to DMI. Since the (G)MCH supports only the SMM space between A0000 and BFFFF, this field is hardwired to 010.

5.1.29 ESMRAMC—Extended System Management RAM Control

B/D/F/Type: 0/0/0/PCI
Address Offset: 9Eh
Default Value: 38h
Access: RW/L, RWC, RO
Size: 8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM space. The Extended SMRAM (E_SMRAM) memory provides a write-back cacheable SMRAM memory space that is above 1 MB.

Bit	Access & Default	Description
7	RW/L 0b	**Enable High SMRAM (H_SMRAME):** This bit controls the SMM memory space location (i.e., above 1 MB or below 1 MB) When G_SMRAME is 1 and H_SMRAME is set to 1, the high SMRAM memory space is enabled. SMRAM accesses within the range 0FEDA0000h to 0FEDBFFFFh are remapped to DRAM addresses within the range 000A0000h to 000BFFFFh. Once D_LCK has been set, this bit becomes read only.
6	RWC 0b	**Invalid SMRAM Access (E_SMERR):** This bit is set when processor has accessed the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with the D-OPEN bit = 0. It is software's responsibility to clear this bit. The software must write a 1 to this bit to clear it.
5	RO 1b	**SMRAM Cacheable (SM_CACHE):** This bit is forced to 1 by the (G)MCH.
4	RO 1b	**L1 Cache Enable for SMRAM (SM_L1):** This bit is forced to 1 by the (G)MCH.
3	RO 1b	**L2 Cache Enable for SMRAM (SM_L2):** This bit is forced to 1 by the (G)MCH.
2:1	RW/L 00b	**TSEG Size (TSEG_SZ):** Selects the size of the TSEG memory block if enabled. Memory from the top of DRAM space is partitioned away so that it may only be accessed by the processor interface and only then when the SMM bit is set in the request packet. Non-SMM accesses to this memory region are sent to DMI when the TSEG memory block is enabled. 00 = 1 MB TSEG. (TOLUD – GTT Graphics Memory Size – Graphics Stolen Memory Size – 1 MB) to (TOLUD – GTT Graphics Memory Size – Graphics Stolen Memory Size). 01 = 2 MB TSEG. (TOLUD – GTT Graphics Memory Size – Graphics Stolen Memory Size – 2 MB) to (TOLUD – GTT Graphics Memory Size – Graphics Stolen Memory Size). 10 = 8 MB TSEG. (TOLUD – GTT Graphics Memory Size – Graphics Stolen Memory Size – 8 MB) to (TOLUD – GTT Graphics Memory Size – Graphics Stolen Memory Size). 11 = Reserved. Once D_LCK has been set, these bits becomes read only.

Bit	Access & Default	Description
0	RW/L 0b	**TSEG Enable (T_EN):** Enabling of SMRAM memory for Extended SMRAM space only. When G_SMRAME = 1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. Note that once D_LCK is set, this bit becomes read only.

5.1.30 TOM—Top of Memory

B/D/F/Type: 0/0/0/PCI
Address Offset: A0–A1h
Default Value: 0001h
Access: RO, RW/L
Size: 16 bits

This Register contains the size of physical memory. BIOS determines the memory size reported to the OS using this Register.

Bit	Access & Default	Description
15:10	RO 00h	Reserved
9:0	RW/L 001h	**Top of Memory (TOM):** This register reflects the total amount of populated physical memory. This is NOT necessarily the highest main memory address (holes may exist in main memory address map due to addresses allocated for memory mapped I/O). These bits correspond to address bits 35:26 (64 MB granularity). Bits 25:0 are assumed to be 0. All the bits in this register are locked in Intel® TXT mode.

5.1.31 TOUUD—Top of Upper Usable Dram

B/D/F/Type: 0/0/0/PCI
Address Offset: A2–A3h
Default Value: 0000h
Access: RW/L
Size: 16 bits

This 16 bit register defines the Top of Upper Usable DRAM.

Configuration software must set this value to TOM minus all EP stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to (reclaim limit + 1 byte) 64 MB aligned since reclaim limit is 64 MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than or equal to 4 GB.

These bits are Intel® TXT lockable.

Bit	Access & Default	Description
15:0	RW/L 0000h	**TOUUD (TOUUD):** This register contains bits 35 to 20 of an address one byte above the maximum DRAM memory above 4 G that is usable by the operating system. Configuration software must set this value to TOM minus all EP stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to (reclaim limit + 1 byte) 64 MB aligned since reclaim limit is 64 MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than 4 GB. All the Bits in this register are locked in Intel® TXT mode.

5.1.32 GBSM—Graphics Base of Stolen Memory

B/D/F/Type: 0/0/0/PCI
Address Offset: A4–A7h
Default Value: 00000000h
Access: RW/L, RO
Size: 32 bits

This register contains the base address of graphics data stolen DRAM memory. BIOS determines the base of graphics data stolen memory by subtracting the graphics data stolen memory size (PCI Device 0 offset 52 bits 7:4) from TOLUD (PCI Device 0, offset B0h, bits 15:4).

Note: This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.

Bit	Access & Default	Description
31:20	RW/L 000h	**Graphics Base of Stolen Memory (GBSM):** This register contains bits 31:20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size (PCI Device 0, offset 52h, bits 6:4) from TOLUD (PCI Device 0, offset B0h, bits 15:04). **Note:** This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.
19:0	RO 00000h	Reserved

5.1.33 BGSM—Base of GTT stolen Memory

B/D/F/Type: 0/0/0/PCI
Address Offset: A8–ABh
Default Value: 00000000h
Access: RW/L, RO
Size: 32 bits

This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 52 bits 9:8) from the graphics stolen memory base (PCI Device 0, offset A4h, bits 31:20).

Note: This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.

Bit	Access & Default	Description
31:20	RW/L 000h	**Graphics Base of Stolen Memory (GBSM):** This register contains bits 31:20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0, offset 52h, bits 9:8) from the graphics stolen memory base (PCI Device 0, offset A4h, bits 31:20). **Note:** This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.
19:0	RO 00000h	Reserved

5.1.34 TSEGMB—TSEG Memory Base

B/D/F/Type: 0/0/0/PCI
Address Offset: AC–AFh
Default Value: 00000000h
Access: RW/L, RO
Size: 32 bits

This register contains the base address of TSEG DRAM memory. BIOS determines the base of TSEG memory by subtracting the TSEG size (PCI Device 0, offset 9Eh, bits 2:1) from graphics GTT stolen base (PCI Device 0, offset A8h, bits 31:20).

Once D_LCK has been set, these bits becomes read only.

Bit	Access & Default	Description
31:20	RW/L 000h	**TESG Memory base (TSEGMB):** This register contains bits 31:20 of the base address of TSEG DRAM memory. BIOS determines the base of TSEG memory by subtracting the TSEG size (PCI Device 0, offset 9Eh, bits 2:1) from graphics GTT stolen base (PCI Device 0, offset A8h, bits 31:20). Once D_LCK has been set, these bits becomes read only.
19:0	RO 00000h	Reserved

5.1.35 TOLUD—Top of Low Usable DRAM

B/D/F/Type:	0/0/0/PCI
Address Offset:	B0–B1h
Default Value:	0010h
Access:	RW/L, RO
Size:	16 bits

This 16 bit register defines the Top of Low Usable DRAM. TSEG, GTT Graphics Memory and Graphics Stolen Memory are within the DRAM space defined. From the top, (G)MCH optionally claims 1 to 64 MB of DRAM for internal graphics if enabled 1, 2 MB of DRAM for GTT Graphics Stolen Memory (if enabled) and 1, 2, or 8 MB of DRAM for TSEG, if enabled.

Programming Example :

C1DRB3 is set to 4 GB

TSEG is enabled and TSEG size is set to 1 MB

Internal Graphics is enabled and Graphics Mode Select set to 32 MB

GTT Graphics Stolen Memory Size set to 2 MB

BIOS knows the OS requires 1 GB of PCI space.

BIOS also knows the range from FEC0_0000h to FFFF_FFFFh is not usable by the system. This 20MB range at the very top of addressable memory space is lost to APIC and Intel® TXT.

According to the above equation, TOLUD is originally calculated to: 4 GB = 1_0000_0000h

The system memory requirements are: 4GB (max addressable space) – 1 GB (PCI space) – 35 MB (lost memory) = 3 GB – 35 MB (minimum granularity) = ECB0_0000h

Since ECB0_0000h (PCI and other system requirements) is less than 1_0000_0000h, TOLUD should be programmed to ECBh.

These bits are Intel® TXT lockable.

Bit	Access & Default	Description
15:4	RW/L 001h	**Top of Low Usable DRAM (TOLUD):** This register contains bits 31:20 of an address one byte above the maximum DRAM memory below 4 GB that is usable by the operating system. Address bits 31:20 programmed to 01h implies a minimum memory size of 1 MB. Configuration software must set this value to the smaller of the following 2 choices: maximum amount memory in the system minus ME stolen memory plus one byte or the minimum address allocated for PCI memory. Address bits 19:0 are assumed to be 0_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register. Note that the Top of Low Usable DRAM is the lowest address above both Graphics Stolen memory and TSEG. BIOS determines the base of Graphics Stolen Memory by subtracting the Graphics Stolen Memory Size from TOLUD and further decrements by TSEG size to determine base of TSEG. All the Bits in this register are locked in Intel® TXT mode. This register must be 64 MB aligned when reclaim is enabled.
3:0	RO 0000b	Reserved

5.1.36 ERRSTS—Error Status

B/D/F/Type: 0/0/0/PCI
Address Offset: C8–C9h
Default Value: 0000h
Access: RO, RWC/S
Size: 16 bits

This register is used to report various error conditions via the SERR DMI messaging mechanism. An SERR DMI message is generated on a zero to one transition of any of these flags (if enabled by the ERRCMD and PCICMD registers).

These bits are set regardless of whether or not the SERR is enabled and generated. After the error processing is complete, the error logging mechanism can be unlocked by clearing the appropriate status bit by software writing a 1 to it.

Bit	Access & Default	Description
15	RO 0b	Reserved
14	RWC/S 0b	**Isochronous TBWRR Run Behind FIFO full (ITCV):** If set, this bit indicates a VC1 TBWRR is running behind, resulting in the slot timer to stop until the request is able to complete. If this bit is already set, then an interrupt message will not be sent on a new error event.

Bit	Access & Default	Description
13	RWC/S 0b	**Isochronous TBWRR Run behind FIFO put (ITSTV):** If set, this bit indicates a VC1 TBWRR request was put into the run behind. This will likely result in a resulting in a contract violation due to the (G)MCH Express port taking too long to service the isochronous request. If this bit is already set, then an interrupt message will not be sent on a new error event.
12	RWC/S 0b	**(G)MCH Software Generated Event for SMI (GSGESMI):** This indicates the source of the SMI was a Device 2 Software Event.
11	RWC/S 0b	**(G)MCH Thermal Sensor Event for SMI/SCI/SERR (GTSE):** This bit indicates that a (G)MCH Thermal Sensor trip has occurred and an SMI, SCI or SERR has been generated. The status bit is set only if a message is sent based on Thermal event enables in Error command, SMI command and SCI command registers. A trip point can generate one of SMI, SCI, or SERR interrupts (two or more per event is invalid). Multiple trip points can generate the same interrupt, if software chooses this mode, subsequent trips may be lost. If this bit is already set, then an interrupt message will not be sent on a new thermal sensor event.
10	RO 0b	Reserved
9	RWC/S 0b	**LOCK to non-DRAM Memory Flag (LCKF):** 1 = (G)MCH has detected a lock operation to memory space that did not map into DRAM.
8	RO 0b	Reserved
7	RWC/S 0b	**DRAM Throttle Flag (DTF):** 1 = DRAM Throttling condition occurred. 0 = Software has cleared this flag since the most recent throttling event.
6:0	RO 0s	Reserved

5.1.37 ERRCMD—Error Command

B/D/F/Type: 0/0/0/PCI
Address Offset: CA–CBh
Default Value: 0000h
Access: RO, RW
Size: 16 bits

This register controls the (G)MCH responses to various system errors. Since the (G)MCH does not have an SERR# signal, SERR messages are passed from the (G)MCH to the ICH over DMI.

When a bit in this register is set, a SERR message will be generated on DMI whenever the corresponding flag is set in the ERRSTS register. The actual generation of the SERR message is globally enabled for Device #0 via the PCI Command register.

Bit	Access & Default	Description
15:12	RO 0h	Reserved
11	RW 0b	**SERR on (G)MCH Thermal Sensor Event (TSESERR):** 1 = The (G)MCH generates a DMI SERR special cycle when bit 11 of the ERRSTS is set. The SERR must not be enabled at the same time as the SMI for the same thermal sensor event. 0 = Reporting of this condition via SERR messaging is disabled.
10	RO 0b	Reserved
9	RW 0b	**SERR on LOCK to non-DRAM Memory (LCKERR):** 1 = The (G)MCH will generate a DMI SERR special cycle whenever a processor lock cycle is detected that does not hit DRAM. 0 = Reporting of this condition via SERR messaging is disabled.
8:7	RW 00b	Reserved
6:0	RO 0s	Reserved

5.1.38 SMICMD—SMI Command

B/D/F/Type: 0/0/0/PCI
Address Offset: CC–CDh
Default Value: 0000h
Access: RO, RW
Size: 16 bits

This register enables various errors to generate an SMI DMI special cycle. When an error flag is set in the ERRSTS register, it can generate an SERR, SMI, or SCI DMI special cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers, respectively. Note that one and only one message type can be enabled.

Bit	Access & Default	Description
15:12	RO 0h	Reserved
11	RW 0b	**SMI on (G)MCH Thermal Sensor Trip (TSTSMI):** 1 = A SMI DMI special cycle is generated by (G)MCH when the thermal sensor trip requires an SMI. A thermal sensor trip point cannot generate more than one special cycle. 0 = Reporting of this condition via SMI messaging is disabled.
10:0	RO 0s	Reserved

5.1.39 SKPD—Scratchpad Data

B/D/F/Type: 0/0/0/PCI
Address Offset: DC–DFh
Default Value: 00000000h
Access: RW
Size: 32 bits

This register holds 32 writable bits with no functionality behind them. It is for the convenience of BIOS and graphics drivers.

Bit	Access & Default	Description
31:0	RW 00000000h	**Scratchpad Data (SKPD):** 1 DWord of data storage.

5.1.40 CAPID0—Capability Identifier

B/D/F/Type: 0/0/0/PCI
Address Offset: E0–EAh
Default Value: 00000100000000010B0009h
Access: RO
Size: 88 bits

Control of bits in this register are only required for customer visible SKU differentiation.

Bit	Access & Default	Description
87:79	RO 0s	Reserved
78	RO 0b	**82Q35, 82Q33, 82G33 GMCH** **Dual Independent Display Disable (DIDD):** This bit determines whether the component is capable of Dual Independent Display functionality. This functionality requires both functions (0 and 1) to be visible in the Internal Graphics Device 2. This capability is only meaningful if the component is capable of Internal Graphics. Definitions: • Clone mode – Same Image. Different display timing on each pipe. • Twin mode – Same Image. Same exact display timings. Extended Desktop mode – Unique images. Different display timings on each pipe. When Device 2 Function 1 is hidden, the second controller and its associated frame buffer are no longer visible to the Operating System. The OS thinks our device has only one display controller and stops supporting Extended Desktop mode. 0 = Capable of Dual Independent Display (independent frame buffers), Extended Desktop mode is supported. 1 = Not capable of Dual Independent Display. Hardwires bit 4 of the Device Enable (DEVEN) register (Device 0 Offset 54h) to '0'. Clone mode and twin mode are still supported (single frame buffer). **82P35 MCH** Reserved
77	RO 0b	**Dual Channel Disable (DCD):** 0 = Dual channel operation allowed 1 = Only single channel operation allowed

Bit	Access & Default	Description
76	RO 0b	**2 DIMMS per Channel Disable (2DPCD):** 0 = 2 DIMMs per channel Enabled 1 = 2 DIMMs per channel disabled. This setting hardwires bits 2 and 3 of the rank population field for each channel to zero. (MCHBAR offset 260h, bits 22–23 for channel 0 and MCHBAR offset 660h, bits 22–23 for channel 1)
75:73	RO 00b	Reserved
72	RO 0b	**Agent Presence Disable (APD):** 0 = Disable 1 = Enable
71	RO 0b	**System Defense Disable (CBD):** 0 = Disable 1 = Enable
70	RO 0b	**Multiprocessor Disable (MD):** 0 = (G)MCH capable of Multiple Processors 1 = (G)MCH capable of uni-processor only.
69	RO 0b	**FAN Speed Control Disable (FSCD):** 0 = Disable 1 = Enable
68	RO 0b	**EastFork Disable (EFD):** 0 = Disable 1 = Enable
67:58	RO 0s	Reserved
57	RO 0b	**ME Disable (MED):** 0 = ME feature is enabled 1 = ME feature is disabled
56:48	RO 0s	Reserved
47	RO 0b	**82Q35, 82Q33, 82G33 GMCH** **3D Integrated graphics Disable (3DIGD):** 0 = 3D Internal Graphics are enabled 1 = 3D Internal Graphics are disabled. VGA still supported **82P35 MCH** Reserved

Bit	Access & Default	Description
46	RO 0b	**82Q35, 82Q33, 82G33 GMCH** **Internal Graphics Disable (IGD):** 0 = There is a graphics engine within this GMCH. Internal Graphics Device (Device #2) is enabled and all of its memory and I/O spaces are accessible. Configuration cycles to Device 2 will be completed within the GMCH. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2 and VGA Enable of the PCI to PCI bridge control register in Device 1 (If PCI Express GFX attach is supported). A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the GMCH Control Register). Graphics Memory is pre-allocated above TSEG Memory. 1 = There is no graphics engine within this GMCH. Internal Graphics Device (Device #2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on to DMI. In addition, all clocks to internal graphics logic are turned off. All non-SMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control register in Device 1. DEVEN [4:3] (Device 0, offset 54h) have no meaning. Device 2 Functions 0 and 1 are disabled and hidden. **82P35 MCH** Reserved
45	RO 0b	**PEG Port x16 Disable (PEGX16D):** 0 = Capable of x16 PEG Port. 1 = Not Capable of x16 PEG port, instead PEG limited to x8 and below. Causes PEG port to enable and train logical lanes 7:0 only. Logical lanes 15:8 are powered down, and the Max Link Width field of the Link Capability register reports x8 instead of x16. (in the case of lane reversal, lanes 15:8 are active and lanes 7:0 are powered down)
44	RO 0b	**PCI Express Port Disable (PEGPD):** 0 = There is a PCI Express Port on this GMCH. Device 1 and associated memory spaces are accessible. All non-SIMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control register in Device 1 and VGA settings controlling internal graphics VGA if internal graphics is enabled. 1 = There is no PCI Express Port on this GMCH. Device 1 and associated memory and IO spaces are disabled by hardwiring the D1EN field bit 1 of the Device Enable register (DEVEN Dev 0 Offset 54h). In addition, Next_Pointer = 00h, VGA memory and IO cannot decode to the PCI Express interface. From a Physical Layer perspective, all 16 lanes are powered down and the link does not attempt to train.
43:39	RO 00000b	Reserved

Bit	Access & Default	Description
38	RO 0b	**DDR3 Disable (DDR3D):** 0 = Capable of supporting DDR3 SDRAM (82G33 GMCH and 82P35 MCH only) 1 = Not Capable of supporting DDR3 SDRAM
37:34	RO 0000b	Reserved
33:31	RO 000b	**DDR Frequency Capability (DDRFC):** This field controls which values may be written to the Memory Frequency Select field 6:4 of the Clocking Configuration registers (MCHBAR Offset C00h). Any attempt to write an unsupported value will be ignored. 000 = (G)MCH capable of "All" memory frequencies 001 = Reserved 010 = Reserved 011 = (G)MCH capable of up to DDR2/DDR3 1333 100 = (G)MCH capable of up to DDR2/DDR3 1067 101 = (G)MCH capable of up to DDR2/DDR3 800 110 = (G)MCH capable of up to DDR2/DDR3 667 NOTE: DDR3 is only supported on the 82G33 GMCH and 82P35 MCH components.
30:28	RO 000b	**FSB Frequency Capability (FSBFC):** This field controls which values are allowed in the PSB Frequency Select Field 2:0 of the Clocking Configuration Register. These values are determined by the BSEL[2:0] frequency straps. Any unsupported strap values will render the (G)MCH System Memory Interface inoperable. 000 = (G)MCH capable of "All" Memory Frequencies 001 = Reserved 010 = Reserved 011 = (G)MCH capable of up to PSB 1333 100 = (G)MCH capable of up to PSB 1067 101 = (G)MCH capable of up to PSB 800 110 = (G)MCH capable of up to PSB 667
27:24	RO 1h	**CAPID Version (CAPIDV):** This field has the value 0001b to identify the first revision of the CAPID register definition.
23:16	RO 0bh	**CAPID Length (CAPIDL):** This field has the value 0bh to indicate the structure length (11 bytes).
15:8	RO 00h	**Next Capability Pointer (NCP):** This field is hardwired to 00h indicating the end of the capabilities linked list.
7:0	RO 09h	**Capability Identifier (CAP_ID):** This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

5.2 MCHBAR

The MCHBAR registers are offset from the MCHBAR base address. Table 5-2 provides an address map of the registers listed by address offset in ascending order. Detailed register bit descriptions follow the table.

Table 5-2. MCHBAR Register Address Map

Address Offset	Register Symbol	Register Name	Default Value	Access
111h	CHDECMISC	Channel Decode Miscellaneous	00h	RW/L
200–01h	C0DRB0	Channel 0 DRAM Rank Boundary Address 0	0000h	RO, RW/L
202–203h	C0DRB1	Channel 0 DRAM Rank Boundary Address 1	0000h	RW/L, RO
204–205h	C0DRB2	Channel 0 DRAM Rank Boundary Address 2	0000h	RW/L, RO
206–207h	C0DRB3	Channel 0 DRAM Rank Boundary Address 3	0000h	RW/L, RO
208–209h	C0DRA01	Channel 0 DRAM Rank 0,1 Attribute	0000h	RW/L
20A–20Bh	C0DRA23	Channel 0 DRAM Rank 2,3 Attribute	0000h	RW/L
250–251h	C0CYCTRKPCHG	Channel 0 CYCTRK PCHG	0000h	RW, RO
252–255h	C0CYCTRKACT	Channel 0 CYCTRK ACT	00000000h	RW, RO
256–257h	C0CYCTRKWR	Channel 0 CYCTRK WR	0000h	RW
258–25Ah	C0CYCTRKRD	Channel 0 CYCTRK READ	000000h	RW, RO
25B–25Ch	C0CYCTRKREFR	Channel 0 CYCTRK REFR	0000h	RO, RW
260–263h	C0CKECTRL	Channel 0 CKE Control	00000800h	RO, RW, RW/L
269–26Eh	C0REFRCTRL	Channel 0 DRAM Refresh Control	021830000 C30h	RW, RO
29C–29Fh	C0ODTCTRL	Channel 0 ODT Control	00000000h	RO, RW
600–601h	C1DRB0	Channel 1 DRAM Rank Boundary Address 0	0000h	RW/L, RO
602–603h	C1DRB1	Channel 1 DRAM Rank Boundary Address 1	0000h	RW/L, RO
604–605h	C1DRB2	Channel 1 DRAM Rank Boundary Address 2	0000h	RW/L, RO
606–607h	C1DRB3	Channel 1 DRAM Rank Boundary Address 3	0000h	RW/L, RO

Address Offset	Register Symbol	Register Name	Default Value	Access
608–609h	C1DRA01	Channel 1 DRAM Rank 0,1 Attributes	0000h	RW/L,
60A–60Bh	C1DRA23	Channel 1 DRAM Rank 2,3 Attributes	0000h	RW/L
650–651h	C1CYCTRKPCHG	Channel 1 CYCTRK PCHG	0000h	RO, RW
652–655h	C1CYCTRKACT	Channel 1 CYCTRK ACT	00000000h	RO, RW
656–657h	C1CYCTRKWR	Channel 1 CYCTRK WR	0000h	RW,
658–65Ah	C1CYCTRKRD	Channel 1 CYCTRK READ	000000h	RO, RW
660–663h	C1CKECTRL	Channel 1 CKE Control	00000800h	RW/L, RW, RO
669–66Eh	C1REFRCTRL	Channel 1 DRAM Refresh Control	021830000 C30h	RW, RO
69C–69Fh	C1ODTCTRL	Channel 1 ODT Control	00000000h	RO, RW
A00– A01h	EPC0DRB0	EP Channel 0 DRAM Rank Boundary Address 0	0000h	RW, RO
A02– A03h	EPC0DRB1	EP Channel 0 DRAM Rank Boundary Address 1	0000h	RO, RW
A04– A05h	EPC0DRB2	EP Channel 0 DRAM Rank Boundary Address 2	0000h	RO, RW
A06– A07h	EPC0DRB3	EP Channel 0 DRAM Rank Boundary Address 3	0000h	RW, RO
A08– A09h	EPC0DRA01	EP Channel 0 DRAM Rank 0,1 Attribute	0000h	RW
A0A– A0Bh	EPC0DRA23	EP Channel 0 DRAM Rank 2,3 Attribute	0000h	RW
A19– A1Ah	EPDCYCTRKWRTPRE	EPD CYCTRK WRT PRE	0000h	RW, RO
A1C– A1Fh	EPDCYCTRKWRTACT	EPD CYCTRK WRT ACT	00000000h	RO, RW
A20– A21h	EPDCYCTRKWRTWR	EPD CYCTRK WRT WR	0000h	RW, RO
A22– A23h	EPDCYCTRKWRTREF	EPD CYCTRK WRT REF	0000h	RO, RW
A24– A26h	EPDCYCTRKWRTRD	EPD CYCTRK WRT READ	000000h	RW
A28– A33h	EPDCKECONFIGREG	EPD CKE related configuration registers	00E0000000 h	RW
A2Eh	MEMEMSPACE	ME Memory Space Configuration	00h	RW, RO
A30–A33h	EPDREFCONFIG	EP DRAM Refresh Configuration	40000C30h	RO, RW
CD8h	TSC1	Thermal Sensor Control 1	00h	RW/L, RW, RS/WC

Address Offset	Register Symbol	Register Name	Default Value	Access
CD9h	TSC2	Thermal Sensor Control 2	00h	RW/L, RO
CDAh	TSS	Thermal Sensor Status	00h	RO
CDC–CDFh	TSTTP	Thermal Sensor Temperature Trip Point	00000000h	RO, RW, RW/L
CE2h	TCO	Thermal Calibration Offset	00h	RW/L/K, RW/L
CE4h	THERM1	Hardware Throttle Control	00h	RW/L, RO, RW/L/K
CEA–CEBh	TIS	Thermal Interrupt Status	0000h	RO, RWC
CF1h	TSMICMD	Thermal SMI Command	00h	RO, RW
F14–F17h	PMSTS	Power Management Status	00000000h	RWC/S, RO

5.2.1 CHDECMISC—Channel Decode Miscellaneous

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 111h
Default Value: 00h
Access: RW/L
Size: 8 bits

This register has Miscellaneous CHDEC/MAGEN configuration bits.

Bit	Access & Default	Description
7	RW/L 0b	Reserved
6:5	RW/L 00b	**Enhanced Mode Select (ENHMODESEL):** 00 = Swap Enabled for Bank Selects and Rank Selects 01 = XOR Enabled for Bank Selects and Rank Selects 10 = Swap Enabled for Bank Selects only 11 = XOR Enabled for Bank Select only This register is locked by ME stolen Memory lock.
4	RW/L 0b	**Ch2 Enhanced Mode (CH2_ENHMODE):** This bit enables Enhanced addressing mode of operation is enabled for Ch 2. 0 = Disable 1 = Enable
3	RW/L 0b	**Ch1 Enhanced Mode (CH1_ENHMODE):** This bit enables Enhanced addressing mode of operation is enabled for Ch 1. 0 = Disable 1 = Enable
2	RW/L 0b	**Ch0 Enhanced Mode (CH0_ENHMODE):** This bit enables Enhanced addressing mode of operation is enabled for Ch 0. 0 = Disable 1 = Enable
1	RW/L 0b	Reserved
0	RW/L 0b	**EP Present (EPPRSNT):** This bit indicates whether EP UMA is present in the system or not. 0 = Not Present 1 = Present This register is locked by ME stolen Memory lock.

5.2.2 C0DRB0—Channel 0 DRAM Rank Boundary Address 0

B/D/F/Type:	0/0/0/MCHBAR
Address Offset:	200–201h
Default Value:	0000h
Access:	R/W, RO
Size:	16 bits

The DRAM Rank Boundary Registers define the upper boundary address of each DRAM rank with a granularity of 64 MB. Each rank has its own single-word DRB register. These registers are used to determine which chip select will be active for a given address. Channel and rank map:

Ch 0, Rank 0 = 200h
Ch 0, Rank 1 = 202h
Ch 0, Rank 2 = 204h
Ch 0, Rank 3 = 206h
Ch 1, Rank 0 = 600h
Ch 1, Rank 1 = 602h
Ch 1, Rank 2 = 604h
Ch 1, Rank 3 = 606h

Programming Guide

If Channel 0 is empty, all of the C0DRBs are programmed with 00h.

C0DRB0 = Total memory in Ch 0, Rank 0 (in 64 MB increments)
C0DRB1 = Total memory in Ch 0, Rank 0 + Ch 0, Rank 1 (in 64 MB increments)
...

If Channel 1 is empty, all of the C1DRBs are programmed with 00h

C1DRB0= Total memory in Ch 1, Rank 0 (in 64 MB increments)
C1DRB1= Total memory in Ch 1, Rank 0 + Ch 1, Rank 1 (in 64 MB increments)
...

For Flex Memory Mode

C1DRB0, C1DRB1, and C1DRB2:

They are also programmed similar to non-Flex mode. Only exception is, the DRBs corresponding to the top most populated rank and higher ranks in Channel 1 must be programmed with the value of the total Channel 1 population plus the value of total Channel 0 population (C0DRB3).

Example: If only Ranks 0 and 1 are populated in Ch1 in Flex mode, then:

C1DRB0 = Total memory in Ch 1, Rank 0 (in 64MB increments)

C1DRB1 = C0DRB3 + Total memory in Ch 1, Rank 0 + Ch 1, Rank 1 (in 64 MB increments) (Rank 1 is the topmost populated rank)

C1DRB2 = C1DRB1

C1DRB3 = C1DRB1

C1DRB3:

C1DRB3 = C0DRB3 + Total memory in Channel 1.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	R/W 000h	**Channel 0 Dram Rank Boundary Address 0 (C0DRBA0):** This register defines the DRAM rank boundary for rank0 of Channel 0 (64 MB granularity) = R0 R0 = Total Rank 0 memory size is 64 MB R1 = Total Rank 1 memory size is 64 MB R2 = Total Rank 2 memory size is 64 MB R3 = Total Rank 3 memory size is 64 MB

5.2.3 C0DRB1—Channel 0 DRAM Rank Boundary Address 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 202–203h
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

See C0DRB0 register for programming information.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	R/W 000h	**Channel 0 Dram Rank Boundary Address 1 (C0DRBA1):** This register defines the DRAM rank boundary for rank1 of Channel 0 (64 MB granularity) = (R1 + R0) R0 = Total Rank 0 memory size is 64 MB R1 = Total Rank 1 memory size is 64 MB R2 = Total Rank 2 memory size is 64 MB R3 = Total Rank 3 memory size is 64 MB

5.2.4 C0DRB2—Channel 0 DRAM Rank Boundary Address 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 204–205h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

See C0DRB0 register for programming information.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	R/W 000h	**Channel 0 DRAM Rank Boundary Address 2 (C0DRBA2):** This register defines the DRAM rank boundary for rank2 of Channel 0 (64 MB granularity) = (R2 + R1 + R0) R0 = Total Rank 0 memory size is 64 MB R1 = Total Rank 1 memory size is 64 MB R2 = Total Rank 2 memory size is 64 MB R3 = Total Rank 3 memory size is 64 MB

5.2.5 C0DRB3—Channel 0 DRAM Rank Boundary Address 3

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 206–207h
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

See C0DRB0 register for programming information.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	R/W 000h	**Channel 0 DRAM Rank Boundary Address 3 (C0DRBA3):** This register defines the DRAM rank boundary for rank3 of Channel 0 (64 MB granularity) = (R3 + R2 + R1 + R0) R0 = Total Rank 0 memory size is 64 MB R1 = Total Rank 1 memory size is 64 MB R2 = Total Rank 2 memory size is 64 MB R3 = Total Rank 3 memory size is 64 MB

5.2.6 C0DRA01—Channel 0 DRAM Rank 0,1 Attribute

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 208–209h
Default Value: 0000h
Access: R/W
Size: 16 bits

The DRAM Rank Attribute Registers define the page sizes/number of banks to be used when accessing different ranks. These registers should be left with their default value (all zeros) for any rank that is unpopulated, as determined by the corresponding CxDRB registers. Each byte of information in the CxDRA registers describes the page size of a pair of ranks. Channel and rank map:

Ch 0, Rank 0, 1= 208h–209h
Ch 0, Rank 2, 3 = 20Ah–20Bh
Ch 1, Rank 0, 1= 608h–609h
Ch 1, Rank 2, 3= 60Ah–60Bh

DRA[7:0] = "00" means Cfg 0 , DRA[7:0] ="01" means Cfg 1 .... DRA[7:0] = "09" means Cfg 9 and so on.

Table 5-3. DRAM Rank Attribute Register Programming

Tech	DDRx	Depth	Width	Row	Col	Bank	Row Size	Page Size
512Mb	2	64M	8	14	10	2	512 MB	8k
512Mb	2	32M	16	13	10	2	256 MB	8k
512Mb	3	64M	8	13	10	3	512 MB	8k
512Mb	3	32M	16	12	10	3	256 MB	8k
1 Gb	2,3	128M	8	14	10	3	1 GB	8k
1 Gb	2,3	64M	16	13	10	3	512 MB	8k

NOTE: DDR3 is only supported on the 82G33 GMCH and 82P35 MCH components.

Bit	Access & Default	Description
15:8	R/W 00h	**Channel 0 DRAM Rank-1 Attributes (C0DRA1):** This field defines DRAM pagesize/number-of-banks for rank1 for given channel. See Table 5-3 for programming.
7:0	R/W 00h	**Channel 0 DRAM Rank-0 Attributes (C0DRA0):** This field defines DRAM page size/number-of-banks for rank0 for given channel. See Table 5-3 for programming.

5.2.7 C0DRA23—Channel 0 DRAM Rank 2,3 Attribute

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 20A–20Bh
Default Value: 0000h
Access: R/W
Size: 16 bits

See C0DRA01 register for programming information.

Bit	Access & Default	Description
15:8	R/W 00h	**Channel 0 DRAM Rank-3 Attributes (CODRA3):** This register defines DRAM pagesize/number-of-banks for rank3 for given channel. See Table 5-3 for programming.
7:0	R/W 00h	**Channel 0 DRAM Rank-2 Attributes (CODRA2):** This register defines DRAM pagesize/number-of-banks for rank2 for given channel. See Table 5-3 for programming.

5.2.8 C0CYCTRKPCHG—Channel 0 CYCTRK PCHG

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 250–251h
Default Value: 0000h
Access: RW, RO
Size: 16 bits

This register provides Channel 0 CYCTRK Precharge.

Bit	Access & Default	Description
15:11	RO 00000b	Reserved
10:6	RW 00000b	**Write To PRE Delayed (C0sd_cr_wr_pchg):** This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and PRE commands to the same rank-bank. This field corresponds to t_{WR} in the DDR Specification.
5:2	RW 0000b	**READ To PRE Delayed (C0sd_cr_rd_pchg):** This field indicates the minimum allowed spacing (in DRAM clocks) between the READ and PRE commands to the same rank-bank.
1:0	RW 00b	**PRE To PRE Delayed (C0sd_cr_pchg_pchg):** This field indicates the minimum allowed spacing (in DRAM clocks) between two PRE commands to the same rank.

5.2.9 C0CYCTRKACT—Channel 0 CYCTRK ACT

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 252–255h
Default Value: 00000000h
Access: RW, RO
Size: 32 bits

This register provides Channel 0 CYCTRK Activate.

Bit	Access & Default	Description
31:28	RO 0h	Reserved
27:22	RW 000000b	**ACT Window Count (C0sd_cr_act_windowcnt):** This field indicates the window duration (in DRAM clocks) during which the controller counts the # of activate commands which are launched to a particular rank. If the number of activate commands launched within this window is greater than 4, then a check is implemented to block launch of further activates to this rank for the rest of the duration of this window.
21	RW 0b	**Max ACT Check Disable (C0sd_cr_maxact_dischk):** This field disenables the check which ensures that there are no more than four activates to a particular rank in a given window.
20:17	RW 0000b	**ACT to ACT Delayed (C0sd_cr_act_act[):** This field indicates the minimum allowed spacing (in DRAM clocks) between two ACT commands to the same rank. This field corresponds to t_{RRD} in the DDR Specification.
16:13	RW 0000b	**PRE to ACT Delayed (C0sd_cr_pre_act):** This field indicates the minimum allowed spacing (in DRAM clocks) between the PRE and ACT commands to the same rank-bank. This field corresponds to t_{RP} in the DDR Specification.
12:9	RW 0h	**ALLPRE to ACT Delay (C0sd0_cr_preall_act):** From the launch of a prechargeall command wait for these many # of memory clocks before launching a activate command. This field corresponds to t_{PALL_RP}.
8:0	RW 00000000 0b	**REF to ACT Delayed (C0sd_cr_rfsh_act):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between REF and ACT commands to the same rank. This field corresponds to t_{RFC} in the DDR Specification.

5.2.10 C0CYCTRKWR—Channel 0 CYCTRK WR

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 256–257h
Default Value: 0000h
Access: RW
Size: 16 bits

This register provides Channel 0 CYCTRK WR.

Bit	Access & Default	Description
15:12	RW 0h	**ACT To Write Delay (C0sd_cr_act_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and WRITE commands to the same rank-bank. This field corresponds to t_{RCD_wr} in the DDR Specification.
11:8	RW 0h	**Same Rank Write To Write Delay (C0sd_cr_wrsr_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between two WRITE commands to the same rank.
7:4	RW 0h	**Different Rank Write to Write Delay (C0sd_cr_wrdr_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between two WRITE commands to different ranks. This field corresponds to t_{WR_WR} in the DDR Specification.
3:0	RW 0h	**READ To WRTE Delay (C0sd_cr_rd_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between the READ and WRITE commands. This field corresponds to t_{RD_WR}.

5.2.11 C0CYCTRKRD—Channel 0 CYCTRK READ

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 258–25Ah
Default Value: 000000h
Access: RW, RO
Size: 24 bits

This register provides Channel 0 CYCTRK RD.

Bit	Access & Default	Description
23:21	RO 000b	Reserved
20:17	RW 0h	**Min ACT To READ Delay (C0sd_cr_act_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and READ commands to the same rank-bank. This field corresponds to t_{RCD_rd} in the DDR Specification.
16:12	RW 00000b	**Same Rank Write To READ Delay (C0sd_cr_wrsr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and READ commands to the same rank. This field corresponds to t_{WTR} in the DDR Specification.
11:8	RW 0000b	**Different Ranks Write To READ Delay (C0sd_cr_wrdr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and READ commands to different ranks. This field corresponds to t_{WR_RD} in the DDR Specification.
7:4	RW 0000b	**Same Rank Read To Read Delay (C0sd_cr_rdsr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between two READ commands to the same rank.
3:0	RW 0000b	**Different Ranks Read To Read Delay (C0sd_cr_rddr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between two READ commands to different ranks. This field corresponds to t_{RD_RD}.

5.2.12 C0CYCTRKREFR—Channel 0 CYCTRK REFR

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 25B–25Ch
Default Value: 0000h
Access: RO, RW
Size: 16 bits

This register provides Channel 0 CYCTRK Refresh.

Bit	Access & Default	Description
15:13	RO 000b	Reserved
12:9	RW 0000b	**Same Rank PALL to REF Delay (C0sd_cr_pchgall_rfsh):** This field indicates the minimum allowed spacing (in DRAM clocks) between the PRE-ALL and REF commands to the same rank.
8:0	RW 000000000b	**Same Rank REF to REF Delay (C0sd_cr_rfsh_rfsh):** This field indicates the minimum allowed spacing (in DRAM clocks) between two REF commands to **same** ranks.

5.2.13 C0CKECTRL—Channel 0 CKE Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 260–263h
Default Value: 00000800h
Access: RO, RW, RW/L
Size: 32 bits

This register provides CKE controls for Channel 0

Bit	Access & Default	Description
31:28	RO 0000b	Reserved
27	RW 0b	**start the self-refresh exit sequence (sd0_cr_srcstart):** This field indicates the request to start the self-refresh exit sequence.
26:24	RW 000b	**CKE pulse width requirement in high phase (sd0_cr_cke_pw_hl_safe):** This field indicates CKE pulse width requirement in high phase. This field corresponds to t_{CKE} (high) in the DDR Specification.
23	RW/L 0b	**Rank 3 Population (sd0_cr_rankpop3):** 1 = Rank 3 populated 0 = Rank 3 not populated This register is locked by ME stolen Memory lock.
22	RW/L 0b	**Rank 2 Population (sd0_cr_rankpop2):** 1 = Rank 2 populated 0 = Rank 2 not populated This register is locked by ME stolen Memory lock.
21	RW/L 0b	**Rank 1 Population (sd0_cr_rankpop1):** 1 = Rank 1 populated 0 = Rank 1 not populated This register is locked by ME stolen Memory lock.
20	RW/L 0b	**Rank 0 Population (sd0_cr_rankpop0):** 1 = Rank 0 populated 0 = Rank 0 not populated This register is locked by ME stolen Memory lock.
19:17	RW 000b	**CKE pulse width requirement in low phase (sd0_cr_cke_pw_lh_safe):** This field indicates CKE pulse width requirement in low phase. This field corresponds to t_{CKE} (low) in the DDR Specification.
16	RW 0b	**Enable CKE toggle for PDN entry/exit (sd0_cr_pdn_enable):** This bit indicates that the toggling of CKEs (for PDN entry/exit) is enabled.
15:14	RO 00b	Reserved

Bit	Access & Default	Description
13:10	RW 0010b	**Minimum Powerdown exit to Non-Read command spacing (sd0_cr_txp):** This field indicates the minimum number of clocks to wait following assertion of CKE before issuing a non-read command. 0000–0001 = Reserved 0010–1001 = 2–9clocks 1010–1111 = Reserved
9:1	RW 00000000 0b	**Self refresh exit count (sd0_cr_slfrfsh_exit_cnt):** This field indicates the Self refresh exit count. (Program to 255). This field corresponds to t_{XSNR}/t_{XSRD} in the DDR Specification.
0	RW 0b	**Indicates only 1 DIMM populated (sd0_cr_singledimmpop):** This bit, when set, indicates that only 1 DIMM is populated.

5.2.14 C0REFRCTRL—Channel 0 DRAM Refresh Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 269–26Eh
Default Value: 021830000C30h
Access: RW, RO
Size: 48 bits

This register provides settings to configure the DRAM refresh controller.

Bit	Access & Default	Description
47:42	RO 00h	Reserved
41:37	RW 10000b	**Direct Rcomp Quiet Window (DIRQUIET):** This field indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.
36:32	RW 11000b	**Indirect Rcomp Quiet Window (INDIRQUIET):** This field indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.
31:27	RW 00110b	**Rcomp Wait (RCOMPWAIT):** This field indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.
26	RW 0b	Reserved

Bit	Access & Default	Description
25	RW 0b	**Refresh Counter Enable (REFCNTEN):** This bit is used to enable the refresh counter to count during times that DRAM is not in self-refresh, but refreshes are not enabled. Such a condition may occur due to need to reprogram DIMMs following DRAM controller switch. This bit has no effect when Refresh is enabled (i.e., there is no mode where Refresh is enabled but the counter does not run). Thus, in conjunction with bit 23 REFEN, the modes are: **REFEN:REFCNTEN** — **Description** 0:0 — Normal refresh disable 0:1 — Refresh disabled, but counter is accumulating refreshes. 1:X — Normal refresh enable
24	RW 0b	**All Rank Refresh (ALLRKREF):** This configuration bit enables (by default) that all the ranks are refreshed in a staggered/atomic fashion. If set, the ranks are refreshed in an independent fashion.
23	RW 0b	**Refresh Enable (REFEN):** Refresh is enabled. 0 = Disabled 1 = Enabled
22	RW 0b	**DDR Initialization Done (INITDONE):** Indicates that DDR initialization is complete. 0 = Not Done 1 = Done
21:20	RW 00b	Reserved
19:18	RW 00b	**DRAM Refresh Panic Watermark (REFPANICWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_panic flag is set. 00 = 5 01 = 6 10 = 7 11 = 8
17:16	RW 00b	**DRAM Refresh High Watermark (REFHIGHWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_high flag is set. 00 = 3 01 = 4 10 = 5 11 = 6

Bit	Access & Default	Description
15:14	RW 00b	**DRAM Refresh Low Watermark (REFLOWWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_low flag is set. 00 = 1 01 = 2 10 = 3 11 = 4
13:0	RW 001100001 10000b	**Refresh Counter Time Out Value (REFTIMEOUT):** Program this field with a value that will provide 7.8 us at the memory clock frequency. At various memory clock frequencies this results in the following values: 667 MHz -> 1450 hex

5.2.15 C0ODTCTRL—Channel 0 ODT Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 29C–29Fh
Default Value: 00000000h
Access: RO, RW
Size: 32 bits

This register provides ODT controls.

Bit	Access & Default	Description
31:12	RO 00000h	Reserved
11:8	RW 0000b	Reserved
7:4	RW 0000b	Reserved
3:0	RW 0000b	Reserved

5.2.16 C1DRB0—Channel 1 DRAM Rank Boundary Address 0

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 600–601h
Default Value: 0000h
Access: RW/L, RO
Size: 16 bits

The operation of this register is detailed in the description for register C0DRB0.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	RW/L 000h	**Channel 1 DRAM Rank Boundary Address 0 (C1DRBA0):** See C0DRB0 register. In stacked mode, if this is the topmost populated rank in Channel 1, program this value to be cumulative of Ch0 DRB3. This register is locked by ME stolen Memory lock.

5.2.17 C1DRB1—Channel 1 DRAM Rank Boundary Address 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 602–603h
Default Value: 0000h
Access: RW/L, RO
Size: 16 bits

The operation of this register is detailed in the description for register C0DRB0.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	RW/L 000h	**Channel 1 DRAM Rank Boundary Address 1 (C1DRBA1):** See C0DRB1 register. In stacked mode, if this is the topmost populated rank in Channel 1, program this value to be cumulative of Ch0 DRB3. This register is locked by ME stolen Memory lock.

5.2.18 C1DRB2—Channel 1 DRAM Rank Boundary Address 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 604–605h
Default Value: 0000h
Access: RW/L, RO
Size: 16 bits

The operation of this register is detailed in the description for register C0DRB0.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	RW/L 000h	**Channel 1 DRAM Rank Boundary Address 2 (C1DRBA2):** See C0DRB2 register. In stacked mode, if this is the topmost populated rank in Channel 1, program this value to be cumulative of Ch0 DRB3. This register is locked by ME stolen Memory lock.

5.2.19 C1DRB3—Channel 1 DRAM Rank Boundary Address 3

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 606–607h
Default Value: 0000h
Access: RW/L, RO
Size: 16 bits

The operation of this register is detailed in the description for register C0DRB0.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	RW/L 000h	**Channel 1 DRAM Rank Boundary Address 3 (C1DRBA3):** See C0DRB3 register. In stacked mode, this will be cumulative of Ch0 DRB3. This register is locked by ME stolen Memory lock.

5.2.20 C1DRA01—Channel 1 DRAM Rank 0,1 Attributes

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 608–609h
Default Value: 0000h
Access: RW/L
Size: 16 bits

The operation of this register is detailed in the description for register C0DRA01.

Bit	Access & Default	Description
15:8	RW/L 00h	**Channel 1 DRAM Rank-1 Attributes (C1DRA1):** See C0DRA1 register. This register is locked by ME stolen Memory lock.
7:0	RW/L 00h	**Channel 1 DRAM Rank-0 Attributes (C1DRA0):** See C0DRA0 register. This register is locked by ME stolen Memory lock.

5.2.21 C1DRA23—Channel 1 DRAM Rank 2,3 Attributes

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 60A–60Bh
Default Value: 0000h
Access: RW/L
Size: 16 bits

The operation of this register is detailed in the description for register C0DRA01.

Bit	Access & Default	Description
15:8	RW/L 00h	**Channel 1 DRAM Rank-3 Attributes (C1DRA3):** See C0DRA3 register. This register is locked by ME stolen Memory lock.
7:0	RW/L 00h	**Channel 1 DRAM Rank-2 Attributes (C1DRA2):** See C0DRA2 register. This register is locked by ME stolen Memory lock.

5.2.22 C1CYCTRKPCHG—Channel 1 CYCTRK PCHG

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 650–651h
Default Value: 0000h
Access: RO, RW
Size: 16 bits

This register provides Channel 1 CYCTRK Precharge.

Bit	Access & Default	Description
15:11	RO 00000b	Reserved
10:6	RW 00000b	**Write To PRE Delayed (C1sd_cr_wr_pchg):** This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and PRE commands to the same rank-bank. This field corresponds to t_{WR} in the DDR Specification.
5:2	RW 0000b	**READ To PRE Delayed (C1sd_cr_rd_pchg):** This field indicates the minimum allowed spacing (in DRAM clocks) between the READ and PRE commands to the same rank-bank
1:0	RW 00b	**PRE To PRE Delayed (C1sd_cr_pchg_pchg):** This field indicates the minimum allowed spacing (in DRAM clocks) between two PRE commands to the same rank.

5.2.23 C1CYCTRKACT—Channel 1 CYCTRK ACT

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 652–655h
Default Value: 00000000h
Access: RO, RW
Size: 32 bits

This register provides Channel 1 CYCTRK ACT.

Bit	Access & Default	Description
31:28	RO 0h	Reserved
27:22	RW 000000b	**ACT Window Count (C1sd_cr_act_windowcnt):** This field indicates the window duration (in DRAM clocks) during which the controller counts the # of activate commands which are launched to a particular rank. If the number of activate commands launched within this window is greater than 4, then a check is implemented to block launch of further activates to this rank for the rest of the duration of this window.
21	RW 0b	**Max ACT Check Disable (C1sd_cr_maxact_dischk):** This field disenables the check which ensures that there are no more than four activates to a particular rank in a given window.
20:17	RW 0000b	**ACT to ACT Delayed (C1sd_cr_act_act[):** This field indicates the minimum allowed spacing (in DRAM clocks) between two ACT commands to the same rank. This field corresponds to t_{RRD} in the DDR Specification.
16:13	RW 0000b	**PRE to ACT Delayed (C1sd_cr_pre_act):** This field indicates the minimum allowed spacing (in DRAM clocks) between the PRE and ACT commands to the same rank-bank:12:9R/W0000bPRE-ALL to ACT Delayed (C1sd_cr_preall_act): This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the PRE-ALL and ACT commands to the same rank. This field corresponds to t_{RP} in the DDR Specification.
12:9	RW 0h	**ALLPRE to ACT Delay (C1sd_cr_preall_act):** From the launch of a Prechargeall command wait for these many # of memory clocks before launching a activate command. This field corresponds to t_{PALL_RP}.
8:0	RW 00000000 0b	**REF to ACT Delayed (C1sd_cr_rfsh_act):** This field indicates the minimum allowed spacing (in DRAM clocks) between REF and ACT commands to the same rank. This field corresponds to t_{RFC} in the DDR Specification.

5.2.24 C1CYCTRKWR—Channel 1 CYCTRK WR

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 656–657h
Default Value: 0000h
Access: RW
Size: 16 bits

This register provides Channel 1 CYCTRK WR.

Bit	Access & Default	Description
15:12	RW 0h	**ACT To Write Delay (C1sd_cr_act_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and WRITE commands to the same rank-bank. This field corresponds to t_{RCD_wr} in the DDR Specification.
11:8	RW 0h	**Same Rank Write To Write Delayed (C1sd_cr_wrsr_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between two WRITE commands to the same rank.
7:4	RW 0h	**Different Rank Write to Write Delay (C1sd_cr_wrdr_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between two WRITE commands to different ranks. This field corresponds to t_{WR_WR} in the DDR Specification.
3:0	RW 0h	**READ To WRTE Delay (C1sd_cr_rd_wr):** This field indicates the minimum allowed spacing (in DRAM clocks) between the READ and WRITE commands. This field corresponds to t_{RD_WR}.

5.2.25 C1CYCTRKRD—Channel 1 CYCTRK READ

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 658–65Ah
Default Value: 000000h
Access: RO, RW
Size: 24 bits

This is the Channel 1 CYCTRK READ register.

Bit	Access & Default	Description
23:21	RO 0h	Reserved
20:17	RW 0h	**Min ACT To READ Delayed (C1sd_cr_act_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and READ commands to the same rank-bank. This field corresponds to t_{RCD_rd} in the DDR Specification.
16:12	RW 00000b	**Same Rank Write To READ Delayed (C1sd_cr_wrsr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and READ commands to the same rank. This field corresponds to t_{WTR} in the DDR Specification.
11:8	RW 0000b	**Different Ranks Write To READ Delayed (C1sd_cr_wrdr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and READ commands to different ranks. This field corresponds to t_{WR_RD} in the DDR Specification.
7:4	RW 0000b	**Same Rank Read To Read Delayed (C1sd_cr_rdsr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between two READ commands to the same rank.
3:0	RW 0000b	**Different Ranks Read To Read Delayed (C1sd_cr_rddr_rd):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between two READ commands to different ranks. This field corresponds to t_{RD_RD}.

5.2.26 C1CKECTRL—Channel 1 CKE Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 660–663h
Default Value: 00000800h
Access: RW/L, RW, RO
Size: 32 bits

This register provides Channel 1 CKE Controls.

Bit	Access & Default	Description
31:28	RO 0h	Reserved
27	RW 0b	**start the self-refresh exit sequence (sd1_cr_srcstart):** This field indicates the request to start the self-refresh exit sequence.
26:24	RW 000b	**CKE pulse width requirement in high phase (sd1_cr_cke_pw_hl_safe):** This field indicates CKE pulse width requirement in high phase. This field corresponds to t_{CKE} (high) in the DDR Specification.
23	RW/L 0b	**Rank 3 Population (sd1_cr_rankpop3):** 1 = Rank 3 populated 0 = Rank 3 not populated. This register is locked by ME stolen Memory lock.
22	RW/L 0b	**Rank 2 Population (sd1_cr_rankpop2):** 1 = Rank 2 populated 0 = Rank 2 not populated This register is locked by ME stolen Memory lock.
21	RW/L 0b	**Rank 1 Population (sd1_cr_rankpop1):** 1 = Rank 1 populated 0 = Rank 1 not populated. This register is locked by ME stolen Memory lock.
20	RW/L 0b	**Rank 0 Population (sd1_cr_rankpop0):** 1 = Rank 0 populated 0 = Rank 0 not populated This register is locked by ME stolen Memory lock.
19:17	RW 000b	**CKE pulse width requirement in low phase (sd1_cr_cke_pw_lh_safe):** This configuration register indicates CKE pulse width requirement in low phase. This field corresponds to t_{CKE} (low) in the DDR Specification.
16	RW 0b	**Enable CKE toggle for PDN entry/exit (sd1_cr_pdn_enable):** This configuration bit indicates that the toggling of CKEs (for PDN entry/exit) is enabled.

Bit	Access & Default	Description
15:14	RO 00b	Reserved
13:10	RW 0010b	**Minimum Powerdown Exit to Non-Read command spacing (sd1_cr_txp):** This configuration register indicates the minimum number of clocks to wait following assertion of CKE before issuing a non-read command. 1010–1111 = Reserved. 0010–1001 = 2-9 clocks 0000–0001 = Reserved.
9:1	RW 000000000b	**Self refresh exit count (sd1_cr_slfrfsh_exit_cnt):** This configuration register indicates the Self refresh exit count. (Program to 255). This field corresponds to t_{XSNR}/t_{XSRD} in the DDR Specification.
0	RW 0b	**indicates only 1 DIMM populated (sd1_cr_singledimmpop):** This bit, when set, indicates that only 1 DIMM is populated.

5.2.27 C1REFRCTRL—Channel 1 DRAM Refresh Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 669–66Eh
Default Value: 021830000C30h
Access: RW, RO
Size: 48 bits

This register provides settings to configure the DRAM refresh controller.

Bit	Access & Default	Description
47:42	RO 00h	Reserved
41:37	RW 10000b	**Direct Rcomp Quiet Window (DIRQUIET):** This configuration setting indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.
36:32	RW 11000b	**Indirect Rcomp Quiet Window (INDIRQUIET):** This configuration setting indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.
31:27	RW 00110b	**Rcomp Wait (RCOMPWAIT):** This configuration setting indicates the amount of refresh_tick events to wait before the service of rcomp request in non-default mode of independent rank refresh.
26	RW 0b	**ZQCAL Enable (ZQCALEN):** This bit enables the DRAM controller to issue ZQCAL S command periodically. 0 = Disable 1 = Enable

Bit	Access & Default	Description
25	RW 0b	**Refresh Counter Enable (REFCNTEN):** This bit is used to enable the refresh counter to count during times that DRAM is not in self-refresh, but refreshes are not enabled. Such a condition may occur due to need to reprogram DIMMs following DRAM controller switch. This bit has no effect when Refresh is enabled (i.e., there is no mode where Refresh is enabled but the counter does not run). Thus, in conjunction with bit 23 REFEN, the modes are: **REFEN:REFCNTEN** — **Description** 0:0 — Normal refresh disable 0:1 — Refresh disabled, but counter is accumulating refreshes. 1:X — Normal refresh enable
24	RW 0b	**All Rank Refresh (ALLRKREF):** This configuration bit enables (by default) that all the ranks are refreshed in a staggered/atomic fashion. If set, the ranks are refreshed in an independent fashion.
23	RW 0b	**Refresh Enable (REFEN):** Refresh is enabled. 0 = Disabled 1 = Enabled
22	RW 0b	**DDR Initialization Done (INITDONE):** Indicates that DDR initialization is complete. 0 = Not Done 1 = Done
21:20	RW 00b	**DRAM Refresh Hysterisis (REFHYSTERISIS):** Hysterisis level - Useful for dref_high watermark cases. The dref_high flag is set when the dref_high watermark level is exceeded, and is cleared when the refresh count is less than the hysterisis level. This field should be set to a value less than the high watermark level. 00 = 3 01 = 4 10 = 5 11 = 6
19:18	RW 00b	**DRAM Refresh Panic Watermark (REFPANICWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_panic flag is set. 00 = 5 01 = 6 10 = 7 11 = 8
17:16	RW 00b	**DRAM Refresh High Watermark (REFHIGHWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_high flag is set. 00 = 3 01 = 4 10 = 5 11 = 6

Bit	Access & Default	Description
15:14	RW 00b	**DRAM Refresh Low Watermark (REFLOWWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_low flag is set. 00 = 1 01 = 2 10 = 3 11 = 4
13:0	RW 00110000 110000b	**Refresh Counter Time Out Value (REFTIMEOUT):** Program this field with a value that will provide 7.8 us at the memory clock frequency. At various memory clock frequencies this results in the following values: 266 MHz -> 820 hex 333 MHz -> A28 hex 400 MHz -> C30 hex 533 MHz -> 104B hex 666 MHz -> 1450 hex

5.2.28 C1ODTCTRL—Channel 1 ODT Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: 69C–69Fh
Default Value: 00000000h
Access: RO, RW
Size: 32 bits

This register provides ODT controls.

Bit	Access & Default	Description
31:12	RO 00000h	Reserved
11:8	RW 0h	**DRAM ODT for Read Commands (sd1_cr_odt_duration_rd):** Specifies the duration in MDCLKs to assert DRAM ODT for Read Commands. The Async value should be used when the Dynamic Powerdown bit is set. Else use the Sync value.
7:4	RW 0h	**DRAM ODT for Write Commands (sd1_cr_odt_duration_wr):** Specifies the duration in MDCLKs to assert DRAM ODT for Write Commands. The Async value should be used when the Dynamic Powerdown bit is set. Else use the Sync value.
3:0	RW 0h	**MCH ODT for Read Commands (sd1_cr_mchodt_duration):** Specifies the duration in MDCLKs to assert MCH ODT for Read Commands

5.2.29 EPC0DRB0—ME Channel 0 DRAM Rank Boundary Address 0

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A00–A01h
Default Value: 0000h
Access: R/W, RO
Size: 16 bits

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	R/W 000h	**Channel 0 Dram Rank Boundary Address 0 (C0DRBA0):**

5.2.30 EPC0DRB1—EP Channel 0 DRAM Rank Boundary Address 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A02–A03h
Default Value: 0000h
Access: RO, RW
Size: 16 bits

See C0DRB0 register.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	RW 000h	**Channel 0 Dram Rank Boundary Address 1 (C0DRBA1):**

5.2.31 EPC0DRB2—EP Channel 0 DRAM Rank Boundary Address 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A04–A05h
Default Value: 0000h
Access: RO, RW
Size: 16 bits

See C0DRB0 register.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	RW 000h	**Channel 0 DRAM Rank Boundary Address 2 (C0DRBA2):**

5.2.32 EPC0DRB3—EP Channel 0 DRAM Rank Boundary Address 3

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A06–A07h
Default Value: 0000h
Access: RW, RO
Size: 16 bits

See C0DRB0 register.

Bit	Access & Default	Description
15:10	RO 000000b	Reserved
9:0	RW 000h	**Channel 0 DRAM Rank Boundary Address 3 (C0DRBA3):**

5.2.33 EPC0DRA01—EP Channel 0 DRAM Rank 0,1 Attribute

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A08–A09h
Default Value: 0000h
Access: RW
Size: 16 bits

The DRAM Rank Attribute Registers define the page sizes/number of banks to be used when accessing different ranks. These registers should be left with their default value (all zeros) for any rank that is unpopulated, as determined by the corresponding CxDRB registers. Each byte of information in the CxDRA registers describes the page size of a pair of ranks. Channel and rank map:

Ch0 Rank0, 1: 108h – 109h

Ch0 Rank2, 3: 10Ah – 10Bh

Ch1 Rank0, 1: 188h – 189h

Ch1 Rank2, 3: 18Ah – 18Bh

Bit	Access & Default	Description
15:8	RW 00h	**Channel 0 DRAM Rank-1 Attributes (C0DRA1):** This field defines DRAM pagesize/number-of-banks for rank1 for given channel.
7:0	RW 00h	**Channel 0 DRAM Rank-0 Attributes (C0DRA0):** This field defines DRAM pagesize/number-of-banks for rank0 for given channel.

5.2.34 EPC0DRA23—EP Channel 0 DRAM Rank 2,3 Attribute

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A0A–A0Bh
Default Value: 0000h
Access: RW
Size: 16 bits

See C0DRA01 register.

Bit	Access & Default	Description
15:8	RW 00h	**Channel 0 DRAM Rank-3 Attributes (C0DRA3):** This field defines DRAM pagesize/number-of-banks for rank3 for given channel.
7:0	RW 00h	**Channel 0 DRAM Rank-2 Attributes (C0DRA2):** This field defines DRAM pagesize/number-of-banks for rank2 for given channel.

5.2.35 EPDCYCTRKWRTPRE—EPD CYCTRK WRT PRE

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A19–A1Ah
Default Value: 0000h
Access: RW, RO
Size: 16 bits

This register provides EPD CYCTRK WRT PRE Status.

Bit	Access & Default	Description
15:11	RW 00000b	**ACTTo PRE Delayed (C0sd_cr_act_pchg):** This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and PRE commands to the same rank-bank
10:6	RW 00000b	**Write To PRE Delayed (C0sd_cr_wr_pchg):** This field indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and PRE commands to the same rank-bank
5:2	RW 0000b	**READ To PRE Delayed (C0sd_cr_rd_pchg):** This field indicates the minimum allowed spacing (in DRAM clocks) between the READ and PRE commands to the same rank-bank
1:0	RO 00b	Reserved

5.2.36 EPDCYCTRKWRTACT—EPD CYCTRK WRT ACT

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A1C–A1Fh
Default Value: 00000000h
Access: RO, RW
Size: 32 bits

This register provides EPD CYCTRK WRT ACT Status.

Bit	Access & Default	Description
31:21	RO 000h	Reserved
20:17	RW 0000b	**ACT to ACT Delayed (C0sd_cr_act_act[):** This field indicates the minimum allowed spacing (in DRAM clocks) between two ACT commands to the same rank.
16:13	RW 0000b	**PRE to ACT Delayed (C0sd_cr_pre_act):** This field indicates the minimum allowed spacing (in DRAM clocks) between the PRE and ACT commands to the same rank-bank:12:9R/W0000bPRE-ALL to ACT Delayed (C0sd_cr_preall_act): This field indicates the minimum allowed spacing (in DRAM clocks) between the PRE-ALL and ACT commands to the same rank.
12:9	RO 0h	Reserved
8:0	RW 000000000b	**REF to ACT Delayed (C0sd_cr_rfsh_act):** This field indicates the minimum allowed spacing (in DRAM clocks) between REF and ACT commands to the same rank.

5.2.37 EPDCYCTRKWRTWR—EPD CYCTRK WRT WR

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A20–A21h
Default Value: 0000h
Access: RW, RO
Size: 16 bits

This register provides EPD CYCTRK WRT WR Status.

Bit	Access & Default	Description
15:12	RW 0h	**ACT To Write Delay (C0sd_cr_act_wr):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the ACT and WRITE commands to the same rank-bank.
11:8	RW 0h	**Same Rank Write To Write Delayed (C0sd_cr_wrsr_wr):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between two WRITE commands to the same rank.
7:4	RO 0h	Reserved
3:0	RW 0h	**Same Rank WRITE to READ Delay (C0sd_cr_rd_wr):** This configuration register indicates the minimum allowed spacing (in DRAM clocks) between the WRITE and READ commands to the same rank

5.2.38 EPDCYCTRKWRTRD—EPD CYCTRK WRT READ

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A24–A26h
Default Value: 000000h
Access: RW
Size: 24 bits
BIOS Optimal Default 000h

This register provides EPD CYCTRK WRT RD Status.

Bit	Access & Default	Description
23:23	RO 0h	Reserved
22:20	RW 000b	**EPDunit DQS Slave DLL Enable to Read Safe (EPDSDLL2RD):** This field provides the setting for Read command safe from the point of enabling the slave DLLs.
19:18	RO 0h	Reserved
17:14	RW 0h	**Min ACT To READ Delayed (C0sd_cr_act_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the ACT and READ commands to the same rank-bank.
13:9	RW 00000b	**Same Rank READ to WRITE Delayed (C0sd_cr_wrsr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between the READ and WRITE commands.
8:6	RO 0h	Reserved
5:3	RW 000b	**Same Rank Read To Read Delayed (C0sd_cr_rdsr_rd):** This field indicates the minimum allowed spacing (in DRAM clocks) between two READ commands to the same rank.
2:0	RO 0h	Reserved

5.2.39 EPDCKECONFIGREG—EPD CKE Related Configuration Register

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A28–A2Ch
Default Value: 00E0000000h
Access: RW
Size: 40 bits
BIOS Optimal Default 0h

This register provides CKE related configuration for EPD.

Bit	Access & Default	Description
39:35	RW 00000b	**EPDunit TXPDLL Count (EPDTXPDLL):** This field specifies the delay from precharge power down exit to a command that requires the DRAM DLL to be operational. The commands are read/write.
34:32	RW 000b	**EPDunit TXP count (EPDCKETXP):** This field specifies the timing requirement for Active power down exit or fast exit pre-charge power down exit to any command or slow exit pre-charge power down to Non-DLL (rd/wr/odt) command.
31:29	RW 111b	**Mode Select (sd0_cr_sms):** This field indicates the mode in which the controller is operating in. 111 = Indicates normal mode of operation, else special mode of operation.
28:27	RW 00b	**EPDunit EMRS command select. (EPDEMRSSEL):** EMRS mode to select BANK address. 01 = EMRS 10 = EMRS2 11 = EMRS3
26:24	RW 000b	**CKE pulse width requirement in high phase (sd0_cr_cke_pw_hl_safe):** This field indicates CKE pulse width requirement in high phase.
23:20	RW 0h	**one-hot active rank population (ep_scr_actrank):** This field indicates the active rank in a one hot manner
19:17	RW 000b	**CKE pulse width requirement in low phase (sd0_cr_cke_pw_lh_safe):** This field indicates CKE pulse width requirement in low phase.
16:15	RO 0h	Reserved
14	RW 0b	**EPDunit MPR mode (EPDMPR):** MPR Read Mode 1 = MPR mode 0 = Normal mode In MPR mode, only read cycles must be issued by Firmware. Page Results are ignored by DCS and just issues the read chip select.

Bit	Access & Default	Description
13	RW 0b	**EPDunit Power Down enable for ODT Rank (EPDOAPDEN):** Configuration to enable the ODT ranks to dynamically enter power down. 1 = Enable active power down. 0 = Disable active power down.
12	RW 0b	**EPDunit Power Down enable for Active Rank (EPDAAPDEN):** Configuration to enable the active rank to dynamically enter power down. 1 = Enable active power down. 0 = Disable active power down.
11:10	RO 0h	Reserved
9:1	RW 00000000 0b	**Self refresh exit count (sd0_cr_slfrfsh_exit_cnt):** This field indicates the Self refresh exit count. (Program to 255)
0	RW 0b	**indicates only 1 rank enabled (sd0_cr_singledimmpop):** This field indicates that only 1 rank is enabled. This bit needs to be set if there is one active rank and no odt ranks, or if there is one active rank and one odt rank and they are the same rank.

5.2.40 MEMEMSPACE—ME Memory Space Configuration

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A2Eh
Default Value: 00h
Access: R/W, RO
Size: 8 bits

This register provides settings to enable the ME memory space and define the size of EP memory if enabled.

Bit	Access & Default	Description
7:5	RO 000b	Reserved
4:0	R/W 00000b	**ME-UMA(Sx) Region Size (EXRS):** These bits are written by firmware to indicate the desired size of ME-UMA(Sx) memory region. This is done prior to bring up core power and allowing BIOS to initialize memory. Within channel 0 DDR, the physical base address for MEUMA(Sx) will be determined by: ME-UMA(Sx)BASE = C0DRB3 - EXRS This forces the ME-UMA(Sx) region to always be positioned at the top of the memory populated in channel 0. The approved sizes for ME-UMA(Sx) are values between 0000b (0MB, no ME-UMA(Sx) region) and 10000b (16MB ME-UMA(Sx) region)

5.2.41 EPDREFCONFIG—EP DRAM Refresh Configuration

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: A30–A33h
Default Value: 40000C30h
Access: RO, RW
Size: 32 bits

This register provides settings to configure the EPD refresh controller.

Bit	Access & Default	Description
31	RO 0b	Reserved
30:29	RW 10b	**EPDunit refresh count addition for self refresh exit. (EPDREF4SR):** Configuration indicating the number of additional refreshes that needs to be added to the refresh request count after exiting self refresh. Typical value is to add 2 refreshes. 00 = Add 0 Refreshes 01 = Add 1 Refreshes 10 = Add 2 Refreshes 11 = Add 3 Refreshes Signal name used: ep_scr_refreq_aftersr[1:0]
28	RW 0b	**Refresh Counter Enable (REFCNTEN):** This bit is used to enable the refresh counter to count during times that DRAM is not in self-refresh, but refreshes are not enabled. Such a condition may occur due to need to reprogram DIMMs following DRAM controller switch. This bit has no effect when Refresh is enabled (i.e. there is no mode where Refresh is enabled but the counter does not run). Thus, in conjunction with bit 23 REFEN, the modes are: **REFEN:REFCNTEN — Description** 0:0 — Normal refresh disable 0:1 — Refresh disabled, but counter is accumulating refreshes. 1:X — Normal refresh enable
27	RW 0b	**Refresh Enable (REFEN):** 0 = Disabled 1 = Enabled
26	RW 0b	**DDR Initialization Done (INITDONE):** Indicates that DDR initialization is complete. 0 = Not Done 1 = Done

Bit	Access & Default	Description
25:22	RW 0000b	**DRAM Refresh Hysterisis (REFHYSTERISIS):** Hysterisis level - Useful for dref_high watermark cases. The dref_high flag is set when the dref_high watermark level is exceeded, and is cleared when the refresh count is less than the hysterisis level. This bit should be set to a value less than the high watermark level. 0000 = 0 0001 = 1 ..... 1000 = 8
21:18	RW 0000b	**DRAM Refresh High Watermark (REFHIGHWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_high flag is set. 0000 = 0 0001 = 1 ..... 1000 = 8
17:14	RW 0000b	**DRAM Refresh Low Watermark (REFLOWWM):** When the refresh count exceeds this level, a refresh request is launched to the scheduler and the dref_low flag is set. 0000 = 0 0001 = 1 ..... 1000 = 8
13:0	RW 001100001 10000b	**Refresh Counter Time Out Value (REFTIMEOUT):** Program this field with a value that will provide 7.8 us at the memory clock frequency. At various memory clock frequencies this results in the following values: 266 MHz -> 820 hex 333 MHz -> A28 hex 400 MHz -> C30 hex 533 MHz -> 104B hex 666 MHz -> 1450 hex

5.2.42 TSC1—Thermal Sensor Control 1

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CD8h
Default Value: 00h
Access: RW/L, RW, RS/WC
Size: 8 bits

This register controls the operation of the thermal sensor. Bits 7:1 of this register are reset to their defaults by CL_PWROK. Bit 0 is reset to its default by PLTRST#.

Bit	Access & Default	Description
7	RW/L 0b	**Thermal Sensor Enable (TSE):** This bit enables power to the thermal sensor. Lockable via TCO bit 7. 0 = Disabled 1 = Enabled
6	RW 0b	**Analog Hysteresis Control (AHC):** This bit enables the analog hysteresis control to the thermal sensor. When enabled, about 1 degree of hysteresis is applied. This bit should normally be off in thermometer mode since the thermometer mode of the thermal sensor defeats the usefulness of analog hysteresis. 0 = hysteresis disabled 1= analog hysteresis enabled.
5:2	RW 0000b	**Digital Hysteresis Amount (DHA):** This bit determines whether no offset, 1 LSB, 2... 15 is used for hysteresis for the trip points. 0000 = digital hysteresis disabled, no offset added to trip temperature 0001 = offset is 1 LSB added to each trip temperature when tripped ... 0110 = ~3.0 °C (Recommended setting) ... 1110 = added to each trip temperature when tripped 1111 = added to each trip temperature when tripped
1	RW/L 0b	**Thermal Sensor Comparator Select (TSCS):** This bit multiplexes between the two analog comparator outputs. Normally Catastrophic is used. Lockable via TCO bit 7. 0 = Catastrophic 1 = Hot

Bit	Access & Default	Description
0	RS/WC 0b	**In Use (IU):** Software semaphore bit. After a full MCH RESET, a read to this bit returns a 0. After the first read, subsequent reads will return a 1. A write of a 1 to this bit will reset the next read value to 0. Writing a 0 to this bit has no effect. Software can poll this bit until it reads a 0, and will then own the usage of the thermal sensor. This bit has no other effect on the hardware, and is only used as a semaphore among various independent software threads that may need to use the thermal sensor. Software that reads this register but does not intend to claim exclusive access of the thermal sensor must write a one to this bit if it reads a 0, in order to allow other software threads to claim it. See also THERM3 bit 7 and IUB, which are independent additional semaphore bits.

5.2.43 TSC2—Thermal Sensor Control 2

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CD9h
Default Value: 00h
Access: RW/L, RO
Size: 8 bits

This register controls the operation of the thermal sensor. All bits in this register are reset to their defaults by CL_PWROK.

Bit	Access & Default	Description
7:4	RO 0h	Reserved
3:0	RW/L 0h	**Thermometer Mode Enable and Rate (TE):** If analog thermal sensor mode is not enabled by setting these bits to 0000b, these bits enable the thermometer mode functions and set the Thermometer controller rate. When the Thermometer mode is disabled and TSC1[TSE] =enabled, the analog sensor mode should be fully functional. In the analog sensor mode, the Catastrophic trip is functional, and the Hot trip is functional at the offset below the catastrophic programmed into TSC2[CHO]. The other trip points are not functional in this mode. When Thermometer mode is enabled, all the trip points (Catastrophic, Hot, Aux0) will all operate using the programmed trip points and Thermometer mode rate. **Note:** When disabling the Thermometer mode while thermometer running, the Thermometer mode controller will finish the current cycle.

Bit	Access & Default	Description
		Note: During boot, all other thermometer mode registers (except lock bits) should be programmed appropriately before enabling the Thermometer Mode. Clock used is the memory command clock (i.e., ep_mcclk). **Note:** The same legacy thermal sensor design in prior (G)MCHs has been used in this design. However, the thermal sensor logic runs in a memory command clock domain that is ½ the frequency of the memory clock used in prior designs. Hence the period counted for the thermal sensor settling time has doubled for the same settings, compared to prior (G)MCHs. Thus the thermal sensor programming should be updated to maintain the same thermometer rate count as in prior (G)MCHs. Lockable via TCO bit 7. 0000 = Thermometer mode disabled (i.e., analog sensor mode) 0001 = enabled, 512 clock mode 0010 = enabled, 1024 clock mode (normal Thermometer mode operation, for DDR 667/800) provides ~6.14 us settling time @ 167 MHz ep_mcclk (DDR 667) provides ~5.12 us settling time @ 200 MHz ep_mcclk (DDR 800) provides ~3.84 us settling time @ 267 MHz ep_mcclk (DDR 1066) 0011 = enabled, 1536 clock mode (normal Thermometer mode operation, for DDR 1066) provides ~9.22 us settling time @ 167 MHz ep_mcclk (DDR 667) provides ~7.68 us settling time @ 200 MHz ep_mcclk (DDR 800) provides ~5.76 us settling time @ 267 MHz ep_mcclk (DDR 1066) provides ~4.61 us settling time @ 333 MHz ep_mcclk (DDR 1333) 0100 = enabled, 2048 clock mode (normal Thermometer mode operation, for DDR 1333) provides ~15.36 us settling time @ 133 MHz ep_mcclk (DDR 533) provides ~12.29 us settling time @ 167 MHz ep_mcclk (DDR 667) provides ~10.24 us settling time @ 200 MHz ep_mcclk (DDR 800) provides ~7.68 us settling time @ 267 MHz ep_mcclk (DDR 1066) 0101 = enabled, 3072 clock mode 0110 = enabled, 4096 clock mode 0111 = enabled, 6144 clock mode all other permutations are reserved 1111 = enabled, 4 clock mode (for testing digital logic) **NOTE:** The settling time for DAC and Thermal Diode is between 2 and 5 us. To meet this requirement the SE value must be programmed to be 5 us or more. Recommendation is to use: “0010” setting for DDR 667/800 and “0011” setting for DDR 1066.

5.2.44 TSS—Thermal Sensor Status

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CDAh
Default Value: 00h
Access: RO
Size: 8 bits

This read only register provides trip point and other status of the thermal sensor. All bits in this register are reset to their defaults by CL_PWROK.

Bit	Access & Default	Description
7	RO 0b	**Catastrophic Trip Indicator (CTI):** 1 = Internal thermal sensor temperature is above the catastrophic setting.
6	RO 0b	**Hot Trip Indicator (HTI):** 1 = Internal thermal sensor temperature is above the Hot setting.
5	RO 0b	**Aux0 Trip Indicator (A0TI):** 1 = Internal thermal sensor temperature is above the Aux0 setting.
4	RO 0b	**Thermometer Mode Output Valid (TOV):** 1 = Thermometer mode is able to converge to a temperature and that the TR register is reporting a reasonable estimate of the thermal sensor temperature. 0 = Thermometer mode is off, or that temperature is out of range, or that the TR register is being looked at before a temperature conversion has had time to complete.
3:2	RO 00b	Reserved
1	RO 0b	**Direct Catastrophic Comparator Read (DCCR):** This bit reads the output of the Catastrophic comparator directly, without latching via the Thermometer mode circuit. Used for testing.
0	RO 0b	**Direct Hot Comparator Read (DHCR):** This bit reads the output of the Hot comparator directly, without latching via the Thermometer mode circuit. Used for testing.

5.2.45 TSTTP—Thermal Sensor Temperature Trip Point

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CDC–CDFh
Default Value: 00000000h
Access: RO, RW, RW/L
Size: 32 bits

This register :

- Sets the target values for the trip points in thermometer mode. See also TST[Direct DAC Connect Test Enable].
- Reports the relative thermal sensor temperature

All bits in this register are reset to their defaults by CL_PWROK.

Bit	Access & Default	Description
31:24	RO 00h	**Relative Temperature (RELT):** In Thermometer mode, the RELT field of this register report the relative temperature of the thermal sensor. Provides a two's complement value of the thermal sensor relative to the Hot Trip Point. Temperature above the Hot Trip Point will be positive. TR and HTPS can both vary between 0 and 255. But RELT will be clipped between ±127 to keep it an 8 bit number. See also TSS[Thermometer mode Output Valid] In the Analog mode, the RELT field reports HTPS value.
23:16	RW 00h	**Aux0 Trip point setting (A0TPS):** Sets the target for the Aux0 trip point.
15:8	RW/L 00h	**Hot Trip Point Setting (HTPS):** Sets the target value for the Hot trip point. Lockable via TCO bit 7.
7:0	RW/L 00h	**Catastrophic Trip Point Setting (CTPS):** Sets the target for the Catastrophic trip point. See also TST[Direct DAC Connect Test Enable]. Lockable via TCO bit 7.

5.2.46 TCO—Thermal Calibration Offset

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CE2h
Default Value: 00h
Access: RW/L/K, RW/L
Size: 8 bits

Bit 7: reset to its default by PLTRST#. Bits 6:0 reset to their defaults by CL_PWROK.

Bit	Access & Default	Description
7	RW/L/K 0b	**Lock Bit for Catastrophic (LBC):** This bit, when written to a 1, locks the Catastrophic programming interface, including bits 7:0 of this register and bits 15:0 of TSTTP, bits 1,7 of TSC 1, bits 3:0 of TSC 2, bits 4:0 of TSC 3, and bits 0,7 of TST. This bit may only be set to a 0 by a hardware reset (PLTRST#). Writing a 0 to this bit has no effect.
6:0	RW/L 00h	**Calibration Offset (CO):** This field contains the current calibration offset for the Thermal Sensor DAC inputs. The calibration offset is a twos complement signed number which is added to the temperature counter value to help generate the final value going to the thermal sensor DAC. This field is Read/Write and can be modified by Software unless locked by setting bit 7 of this register. The fuses cannot be programmed via this register. Once this register has been overwritten by software, the values of the TCO fuses can be read using the Therm3 register. Note for TCO operation: While this is a seven-bit field, the 7th bit is sign extended to 9 bits for TCO operation. The range of 00h to 3Fh corresponds to 0 0000 0000 to 0 0011 1111. The range of 41h to 7Fh corresponds to 1 1100 001 (i.e., negative 3Fh) to 1 1111 1111 (i.e., negative 1), respectively.

5.2.47 THERM1—Hardware Throttle Control

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CE4h
Default Value: 00h
Access: RW/L, RO, RW/L/K
Size: 8 bits

All bits in this register are reset to their defaults by PLTRST#.

Bit	Access & Default	Description
7	RW/L 00h	**Internal Thermal Hardware Throttling Enable (ITHTE):** This bit is a master enable for internal thermal sensor-based hardware throttling. 0 = Disable. Hardware actions via the internal thermal sensor are disabled. 1 = Enable. Hardware actions via the internal thermal sensor are enabled.
6	RW/L 00h	**Internal Thermal Hardware Throttling Type (ITHTT):** This policy bit determines what type of hardware throttling will be enacted by the internal thermal sensor when enabled by ITHTE. 0 = (G)MCH throttling 1 = DRAM throttling
5	RO 00h	Reserved
4	RW/L 00h	**Throttling Temperature Range Selection (TTRS):** This bit determines what temperature ranges will enable throttling. Lockable by bit 0 of this register. See also the throttling registers in MCHBAR configuration space C0GTC and C1GTC [(G)MCH Thermal Sensor Trip Enable] and PEFC [Thermal Sensor Trip Enable] which are used to enable or disable throttling. 0 = Catastrophic only. The Catastrophic thermal temperature range will enable main memory thermal throttling. 1 = Hot and Catastrophic.
3	RW/L 00h	**Halt on Catastrophic (HOC):** 0 = Continue to toggle clocks when the catastrophic sensor trips. 1 = All clocks are disabled when the catastrophic sensor trips. A system reset is required to bring the system out of a halt from the thermal sensor.
2:1	RO 00b	Reserved
0	RW/L/K 00h	**Hardware Throttling Lock Bit (HTL):** This bit locks bits 7:0 of this register. 0 = The register bits are unlocked. 1 = The register bits are locked. It may only be set to a 0 by a hardware reset. Writing a 0 to this bit has no effect.

5.2.48 TIS—Thermal Interrupt Status

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CEA–CEBh
Default Value: 0000h
Access: RO, RWC
Size: 16 bits

This register is used to report which specific error condition resulted in the dev. 0 fn. 0 ERRSTS[Thermal Sensor event for SMI/SCI/SERR] or memory mapped IIR Thermal Event. Software can examine the current state of the thermal zones by examining the TSS. Software can distinguish internal or external Trip Event by examining EXTTSCS.

Software must write a 1 to clear the status bits in this register.

Following scenario is possible. An interrupt is initiated on a rising temperature trip, the appropriate DMI cycles are generated, and eventually the software services the interrupt and sees a rising temperature trip as the cause in the status bits for the interrupts. Assume that the software then goes and clears the local interrupt status bit in the TIS register for that trip event. It is possible at this point that a falling temperature trip event occurs before the software has had the time to clear the global interrupts status bit. But since software has already looked at the status register before this event happened, software may not clear the local status flag for this event. Therefore, after the global interrupt is cleared by software, software must look at the instantaneous status in the TSS register.

All bits in this register are reset to their defaults by PLTRST#.

Bit	Access & Default	Description
15:10	RO 00h	Reserved
9	RWC 0b	**Was Catastrophic Thermal Sensor Interrupt Event (WCTSIE):** 1 = Indicates that a Catastrophic Thermal Sensor trip based on a higher to lower temperature transition thru the trip point 0 = No trip for this event
8	RWC 0b	**Was Hot Thermal Sensor Interrupt Event (WHTSIE):** 1 = Indicates that a Hot Thermal Sensor trip based on a higher to lower temperature transition thru the trip point 0 = No trip for this event
7	RWC 0b	**Was Aux0 Thermal Sensor Interrupt Event (WA0TSIE):** 1 = Indicates that an Aux0 Thermal Sensor trip based on a higher to lower temperature transition thru the trip point 0 = No trip for this event Software must write a 1 to clear this status bit.
6:5	RO 00b	Reserved

Bit	Access & Default	Description
4	RWC 0b	**Catastrophic Thermal Sensor Interrupt Event (CTSIE):** 1 = Indicates that a Catastrophic Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point. 0 = No trip for this event Software must write a 1 to clear this status bit.
3	RWC 0b	**Hot Thermal Sensor Interrupt Event (HTSIE):** 1 = Indicates that a Hot Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point. 0 = No trip for this event Software must write a 1 to clear this status bit.
2	RWC 0b	**Aux0 Thermal Sensor Interrupt Event (A0TSIE):** 1 = Indicates that an Aux0 Thermal Sensor trip event occurred based on a lower to higher temperature transition thru the trip point. 0 = No trip for this event Software must write a 1 to clear this status bit.
1:0	RO 00b	Reserved

5.2.49 TSMICMD—Thermal SMI Command

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: CF1h
Default Value: 00h
Access: RO, RW
Size: 8 bits

This register selects specific errors to generate a SMI DMI special cycle, as enabled by the Device 0 SMI Error Command Register [SMI on (G)MCH Thermal Sensor Trip]. The SMI must not be enabled at the same time as the SERR/SCI for the thermal sensor event.

All bits in this register are reset to their defaults by PLTRST#.

Bit	Access & Default	Description
7:3	RO 00h	Reserved
2	RW 0b	**SMI on (G)MCH Catastrophic Thermal Sensor Trip (SMGCTST):** 1 = Does not mask the generation of an SMI DMI special cycle on a catastrophic thermal sensor trip. 0 = Disable reporting of this condition via SMI messaging.
1	RW 0b	**SMI on (G)MCH Hot Thermal Sensor Trip (SMGHTST):** 1 = Does not mask the generation of an SMI DMI special cycle on a Hot thermal sensor trip. 0 = Disable reporting of this condition via SMI messaging.
0	RW 0b	**SMI on (G)MCH Aux Thermal Sensor Trip (SMGATST):** 1 = Does not mask the generation of an SMI DMI special cycle on an Auxiliary thermal sensor trip. 0 = Disable reporting of this condition via SMI messaging.

5.2.50 PMSTS—Power Management Status

B/D/F/Type: 0/0/0/MCHBAR
Address Offset: F14–F17h
Default Value: 00000000h
Access: RWC/S, RO
Size: 32 bits

This register is Reset by PWROK only.

Bit	Access & Default	Description
31:9	RO 000000h	Reserved
8	RWC/S 0b	**Warm Reset Occurred (WRO):** Set by the PMunit whenever a Warm Reset is received, and cleared by PWROK=0. 0 = No Warm Reset occurred. 1 = Warm Reset occurred. BIOS Requirement: BIOS can check and clear this bit whenever executing POST code. This way BIOS knows that if the bit is set, then the PMSTS bits [1:0] must also be set, and if not BIOS needs to power-cycle the platform.
7:2	RO 00h	Reserved
1	RWC/S 0b	**Channel 1 in Self-Refresh (C1SR):** Set by power management hardware after Channel 1 is placed in self refresh as a result of a Power State or a Reset Warn sequence. Cleared by Power management hardware before starting Channel 1 self refresh exit sequence initiated by a power management exit. Cleared by the BIOS by writing a 1 in a warm reset (Reset# asserted while PWROK is asserted) exit sequence. 0 = Channel 1 not ensured to be in self refresh. 1 = Channel 1 in Self Refresh.
0	RWC/S 0b	**Channel 0 in Self-Refresh (C0SR):** Set by power management hardware after Channel 0 is placed in self refresh as a result of a Power State or a Reset Warn sequence. Cleared by Power management hardware before starting Channel 0 self refresh exit sequence initiated by a power management exit. Cleared by the BIOS by writing a 1 in a warm reset (Reset# asserted while PWROK is asserted) exit sequence. 0 = Channel 0 not ensured to be in self refresh. 1 = Channel 0 in Self Refresh.

5.3 EPBAR

Table 5-4. EPBAR Register Address Map

Address Offset	Symbol	Register Name	Default Value	Access
44–47h	EPESD	EP Element Self Description	00000201h	RO, RWO
50–53h	EPLE1D	EP Link Entry 1 Description	01000000h	RO, RWO
58–5Fh	EPLE1A	EP Link Entry 1 Address	0000000000000000h	RO, RWO
60–63h	EPLE2D	EP Link Entry 2 Description	02000002h	RO, RWO
68–6Fh	EPLE2A	EP Link Entry 2 Address	0000000000008000h	RO

5.3.1 EPESD—EP Element Self Description

B/D/F/Type: 0/0/0/PXPEPBAR
Address Offset: 44–47h
Default Value: 00000201h
Access: RO, RWO
Size: 32 bits

This register provides information about the root complex element containing this Link Declaration Capability.

Bit	Access & Default	Description
31:24	RO 00h	**Port Number (PN):** This field specifies the port number associated with this element with respect to the component that contains this element. A value of 00h indicates to configuration software that this is the default Express port.
23:16	RWO 00h	**Component ID (CID):** This field indicates identifies the physical component that contains this Root Complex Element. **BIOS Requirement:** Must be initialized according to guidelines in the *PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS).*
15:8	RO 0sh	**Number of Link Entries (NLE):** This field indicates the number of link entries following the Element Self Description. This field reports 2 (one each for PEG and DMI).
7:4	RO 0h	Reserved
3:0	RO 1h	**Element Type (ET):** This field indicates the type of the Root Complex Element. Value of 1 h represents a port to system memory.

5.3.2 EPLE1D—EP Link Entry 1 Description

B/D/F/Type: 0/0/0/PXPEPBAR
Address Offset: 50–53h
Default Value: 01000000h
Access: RO, RWO
Size: 32 bits

This register provides the first part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
31:24	RO 01h	**Target Port Number (TPN):** Specifies the port number associated with the element targeted by this link entry (DMI). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	RWO 00h	**Target Component ID (TCID):** This field indicates the physical or logical component that is targeted by this link entry. **BIOS Requirement:** Must be initialized according to guidelines in the *PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS).*
15:2	RO 0000h	Reserved
1	RO 0b	**Link Type (LTYP):** This field indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	RWO 0b	**Link Valid (LV):** 0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.

5.3.3 EPLE1A—EP Link Entry 1 Address

B/D/F/Type: 0/0/0/PXPEPBAR
Address Offset: 58–5Fh
Default Value: 0000000000000000h
Access: RO, RWO
Size: 64 bits

This register provides the second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
63:36	RO 0s	Reserved
35:12	RWO 0s	**Link Address (LA):** This field contains the memory mapped base address of the RCRB that is the target element (DMI) for this link entry.
11:0	RO 0s	Reserved

5.3.4 EPLE2D—EP Link Entry 2 Description

B/D/F/Type: 0/0/0/PXPEPBAR
Address Offset: 60–63h
Default Value: 02000002h
Access: RO, RWO
Size: 32 bits

This register provides the first part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
31:24	RO 02h	**Target Port Number (TPN):** This field specifies the port number associated with the element targeted by this link entry (PEG). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	RWO 00h	**Target Component ID (TCID):** This field indicates the physical or logical component that is targeted by this link entry. A value of 0 is reserved. Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. **BIOS Requirement:** Must be initialized according to guidelines in the *PCI Express* Isochronous/Virtual Channel Support Hardware Programming Specification (HPS).*
15:2	RO 0s	Reserved
1	RO 1b	**Link Type (LTYP):** This field indicates that the link points to configuration space of the integrated device which controls the x16 root port. The link address specifies the configuration address (segment, bus, device, function) of the target root port.
0	RWO 0b	**Link Valid (LV):** 0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.

5.3.5 EPLE2A—EP Link Entry 2 Address

B/D/F/Type: 0/0/0/PXPEPBAR
Address Offset: 68–6Fh
Default Value: 0000000000008000h
Access: RO
Size: 64 bits

This register provides the second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
63:28	RO 0s	**Reserved for Configuration Space Base Address ():** Not required if root complex has only one configuration space.
27:20	RO 0s	**Bus Number (BUSN):**
19:15	RO 00001b	**Device Number (DEVN):** Target for this link is PCI Express x16 port (Device 1).
14:12	RO 000b	**Function Number (FUNN):**
11:0	RO 0s	Reserved

§

6 PCI Express* Registers (D1:F0)

Device 1 (D1), Funciton 0 (F0) contains the controls associated with the PCI Express x16 root port that is the intended to attach as the point for external graphics. It also functions as the virtual PCI-to-PCI bridge.

Warning: When reading the PCI Express "conceptual" registers such as this, you may not get a valid value unless the register value is stable.

The *PCI Express* Specification* defines two types of reserved bits.

Reserved and Preserved:

1. Reserved for future RW implementations; software must preserve value read for writes to bits.

2. Reserved and Zero: Reserved for future R/WC/S implementations; software must use 0 for writes to bits.

Unless explicitly documented as Reserved and Zero, all bits marked as reserved are part of the Reserved and Preserved type, which have historically been the typical definition for Reserved.

Note: Most (if not all) control bits in this device cannot be modified unless the link is down. Software is required to first Disable the link, then program the registers, and then re-enable the link (which will cause a full-retrain with the new settings).

Table 6-1. PCI Express* Register Address Map (D1:F0)

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID1	Vendor Identification	8086h	RO
02–03h	DID1	Device Identification	29C1h	RO
04–05h	PCICMD1	PCI Command	0000h	RO, RW
06–07h	PCISTS1	PCI Status	0010h	RO, RWC
08h	RID1	Revision Identification	00h	RO
09–0Bh	CC1	Class Code	060400h	RO
0Ch	CL1	Cache Line Size	00h	RW
0Eh	HDR1	Header Type	01h	RO
18h	PBUSN1	Primary Bus Number	00h	RO
19h	SBUSN1	Secondary Bus Number	00h	RW
1Ah	SUBUSN1	Subordinate Bus Number	00h	RW
1Ch	IOBASE1	I/O Base Address	F0h	RW, RO

Address Offset	Register Symbol	Register Name	Default Value	Access
1D	IOLIMIT1	I/O Limit Address	00h	RW, RO
1E–1Fh	SSTS1	Secondary Status	0000h	RWC, RO
20–21h	MBASE1	Memory Base Address	FFF0h	RW, RO
22–23h	MLIMIT1	Memory Limit Address	0000h	RW, RO
24–25h	PMBASE1	Prefetchable Memory Base Address	FFF1h	RW, RO
26–27h	PMLIMIT1	Prefetchable Memory Limit Address	0001h	RW, RO
28–2Bh	PMBASEU1	Prefetchable Memory Base Address	00000000h	RW,
2C–2Fh	PMLIMITU1	Prefetchable Memory Limit Address	00000000h	RW
34h	CAPPTR1	Capabilities Pointer	88h	RO
3Ch	INTRLINE1	Interrupt Line	00h	RW
3Dh	INTRPIN1	Interrupt Pin	01h	RO
3E–3Fh	BCTRL1	Bridge Control	0000h	RO, RW
80–83h	PM_CAPID1	Power Management Capabilities	C8039001h	RO
84–87h	PM_CS1	Power Management Control/Status	00000000h	RO, RW/S, RW
88–8Bh	SS_CAPID	Subsystem ID and Vendor ID Capabilities	0000800Dh	RO
8C–8Fh	SS	Subsystem ID and Subsystem Vendor ID	00008086h	RWO
90–91h	MSI_CAPID	Message Signaled Interrupts Capability ID	A005h	RO
92–93h	MC	Message Control	0000h	RW, RO
94–97h	MA	Message Address	00000000h	RW, RO
98–99h	MD	Message Data	0000h	RW
A0–A1h	PEG_CAPL	PCI Express-G Capability List	0010h	RO
A2–A3h	PEG_CAP	PCI Express-G Capabilities	0141h	RO, RWO
A4–A7h	DCAP	Device Capabilities	00008000h	RO
A8–A9h	DCTL	Device Control	0000h	RO, RW
AA–ABh	DSTS	Device Status	0000h	RO, RWC
AC–AFh	LCAP	Link Capabilities	02014D01h	RO, RWO
B0–B1h	LCTL	Link Control	0000h	RO, RW, RW/SC
B2–B3h	LSTS	Link Status	1001h	RO
B4–B7h	SLOTCAP	Slot Capabilities	00040000h	RWO, RO
B8–B9h	SLOTCTL	Slot Control	01C0h	RO, RW

Address Offset	Register Symbol	Register Name	Default Value	Access
BA–BBh	SLOTSTS	Slot Status	0000h	RO, RWC
BC–BDh	RCTL	Root Control	0000h	RO, RW
C0– C3h	RSTS	Root Status	00000000h	RO, RWC
EC– EFh	PEGLC	PCI Express-G Legacy Control	00000000h	RW, RO
100–103h	VCECH	Virtual Channel Enhanced Capability Header	14010002h	RO
104–107h	PVCCAP1	Port VC Capability Register 1	00000000h	RO
108–10Bh	PVCCAP2	Port VC Capability Register 2	00000000h	RO
10C–10Dh	PVCCTL	Port VC Control	0000h	RO, RW
110–113h	VC0RCAP	VC0 Resource Capability	00000000h	RO
114–117h	VC0RCTL	VC0 Resource Control	800000FFh	RO, RW
11A–11Bh	VC0RSTS	VC0 Resource Status	0002h	RO
140–143h	RCLDECH	Root Complex Link Declaration Enhanced	00010005h	RO
144–147h	ESD	Element Self Description	02000100h	RO, RWO
150–153h	LE1D	Link Entry 1 Description	00000000h	RO, RWO
158–15Fh	LE1A	Link Entry 1 Address	0000000000000000h	RO, RWO
218–21Fh	PEGSSTS	PCI Express-G Sequence Status	0000000000000FFFh	RO

6.1 PCI Express* Configuration Register Details (D1:F0)

6.1.1 VID1—Vendor Identification

B/D/F/Type: 0/1/0/PCI
Address Offset: 00–01h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identify any PCI device.

Bit	Access & Default	Description
15:0	RO 8086h	**Vendor Identification (VID1):** PCI standard identification for Intel.

6.1.2 DID1—Device Identification

B/D/F/Type: 0/1/0/PCI
Address Offset: 02–03h
Default Value: 29C1h
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:8	RO 29h	**Device Identification Number (DID1(UB)):** Identifier assigned to the (G)MCH device 1 (virtual PCI-to-PCI bridge, PCI Express Graphics port).
7:4	RO 7h	**Device Identification Number (DID1(HW)):** Identifier assigned to the (G)MCH device 1 (virtual PCI-to-PCI bridge, PCI Express Graphics port)
3:0	RO 1h	**Device Identification Number (DID1(LB)):** Identifier assigned to the (G)MCH device 1 (virtual PCI-to-PCI bridge, PCI Express Graphics port).

6.1.3 PCICMD1—PCI Command

B/D/F/Type: 0/1/0/PCI
Address Offset: 04–05h
Default Value: 0000h
Access: RO, RW
Size: 16 bits

Bit	Access & Default	Description
15:11	RO 00h	Reserved
10	RW 0b	**INTA Assertion Disable (INTAAD):** This bit 0nly affects interrupts generated by the device (PCI INTA from a PME or Hot Plug event) controlled by this command register. It does not affect upstream MSIs, upstream PCI INTA–INTD assert and de-assert messages. 0 = This device is permitted to generate INTA interrupt messages. 1 = This device is prevented from generating interrupt messages. Any INTA emulation interrupts already asserted must be de-asserted when this bit is set.
9	RO 0b	**Fast Back-to-Back Enable (FB2B):** Not Applicable or Implemented. Hardwired to 0.
8	RW 0b	**SERR# Message Enable (SERRE1):** Controls Device 1 SERR# messaging. The (G)MCH communicates the SERR# condition by sending an SERR message to the ICH. This bit, when set, enables reporting of non-fatal and fatal errors detected by the device to the Root Complex. Note that errors are reported if enabled either through this bit or through the PCI Express specific bits in the Device Control Register. 0 = The SERR message is generated by the (G)MCH for Device #1 only under conditions enabled individually through the Device Control Register. 1 = The (G)MCH is enabled to generate SERR messages which will be sent to the ICH for specific Device #1 error conditions generated/detected on the primary side of the virtual PCI to PCI bridge (not those received by the secondary side). The status of SERRs generated is reported in the PCISTS1 register.
7	RO 0b	Reserved**:** Not Applicable or Implemented. Hardwired to 0.
6	RW 0b	**Parity Error Response Enable (PERRE):** This bit controls whether or not the Master Data Parity Error bit in the PCI Status register can bet set. 0 = Master Data Parity Error bit in PCI Status register can NOT be set. 1 = Master Data Parity Error bit in PCI Status register CAN be set.
5	RO 0b	**VGA Palette Snoop (VGAPS):** Not Applicable or Implemented. Hardwired to 0.

Bit	Access & Default	Description
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Not Applicable or Implemented. Hardwired to 0.
3	RO 0b	**Special Cycle Enable (SCE):** Not Applicable or Implemented. Hardwired to 0.
2	RW 0b	**Bus Master Enable (BME):** This bit controls the ability of the PEG port to forward Memory and IO Read/Write Requests in the upstream direction. This bit does not affect forwarding of Completions from the primary interface to the secondary interface. 0 = This device is prevented from making memory or IO requests to its primary bus. Note that according to PCI Specification, as MSI interrupt messages are in-band memory writes, disabling the bus master enable bit prevents this device from generating MSI interrupt messages or passing them from its secondary bus to its primary bus. Upstream memory writes/reads, IO writes/reads, peer writes/reads, and MSIs will all be treated as invalid cycles. Writes are forwarded to memory address **000C_0000h** with byte enables de-asserted. Reads will be forwarded to memory address **000C_0000h** and will return Unsupported Request status (or Master abort) in its completion packet. 1 = This device is allowed to issue requests to its primary bus. Completions for previously issued memory read requests on the primary bus will be issued when the data is available.
1	RW 0b	**Memory Access Enable (MAE):** 0 = All of device 1's memory space is disabled. 1 = Enable the Memory and Pre-fetchable memory address ranges defined in the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers.
0	RW 0b	**IO Access Enable (IOAE):** 0 = All of device 1's I/O space is disabled. 1 = Enable the I/O address range defined in the IOBASE1, and IOLIMIT1 registers.

6.1.4 PCISTS1—PCI Status

B/D/F/Type: 0/1/0/PCI
Address Offset: 06–07h
Default Value: 0010h
Access: RO, RWC
Size: 16 bits

This register reports the occurrence of error conditions associated with primary side of the "virtual" Host-PCI Express bridge embedded within the (G)MCH.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Not Applicable or Implemented. Hardwired to 0. Parity (generating poisoned TLPs) is not supported on the primary side of this device (we don't do error forwarding).
14	RWC 0b	**Signaled System Error (SSE):** This bit is set when this Device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition and the SERR Enable bit in the Command register is 1. Both received (if enabled by BCTRL1[1]) and internally detected error messages affect this field.
13	RO 0b	**Received Master Abort Status (RMAS):** Not Applicable or Implemented. Hardwired to 0. The concept of a master abort does not exist on primary side of this device.
12	RO 0b	**Received Target Abort Status (RTAS):** Not Applicable or Implemented. Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
11	RO 0b	**Signaled Target Abort Status (STAS):** Not Applicable or Implemented. Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
10:9	RO	**DEVSELB Timing (DEVT):** This device is not the subtractively decoded device on bus 0. This bit field is therefore hardwired to 00 to indicate that the device uses the fastest possible decode.
8	RO 0b	**Master Data Parity Error (PMDPE):** Because the primary side of the PEG's virtual PCI-to-PCI bridge is integrated with the (G)MCH functionality there is no scenario where this bit will get set. Because hardware will never set this bit, it is impossible for software to have an opportunity to clear this bit or otherwise test that it is implemented. The PCI specification defines it as a RWC, but for this implementation an RO definition behaves the same way and will meet all Microsoft testing requirements. This bit can only be set when the Parity Error Enable bit in the PCI Command register is set.
7	RO 0b	**Fast Back-to-Back (FB2B):** Not Applicable or Implemented. Hardwired to 0.
6	RO 0b	Reserved
5	RO 0b	**66/60MHz capability (CAP66):** Not Applicable or Implemented. Hardwired to 0.

Bit	Access & Default	Description
4	RO 1b	**Capabilities List (CAPL):** Indicates that a capabilities list is present. Hardwired to 1.
3	RO 0b	**INTA Status (INTAS):** Indicates that an interrupt message is pending internally to the device. Only PME and Hot Plug sources feed into this status bit (not PCI INTA-INTD assert and de-assert messages). The INTA Assertion Disable bit, PCICMD1[10], has no effect on this bit.
2:0	RO 000b	Reserved

6.1.5 RID1—Revision Identification

B/D/F/Type: 0/1/0/PCI
Address Offset: 08h
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the revision number of the (G)MCH device 1. These bits are read only and writes to this register have no effect.

Bit	Access & Default	Description
7:0	RO 00h	**Revision Identification Number (RID1):** This is an 8-bit value that indicates the revision identification number for the (G)MCH Device 0. Refer to the *Intel® 3 Series Express Chipset Family Specification Update* for the value of the Revision ID register.

6.1.6 CC1—Class Code

B/D/F/Type: 0/1/0/PCI
Address Offset: 09–0Bh
Default Value: 060400h
Access: RO
Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register- specific programming interface.

Bit	Access & Default	Description
23:16	RO 06h	**Base Class Code (BCC):** This field indicates the base class code for this device. This code has the value 06h, indicating a Bridge device.
15:8	RO 04h	**Sub-Class Code (SUBCC):** This field indicates the sub-class code for this device. The code is 04h indicating a PCI to PCI Bridge.
7:0	RO 00h	**Programming Interface (PI):** This field indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

6.1.7 CL1—Cache Line Size

B/D/F/Type: 0/1/0/PCI
Address Offset: 0Ch
Default Value: 00h
Access: RW
Size: 8 bits

Bit	Access & Default	Description
7:0	RW 00h	**Cache Line Size (Scratch pad):** Implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no impact on any PCI Express device functionality.

6.1.8 HDR1—Header Type

B/D/F/Type: 0/1/0/PCI
Address Offset: 0Eh
Default Value: 01h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Access & Default	Description
7:0	RO 01h	**Header Type Register (HDR):** Returns 01 to indicate that this is a single function device with bridge header layout.

6.1.9 PBUSN1—Primary Bus Number

B/D/F/Type: 0/1/0/PCI
Address Offset: 18h
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies that this "virtual" Host-PCI Express bridge is connected to PCI bus #0.

Bit	Access & Default	Description
7:0	RO 00h	**Primary Bus Number (BUSN):** Configuration software typically programs this field with the number of the bus on the primary side of the bridge. Since device 1 is an internal device and its primary bus is always 0, these bits are read only and are hardwired to 0.

6.1.10 SBUSN1—Secondary Bus Number

B/D/F/Type: 0/1/0/PCI
Address Offset: 19h
Default Value: 00h
Access: RW
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the "virtual" bridge (i.e., to PCI Express-G). This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express-G.

Bit	Access & Default	Description
7:0	RW 00h	**Secondary Bus Number (BUSN):** This field is programmed by configuration software with the bus number assigned to PCI Express.

6.1.11 SUBUSN1—Subordinate Bus Number

B/D/F/Type: 0/1/0/PCI
Address Offset: 1Ah
Default Value: 00h
Access: RW
Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below PCI Express-G. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express-G.

Bit	Access & Default	Description
7:0	RW 00h	**Subordinate Bus Number (BUSN):** This register is programmed by configuration software with the number of the highest subordinate bus that lies behind the device #1 bridge. When only a single PCI device resides on the PCI Express segment, this register will contain the same value as the SBUSN1 register.

6.1.12 IOBASE1—I/O Base Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 1Ch
Default Value: F0h
Access: RW, RO
Size: 8 bits

This register controls the processor to PCI Express-G I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT

Only the upper 4 bits are programmable. For the purpose of address decode, address bits A[11:0] are treated as 0. Thus the bottom of the defined I/O address range will be aligned to a 4 KB boundary.

Bit	Access & Default	Description
7:4	RW Fh	**I/O Address Base (IOBASE):** This field corresponds to A[15:12] of the I/O addresses passed by bridge 1 to PCI Express.
3:0	RO 0h	Reserved

6.1.13 IOLIMIT1—I/O Limit Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 1Dh
Default Value: 00h
Access: RW, RO
Size: 8 bits

This register controls the processor to PCI Express-G I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT

Only the upper 4 bits are programmable. For the purpose of address decode, address bits A[11:0] are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4 KB aligned address block.

Bit	Access & Default	Description
7:4	RW 0h	**I/O Address Limit (IOLIMIT):** This field corresponds to A[15:12] of the I/O address limit of device 1. Devices between this upper limit and IOBASE1 will be passed to the PCI Express hierarchy associated with this device.
3:0	RO 0h	Reserved

6.1.14 SSTS1—Secondary Status

B/D/F/Type: 0/1/0/PCI
Address Offset: 1E–1Fh
Default Value: 0000h
Access: RWC, RO
Size: 16 bits

SSTS1 is a 16-bit status register that reports the occurrence of error conditions associated with secondary side (i.e., PCI Express side) of the "virtual" PCI-PCI bridge embedded within (G)MCH.

Bit	Access & Default	Description
15	RWC 0b	**Detected Parity Error (DPE):** This bit is set by the Secondary Side for a Type 1 Configuration Space header device whenever it receives a Poisoned TLP, regardless of the state of the Parity Error Response Enable bit in the Bridge Control Register.
14	RWC 0b	**Received System Error (RSE):** This bit is set when the Secondary Side for a Type 1 configuration space header device receives an ERR_FATAL or ERR_NONFATAL.
13	RWC 0b	**Received Master Abort (RMA):** This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with Unsupported Request Completion Status.
12	RWC 0b	**Received Target Abort (RTA):** This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with Completer Abort Completion Status.
11	RO 0b	**Signaled Target Abort (STA):** Not Applicable or Implemented. Hardwired to 0. The (G)MCH does not generate Target Aborts (the (G)MCH will never complete a request using the Completer Abort Completion status).
10:9	RO 00b	**DEVSELB Timing (DEVT):** Not Applicable or Implemented. Hardwired to 0.
8	RWC 0b	**Master Data Parity Error (SMDPE):** When set, this bit indicates that the (G)MCH received across the link (upstream) a Read Data Completion Poisoned TLP (EP=1). This bit can only be set when the Parity Error Enable bit in the Bridge Control register is set.
7	RO 0b	**Fast Back-to-Back (FB2B):** Not Applicable or Implemented. Hardwired to 0.
6	RO 0b	Reserved
5	RO 0b	**66/60 MHz capability (CAP66):** Not Applicable or Implemented. Hardwired to 0.
4:0	RO 00h	Reserved

6.1.15 MBASE1—Memory Base Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 20–21h
Default Value: FFF0h
Access: RW, RO
Size: 16 bits

This register controls the processor-to-PCI Express non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1 MB boundary.

Bit	Access & Default	Description
15:4	RW FFFh	**Memory Address Base (MBASE):** This field corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express.
3:0	RO 0h	Reserved

6.1.16 MLIMIT1—Memory Limit Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 22–23h
Default Value: 0000h
Access: RW, RO
Size: 16 bits

This register controls the processor to PCI Express-G non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1MB aligned memory block. NOTE: Memory range covered by MBASE and MLIMIT registers are used to map non-prefetchable PCI Express address ranges (typically where control/status memory-mapped I/O data structures of the graphics controller will reside) and PMBASE and PMLIMIT are used to map prefetchable address ranges (typically graphics local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the prefetchable address range for improved processor - PCI Express memory access performance.

Note also that configuration software is responsible for programming all address range registers (prefetchable, non-prefetchable) with the values that provide exclusive address ranges i.e. prevent overlap with each other and/or with the ranges covered with the main memory. There is no provision in the (G)MCH hardware to enforce prevention of overlap and operations of the system in the case of overlap are not ensured.

Bit	Access & Default	Description
15:4	RW 000h	**Memory Address Limit (MLIMIT):** This field corresponds to A[31:20] of the upper limit of the address range passed to PCI Express.
3:0	RO 0h	Reserved

6.1.17 PMBASE1—Prefetchable Memory Base Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 24–25h
Default Value: FFF1h
Access: RW, RO
Size: 16 bits

This register in conjunction with the corresponding Upper Base Address register controls the processor-to-PCI Express prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Base Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1 MB boundary.

Bit	Access & Default	Description
15:4	RW FFFh	**Prefetchable Memory Base Address (MBASE):** This field corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express.
3:0	RO 1h	**64-bit Address Support:** This field indicates that the upper 32 bits of the prefetchable memory region base address are contained in the Prefetchable Memory base Upper Address register at 28h.

6.1.18 PMLIMIT1—Prefetchable Memory Limit Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 26–27h
Default Value: 0001h
Access: RW, RO
Size: 16 bits

This register in conjunction with the corresponding Upper Limit Address register controls the processor-to-PCI Express prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Limit Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1MB aligned memory block. Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e. prefetchable) from the processor perspective.

Bit	Access & Default	Description
15:4	RW 000h	**Prefetchable Memory Address Limit (PMLIMIT):** This field corresponds to A[31:20] of the upper limit of the address range passed to PCI Express.
3:0	RO 1h	**64-bit Address Support:** This field indicates that the upper 32 bits of the prefetchable memory region limit address are contained in the Prefetchable Memory Base Limit Address register at 2Ch

6.1.19 PMBASEU1—Prefetchable Memory Base Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 28–2Bh
Default Value: 00000000h
Access: RW
Size: 32 bits

The functionality associated with this register is present in the PEG design implementation.

This register in conjunction with the corresponding Upper Base Address register controls the processor-to-PCI Express prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Base Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1 MB boundary.

Bit	Access & Default	Description
31:0	RW 00000000h	**Prefetchable Memory Base Address (MBASEU):** This field corresponds to A[63:32] of the lower limit of the prefetchable memory range that will be passed to PCI Express.

6.1.20 PMLIMITU1—Prefetchable Memory Limit Address

B/D/F/Type:	0/1/0/PCI
Address Offset:	2C–2Fh
Default Value:	00000000h
Access:	RW
Size:	32 bits

The functionality associated with this register is present in the PEG design implementation.

This register in conjunction with the corresponding Upper Limit Address register controls the processor-to-PCI Express prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40- bit address. The lower 8 bits of the Upper Limit Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1MB aligned memory block.

Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e. prefetchable) from the processor perspective.

Bit	Access & Default	Description
31:0	RW 00000000h	**Prefetchable Memory Address Limit (MLIMITU):** This field corresponds to A[63:32] of the upper limit of the prefetchable Memory range that will be passed to PCI Express.

6.1.21 CAPPTR1—Capabilities Pointer

B/D/F/Type: 0/1/0/PCI
Address Offset: 34h
Default Value: 88h
Access: RO
Size: 8 bits

The capabilities pointer provides the address offset to the location of the first entry in this device's linked list of capabilities.

Bit	Access & Default	Description
7:0	RO 88h	**First Capability (CAPPTR1):** The first capability in the list is the Subsystem ID and Subsystem Vendor ID Capability.

6.1.22 INTRLINE1—Interrupt Line

B/D/F/Type: 0/1/0/PCI
Address Offset: 3Ch
Default Value: 00h
Access: RW
Size: 8 bits

This register contains interrupt line routing information. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.

Bit	Access & Default	Description
7:0	RW 00h	**Interrupt Connection (INTCON):** Used to communicate interrupt line routing information.

6.1.23 INTRPIN1—Interrupt Pin

B/D/F/Type: 0/1/0/PCI
Address Offset: 3Dh
Default Value: 01h
Access: RO
Size: 8 bits

This register specifies which interrupt pin this device uses.

Bit	Access & Default	Description
7:0	RO 01h	**Interrupt Pin (INTPIN):** As a single function device, the PCI Express device specifies INTA as its interrupt pin. 01h=INTA.

6.1.24 BCTRL1—Bridge Control

B/D/F/Type: 0/1/0/PCI
Address Offset: 3E–3Fh
Default Value: 0000h
Access: RO, RW
Size: 16 bits

This register provides extensions to the PCICMD1 register that are specific to PCI-to-PCI bridges. The BCTRL provides additional control for the secondary interface (i.e., PCI Express) as well as some bits that affect the overall behavior of the "virtual" Host-PCI Express bridge in the (G)MCH (e.g., VGA compatible address ranges mapping).

Bit	Access & Default	Description
15:12	RO 0h	Reserved
11	RO 0b	**Discard Timer SERR# Enable (DTSERRE):** Not Applicable or Implemented. Hardwired to 0.
10	RO 0b	**Discard Timer Status (DTSTS):** Not Applicable or Implemented. Hardwired to 0.
9	RO 0b	**Secondary Discard Timer (SDT):** Not Applicable or Implemented. Hardwired to 0.
8	RO 0b	**Primary Discard Timer (PDT):** Not Applicable or Implemented. Hardwired to 0.
7	RO 0b	**Fast Back-to-Back Enable (FB2BEN):** Not Applicable or Implemented. Hardwired to 0.
6	RW 0b	**Secondary Bus Reset (SRESET):** Setting this bit triggers a hot reset on the corresponding PCI Express Port. This will force the LTSSM to transition to the Hot Reset state (via Recovery) from L0, L0s, or L1 states.
5	RO 0b	**Master Abort Mode (MAMODE):** Does not apply to PCI Express. Hardwired to 0.
4	RW 0b	**VGA 16-bit Decode (VGA16D):** Enables the PCI-to-PCI bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 KB. This bit only has meaning if bit 3 (VGA Enable) of this register is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. 0 = Execute 10-bit address decodes on VGA I/O accesses. 1 = Execute 16-bit address decodes on VGA I/O accesses.
3	RW 0b	**VGA Enable (VGAEN):** This bit controls the routing of processor initiated transactions targeting VGA compatible I/O and memory address ranges.

Bit	Access & Default	Description
2	RW 0b	**ISA Enable (ISAEN):** Needed to exclude legacy resource decode to route ISA resources to legacy decode path. This bit modifies the response by the (G)MCH to an I/O access issued by the processor that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 0 = All addresses defined by the IOBASE and IOLIMIT for processor I/O transactions will be mapped to PCI Express. 1 = (G)MCH will not forward to PCI Express any I/O transactions addressing the last 768 bytes in each 1 KB block even if the addresses are within the range defined by the IOBASE and IOLIMIT registers.
1	RW 0b	**SERR Enable (SERREN):** 0 = No forwarding of error messages from secondary side to primary side that could result in an SERR. 1 = ERR_COR, ERR_NONFATAL, and ERR_FATAL messages result in SERR message when individually enabled by the Root Control register.
0	RW 0b	**Parity Error Response Enable (PEREN):** This bit controls whether or not the Master Data Parity Error bit in the Secondary Status register is set when the (G)MCH receives across the link (upstream) a Read Data Completion Poisoned TLP. 0 = Master Data Parity Error bit in Secondary Status register can NOT be set. 1 = Master Data Parity Error bit in Secondary Status register CAN be set.

6.1.25 PM_CAPID1—Power Management Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: 80–83h
Default Value: C8039001h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:27	RO 19h	**PME Support (PMES):** This field indicates the power states in which this device may indicate PME wake via PCI Express messaging. D0, D3hot & D3cold. This device is not required to do anything to support D3hot & D3cold, it simply must report that those states are supported. Refer to the PCI Power Management 1.1 specification for encoding explanation and other power management details.
26	RO 0b	**D2 Power State Support (D2PSS):** Hardwired to 0 to indicate that the D2 power management state is NOT supported.
25	RO 0b	**D1 Power State Support (D1PSS):** Hardwired to 0 to indicate that the D1 power management state is NOT supported.
24:22	RO 000b	**Auxiliary Current (AUXC):** Hardwired to 0 to indicate that there are no 3.3Vaux auxiliary current requirements.
21	RO 0b	**Device Specific Initialization (DSI):** Hardwired to 0 to indicate that special initialization of this device is NOT required before generic class device driver is to use it.
20	RO 0b	**Auxiliary Power Source (APS):** Hardwired to 0.
19	RO 0b	**PME Clock (PMECLK):** Hardwired to 0 to indicate this device does NOT support PMEB generation.
18:16	RO 011b	**PCI PM CAP Version (PCIPMCV):** A value of 011b indicates that this function complies with revision 1.2 of the PCI Power Management Interface Specification.
15:8	RO 90h	**Pointer to Next Capability (PNC):** This contains a pointer to the next item in the capabilities list. If MSICH (CAPL[0] @ 7Fh) is 0, then the next item in the capabilities list is the Message Signaled Interrupts (MSI) capability at 90h
7:0	RO 01h	**Capability ID (CID):** Value of 01h identifies this linked list item (capability structure) as being for PCI Power Management registers.

6.1.26 PM_CS1—Power Management Control/Status

B/D/F/Type: 0/1/0/PCI
Address Offset: 84–87h
Default Value: 00000000h
Access: RO, RW/S, RW
Size: 32 bits

Bit	Access & Default	Description
31:16	RO 0000h	Reserved: Not Applicable or Implemented. Hardwired to 0.
15	RO 0b	**PME Status (PMESTS):** Indicates that this device does not support PME# generation from D3cold.
14:13	RO 00b	**Data Scale (DSCALE):** Indicates that this device does not support the power management data register.
12:9	RO 0h	**Data Select (DSEL):** Indicates that this device does not support the power management data register.
8	RW/S 0b	**PME Enable (PMEE):** Indicates that this device does not generate PMEB assertion from any D-state. 0 = PMEB generation not possible from any D State 1 = PMEB generation enabled from any D State The setting of this bit has no effect on hardware. See PM_CAP[15:11]
7:2	RO 00h	Reserved
1:0	RW 00b	**Power State (PS):** This field indicates the current power state of this device and can be used to set the device into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. 00 = D0 01 = D1 (Not supported in this device. 10 = D2 (Not supported in this device.) 11 = D3 Support of D3cold does not require any special action. While in the D3hot state, this device can only act as the target of PCI configuration transactions (for power management control). This device also cannot generate interrupts or respond to MMR cycles in the D3 state. The device must return to the D0 state to be fully-functional. When the Power State is other than D0, the bridge will Master Abort (i.e., not claim) any downstream cycles (with exception of type 0 configuration cycles). Consequently, these unclaimed cycles will go down DMI and come back up as Unsupported Requests, which the (G)MCH logs as Master Aborts in Device 0 PCISTS[13] There is no additional hardware functionality required to support these Power States.

6.1.27 SS_CAPID—Subsystem ID and Vendor ID Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: 88–8Bh
Default Value: 0000800Dh
Access: RO
Size: 32 bits

This capability is used to uniquely identify the subsystem where the PCI device resides. Because this device is an integrated part of the system and not an add-in device, it is anticipated that this capability will never be used. However, it is necessary because Microsoft will test for its presence.

Bit	Access & Default	Description
31:16	RO 0000h	Reserved
15:8	RO 80h	**Pointer to Next Capability (PNC):** This contains a pointer to the next item in the capabilities list which is the PCI Power Management capability.
7:0	RO 0Dh	**Capability ID (CID):** Value of 0Dh identifies this linked list item (capability structure) as being for SSID/SSVID registers in a PCI-to-PCI Bridge.

6.1.28 SS—Subsystem ID and Subsystem Vendor ID

B/D/F/Type: 0/1/0/PCI
Address Offset: 8C–8Fh
Default Value: 00008086h
Access: RWO
Size: 32 bits

System BIOS can be used as the mechanism for loading the SSID/SVID values. These values must be preserved through power management transitions and a hardware reset.

Bit	Access & Default	Description
31:16	RWO 0000h	**Subsystem ID (SSID):** Identifies the particular subsystem and is assigned by the vendor.
15:0	RWO 8086h	**Subsystem Vendor ID (SSVID):** Identifies the manufacturer of the subsystem and is the same as the vendor ID which is assigned by the PCI Special Interest Group.

6.1.29 MSI_CAPID—Message Signaled Interrupts Capability ID

B/D/F/Type: 0/1/0/PCI
Address Offset: 90–91h
Default Value: A005h
Access: RO
Size: 16 bits

When a device supports MSI it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.

Bit	Access & Default	Description
15:8	RO A0h	**Pointer to Next Capability (PNC):** This contains a pointer to the next item in the capabilities list which is the PCI Express capability.
7:0	RO 05h	**Capability ID (CID):** Value of 05h identifies this linked list item (capability structure) as being for MSI registers.

6.1.30 MC—Message Control

B/D/F/Type: 0/1/0/PCI
Address Offset: 92–93h
Default Value: 0000h
Access: RW, RO
Size: 16 bits

System software can modify bits in this register, but the device is prohibited from doing so.

If the device writes the same message multiple times, only one of those messages is ensured to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

Bit	Access & Default	Description
15:8	RO 00h	Reserved
7	RO 0b	**64-bit Address Capable (64AC):** Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message Address register and is incapable of generating a 64-bit memory address.
6:4	RW 000b	**Multiple Message Enable (MME):** System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. The encoding is the same as for the MMC field below.
3:1	RO 000b	**Multiple Message Capable (MMC):** System software reads this field to determine the number of messages being requested by this device. 000 = 1 message requested All others are reserved.

Bit	Access & Default	Description
0	RW 0b	**MSI Enable (MSIEN):** Controls the ability of this device to generate MSIs. 0 = MSI will not be generated. 1 = MSI will be generated when we receive PME or HotPlug messages. INTA will not be generated and INTA Status (PCISTS1[3]) will not be set.

6.1.31 MA—Message Address

B/D/F/Type: 0/1/0/PCI
Address Offset: 94–97h
Default Value: 00000000h
Access: RW, RO
Size: 32 bits

Bit	Access & Default	Description
31:2	RW 00000000h	**Message Address (MA):** Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
1:0	RO 00b	**Force DWord Align (FDWA):** Hardwired to 0 so that addresses assigned by system software are always aligned on a DWord address boundary.

6.1.32 MD—Message Data

B/D/F/Type: 0/1/0/PCI
Address Offset: 98–99h
Default Value: 0000h
Access: RW
Size: 16 bits

Bit	Access & Default	Description
15:0	RW 0000h	**Message Data (MD):** Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.

6.1.33 PEG_CAPL—PCI Express*-G Capability List

B/D/F/Type: 0/1/0/PCI
Address Offset: A0–A1h
Default Value: 0010h
Access: RO
Size: 16 bits

This register enumerates the PCI Express capability structure.

Bit	Access & Default	Description
15:8	RO 00h	**Pointer to Next Capability (PNC):** This value terminates the capabilities list. The Virtual Channel capability and any other PCI Express specific capabilities that are reported via this mechanism are in a separate capabilities list located entirely within PCI Express Extended Configuration Space.
7:0	RO 10h	**Capability ID (CID):** Identifies this linked list item (capability structure) as being for PCI Express registers.

6.1.34 PEG_CAP—PCI Express*-G Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: A2–A3h
Default Value: 0141h
Access: RO, RWO
Size: 16 bits

This register indicates PCI Express device capabilities.

Bit	Access & Default	Description
15:14	RO 00b	Reserved
13:9	RO 00h	**Interrupt Message Number (IMN):** Not Applicable or Implemented. Hardwired to 0.
8	RWO 1b	**Slot Implemented (SI):** 0 = The PCI Express Link associated with this port is connected to an integrated component or is disabled. 1 = The PCI Express Link associated with this port is connected to a slot.
7:4	RO 4h	**Device/Port Type (DPT):** Hardwired to 4h to indicate root port of PCI Express Root Complex.
3:0	RO 1h	**PCI Express Capability Version (PCI EXPRESS*CV):** Hardwired to 1 as it is the first version.

6.1.35 DCAP—Device Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: A4–A7h
Default Value: 00008000h
Access: RO
Size: 32 bits

This register indicates PCI Express device capabilities.

Bit	Access & Default	Description
31:16	RO 0000h	Reserved: Not Applicable or Implemented. Hardwired to 0.
15	RO 1b	**Role Based Error Reporting (RBER):** This bit indicates that this device implements the functionality defined in the Error Reporting ECN as required by the PCI Express 1.1 specification.
14:6	RO 000h	Reserved: Not Applicable or Implemented. Hardwired to 0.
5	RO 0b	**Extended Tag Field Supported (ETFS):** Hardwired to indicate support for 5-bit Tags as a Requestor.
4:3	RO 00b	**Phantom Functions Supported (PFS):** Not Applicable or Implemented. Hardwired to 0.
2:0	RO 000b	**Max Payload Size (MPS):** Hardwired to indicate 128B max supported payload for Transaction Layer Packets (TLP).

6.1.36 DCTL—Device Control

B/D/F/Type: 0/1/0/PCI
Address Offset: A8–A9h
Default Value: 0000h
Access: RO, RW
Size: 16 bits

This register provides control for PCI Express device specific capabilities.

The error reporting enable bits are in reference to errors detected by this device, not error messages received across the link. The reporting of error messages (ERR_CORR, ERR_NONFATAL, ERR_FATAL) received by Root Port is controlled exclusively by Root Port Command Register.

Bit	Access & Default	Description
15:8	RO 000h	Reserved
7:5	RW 000b	**Max Payload Size (MPS):** 000 = 128B max supported payload for Transaction Layer Packets (TLP). As a receiver, the Device must handle TLPs as large as the set value; as transmitter, the Device must not generate TLPs exceeding the set value. All other encodings are reserved. Hardware will actually ignore this field. It is writeable only to support compliance testing.
4	RO 0b	Reserved: For Enable Relaxed Ordering
3	RW 0b	**Unsupported Request Reporting Enable (URRE):** When set, allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_CORR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_CORR is signaled when an unmasked Advisory Non-Fatal UR is received. An ERR_FATAL or ERR_NONFATAL is sent to the Root Control register when an uncorrectable non-Advisory UR is received with the severity bit set in the Uncorrectable Error Severity register.
2	RW 0b	**Fatal Error Reporting Enable (FERE):** When set, enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	RW 0b	**Non-Fatal Error Reporting Enable (NERE):** When set, enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	RW 0b	**Correctable Error Reporting Enable (CERE):** When set, enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

6.1.37 DSTS—Device Status

B/D/F/Type: 0/1/0/PCI
Address Offset: AA–ABh
Default Value: 0000h
Access: RO, RWC
Size: 16 bits

This register reflects status corresponding to controls in the Device Control register. The error reporting bits are in reference to errors detected by this device, not errors messages received across the link.

Bit	Access & Default	Description
15:6	RO 000h	Reserved and Zero: For future R/WC/S implementations; software must use 0 for writes to bits.
5	RO 0b	**Transactions Pending (TP):** 0 = All pending transactions (including completions for any outstanding non-posted requests on any used virtual channel) have been completed. 1 = Device has transaction(s) pending (including completions for any outstanding non-posted requests for all used Traffic Classes).
4	RO 0b	Reserved
3	RWC 0b	**Unsupported Request Detected (URD):** 0 = Unsupported request **Not** detected. 1 = Device received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register. Additionally, the Non-Fatal Error Detected bit or the Fatal Error Detected bit is set according to the setting of the Unsupported Request Error Severity bit. In production systems setting the Fatal Error Detected bit is not an option as support for AER will not be reported.
2	RWC 0b	**Fatal Error Detected (FED):** 0 = Fatal error **Not** detected. 1 = Fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the uncorrectable error mask register.
1	RWC 0b	**Non-Fatal Error Detected (NFED):** 0 = Non-Fatal error **Not** detected. 1 = Non-fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the uncorrectable error mask register.

Bit	Access & Default	Description
0	RWC 0b	**Correctable Error Detected (CED):** 0 = Correctable error **Not** detected. 1 = Correctable error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. When Advanced Error Handling is enabled, errors are logged in this register regardless of the settings of the correctable error mask register.

6.1.38 LCAP—Link Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: AC–AFh
Default Value: 02014D01h
Access: RO, RWO
Size: 32 bits

This register indicates PCI Express device specific capabilities.

Bit	Access & Default	Description
31:24	RO 02h	**Port Number (PN):** This field indicates the PCI Express port number for the given PCI Express link. Matches the value in Element Self Description[31:24].
23:21	RO 000b	Reserved
20	RO 0b	**Data Link Layer Link Active Reporting Capable (DLLLARC):** For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine. For a hot-plug capable Downstream Port (as indicated by the Hot-Plug Capable field of the Slot Capabilities register), this bit must be set to 1b. For Upstream Ports and components that do not support this optional capability, this bit must be hardwired to 0b.
19	RO 0b	**Surprise Down Error Reporting Capable (SDERC):** For a Downstream Port, this bit must be set to 1b if the component supports the optional capability of detecting and reporting a Surprise Down error condition. For Upstream Ports and components that do not support this optional capability, this bit must be hardwired to 0b.

Bit	Access & Default	Description
18	RO 0b	**Clock Power Management (CPM):** A value of 1b in this bit indicates that the component tolerates the removal of any reference clock(s) when the link is in the L1 and L2/3 Ready link states. A value of 0b indicates the component does not have this capability and that reference clock(s) must not be removed in these link states. This capability is applicable only in form factors that support “clock request” (CLKREQ#) capability. For a multi-function device, each function indicates its capability independently. Power Management configuration software must only permit reference clock removal if all functions of the multifunction device indicate a 1b in this bit.
17:15	RWO 010b	**L1 Exit Latency (L1ELAT):** This field indicates the length of time this Port requires to complete the transition from L1 to L0. The value 010 b indicates the range of 2 us to less than 4 us. Both bytes of this register that contain a portion of this field must be written simultaneously in order to prevent an intermediate (and undesired) value from ever existing.
14:12	RO 100b	**L0s Exit Latency (L0SELAT):** Indicates the length of time this Port requires to complete the transition from L0s to L0. 000 = Less than 64 ns 001 = 64ns to less than 128ns 010 = 128ns to less than 256 ns 011 = 256ns to less than 512 ns 100 = 512ns to less than 1 us 101 = 1 us to less than 2 us 110 = 2 us – 4 us 111 = More than 4 us The actual value of this field depends on the common Clock Configuration bit (LCTL[6]) and the Common and Non-Common clock L0s Exit Latency values in PEGL0SLAT (Offset 22Ch)
11:10	RWO 11b	**Active State Link PM Support (ASLPMS):** 00 = Reserved 01 = L0s is supported 10 = Reserved 11 = L1 and L0s are supported
9:4	RO 10h	**Max Link Width (MLW):** This field indicates the maximum number of lanes supported for this link.
3:0	RO 1h	**Max Link Speed (MLS):** Hardwired to indicate 2.5 Gb/s.

6.1.39 LCTL—Link Control

B/D/F/Type: 0/1/0/PCI
Address Offset: B0–B1h
Default Value: 0000h
Access: RO, RW, RW/SC
Size: 16 bits
BIOS Optimal Default 0h

This register allows control of PCI Express link.

Bit	Access & Default	Description
15:9	RO 0000000b	Reserved
8	RO 0b	**Enable Clock Power Management (ECPM):** Applicable only for form factors that support a "Clock Request" (CLKREQ#) mechanism, this enable functions as follows 0 = Disable. Clock power management is disabled and device must hold CLKREQ# signal low (Default) 1 = Enable. Device is permitted to use CLKREQ# signal to power manage link clock according to protocol defined in appropriate form factor specification. Components that do not support Clock Power Management (as indicated by a 0b value in the Clock Power Management bit of the Link Capabilities Register) must hardwire this bit to 0b.
7	RW 0b	**Extended Synch (ES):** 0 = Standard Fast Training Sequence (FTS). 1 = Forces the transmission of additional ordered sets when exiting the L0s state and when in the Recovery state. This mode provides external devices (e.g., logic analyzers) monitoring the Link time to achieve bit and symbol lock before the link enters L0 and resumes communication. This is a test mode only and may cause other undesired side effects such as buffer overflows or underruns.
6	RW 0b	**Common Clock Configuration (CCC):** The state of this bit affects the L0s Exit Latency reported in LCAP[14:12] and the N_FTS value advertised during link training. See PEGL0SLAT at offset 22Ch. 0 = This component and the component at the opposite end of this Link are operating with asynchronous reference clock. 1 = This component and the component at the opposite end of this Link are operating with a distributed common reference clock.
5	RW/SC 0b	**Retrain Link (RL):** This bit always returns 0 when read. This bit is cleared automatically (no need to write a 0). 0 = Normal operation. 1 = Full Link retraining is initiated by directing the Physical Layer LTSSM from L0, L0s, or L1 states to the Recovery state.

Bit	Access & Default	Description
4	RW 0b	**Link Disable (LD):** Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state. 0 = Normal operation 1 = Link is disabled. Forces the LTSSM to transition to the Disabled state (via Recovery) from L0, L0s, or L1 states. Link retraining happens automatically on 0 to 1 transition, just like when coming out of reset.
3	RO 0b	**Read Completion Boundary (RCB):** Hardwired to 0 to indicate 64 byte.
2	RW 0b	**Far-End Digital Loopback (FEDLB):**
1:0	RW 00b	**Active State PM (ASPM):** This field controls the level of active state power management supported on the given link. 00 = Disabled 01 = L0s Entry Supported 10 = Reserved 11 = L0s and L1 Entry Supported

6.1.40 LSTS—Link Status

B/D/F/Type: 0/1/0/PCI
Address Offset: B2–B3h
Default Value: 1001h
Access: RO
Size: 16 bits

This register indicates PCI Express link status.
“

Bit	Access & Default	Description
15:14	RO 00b	Reserved and Zero: For future R/WC/S implementations; software must use 0 for writes to bits.
13	RO 0b	**Data Link Layer Link Active (Optional) (DLLLA):** This bit indicates the status of the Data Link Control and Management State Machine. It returns a 1b to indicate the DL_Active state, 0b otherwise. This bit must be implemented if the corresponding Data Link Layer Active Capability bit is implemented. Otherwise, this bit must be hardwired to 0b.
12	RO 1b	**Slot Clock Configuration (SCC):** 0 = The device uses an independent clock irrespective of the presence of a reference on the connector. 1 = The device uses the same physical reference clock that the platform provides on the connector.
11	RO 0b	**Link Training (LTRN):** This bit indicates that the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state once Link training is complete.
10	RO 0b	**Undefined:** The value read from this bit is undefined. In previous versions of this specification, this bit was used to indicate a Link Training Error. System software must ignore the value read from this bit. System software is permitted to write any value to this bit.
9:4	RO 00h	**Negotiated Width (NW):** Indicates negotiated link width. This field is valid only when the link is in the L0, L0s, or L1 states (after link width negotiation is successfully completed). 00h = Reserved 01h = X1 02h = Reserved 04h = Reserved 08h = Reserved 10h = X16 All other encodings are reserved.
3:0	RO 1h	**Negotiated Speed (NS):** Indicates negotiated link speed. 1h = 2.5 Gb/s All other encodings are reserved.

6.1.41 SLOTCAP—Slot Capabilities

B/D/F/Type: 0/1/0/PCI
Address Offset: B4–B7h
Default Value: 00040000h
Access: RWO, RO
Size: 32 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Bit	Access & Default	Description
31:19	RWO 0000h	**Physical Slot Number (PSN):** Indicates the physical slot number attached to this Port.
18	RWO 1b	**No Command Completed Support (NCCS):** 1 = This slot does not generate software notification when an issued command is completed by the Hot-Plug Controller. This bit is only permitted to be set to 1b if the hotplug capable port is able to accept writes to all fields of the Slot Control register without delay between successive writes.
17	RO 0b	Reserved for Electromechanical Interlock Present (EIP):
16:15	RWO 00b	**Slot Power Limit Scale (SPLS):** This field specifies the scale used for the Slot Power Limit Value. 00 = 1.0x 01 = 0.1x 10 = 0.01x 11 = 0.001x If this field is written, the link sends a Set_Slot_Power_Limit message.
14:7	RWO 00h	**Slot Power Limit Value (SPLV):** In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. If this field is written, the link sends a Set_Slot_Power_Limit message.
6	RO 0b	**Hot-plug Capable (HPC):** 0 = Not Hot-plug capable 1 = Slot is capable of supporting hot-lug operations.
5	RO 0b	**Hot-plug Surprise (HPS):** 0 = No Hot-plug surprise 1 = An adapter present in this slot might be removed from the system without any prior notification. This is a form factor specific capability. This bit is an indication to the operating system to allow for such removal without impacting continued software operation.

Bit	Access & Default	Description
4	RO 0b	**Power Indicator Present (PIP):** 0 = No power indicator 1 = A Power Indicator is electrically controlled by the chassis for this slot.
3	RO 0b	**Attention Indicator Present (AIP):** 0 = No Attention indicator 1 = An Attention Indicator is electrically controlled by the chassis.
2	RO 0b	**MRL Sensor Present (MSP):** 0 = No MRL sensor 1 = MRL Sensor is implemented on the chassis for this slot.
1	RO 0b	**Power Controller Present (PCP):** 0 = No power controller 1 = A software programmable Power Controller is implemented for this slot/adapter (depending on form factor).
0	RO 0b	**Attention Button Present (ABP):** 0 = No attention button 1 = An Attention Button for this slot is electrically controlled by the chassis.

6.1.42 SLOTCTL—Slot Control

B/D/F/Type: 0/1/0/PCI
Address Offset: B8–B9h
Default Value: 01C0h
Access: RO, RW
Size: 16 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Bit	Access & Default	Description
15:13	RO 000b	Reserved
12	RO 0b	**Data Link Layer State Changed Enable (DLLSCE):** If the Data Link Layer Link Active capability is implemented, when set to 1b, this field enables software notification when Data Link Layer Link Active field is changed.
11	RO 0b	**Electromechanical Interlock Control (EIC):** If an Electromechanical Interlock is implemented, a write of 1b to this field causes the state of the interlock to toggle. A write of 0b to this field has no effect. A read to this register always returns a 0.

Bit	Access & Default	Description
10	RO 0b	**Power Controller Control (PCC):** If a Power Controller is implemented, this field when written sets the power state of the slot per the defined encodings. Reads of this field must reflect the value from the latest write, even if the corresponding hotplug command is not complete, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. Depending on the form factor, the power is turned on/off either to the slot or within the adapter. Note that in some cases the power controller may autonomously remove slot power or not respond to a power-up request based on a detected fault condition, independent of the Power Controller Control setting. The defined encodings are: 0 = Power On 1 = Power Off If the Power Controller Implemented field in the Slot Capabilities register is set to 0b, then writes to this field have no effect and the read value of this field is undefined.
9:8	RO 01b	**Power Indicator Control (PIC):** If a Power Indicator is implemented, writes to this field set the Power Indicator to the written state. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. 00 = Reserved 01 = On 10 = Blink 11 = Off
7:6	RO 11b	**Attention Indicator Control (AIC):** If an Attention Indicator is implemented, writes to this field set the Attention Indicator to the written state. Reads of this field must reflect the value from the latest write, even if the corresponding hot-plug command is not complete, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. If the indicator is electrically controlled by chassis, the indicator is controlled directly by the downstream port through implementation specific mechanisms. 00 = Reserved 01 = On 10 = Blink 11 = Off

Bit	Access & Default	Description
5	RO 0b	**Hot-plug Interrupt Enable (HPIE):** 0 = Disable 1 = Enables generation of an interrupt on enabled hot-plug events Default value of this field is 0b. If the Hot Plug Capable field in the Slot Capabilities register is set to 0b, this bit is permitted to be read-only with a value of 0b.
4	RO 0b	**Command Completed Interrupt Enable (CCI):** If Command Completed notification is supported (as indicated by No Command Completed Support field of Slot Capabilities Register), when set to 1b, this bit enables software notification when a hot-plug command is completed by the Hot-Plug Controller. If Command Completed notification is not supported, this bit must be hardwired to 0b.
3	RW 0b	**Presence Detect Changed Enable (PDCE):** 0 = Disable 1 = Enables software notification on a presence detect changed event.
2	RO 0b	**MRL Sensor Changed Enable (MSCE):** If the MRL Sensor Present field in the Slot Capabilities register is set to 0b, this bit is permitted to be read-only with a value of 0b. 0 = Disable (default) 1 = Enables software notification on a MRL sensor changed event.
1	RO 0b	**Power Fault Detected Enable (PFDE):** If Power Fault detection is not supported, this bit is permitted to be read-only with a value of 0b. 0 = Disable (default) 1 = Enables software notification on a power fault event.
0	RO 0b	**Attention Button Pressed Enable (ABPE):** 0 = Disable (default) 1 = Enables software notification on an attention button pressed event.

6.1.43 SLOTSTS—Slot Status

B/D/F/Type: 0/1/0/PCI
Address Offset: BA–BBh
Default Value: 0000h
Access: RO, RWC
Size: 16 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Bit	Access & Default	Description
15:7	RO 0000000b	Reserved and Zero: For future R/WC/S implementations; software must use 0 for writes to bits.
6	RO 0b	**Presence Detect State (PDS):** This bit indicates the presence of an adapter in the slot, reflected by the logical "OR" of the Physical Layer in-band presence detect mechanism and, if present, any out-of-band presence detect mechanism defined for the slot's corresponding form factor. Note that the in-band presence detect mechanism requires that power be applied to an adapter for its presence to be detected. Consequently, form factors that require a power controller for hot-plug must implement a physical pin presence detect mechanism. 0 = Slot Empty 1 = Card Present in slot This register must be implemented on all Downstream Ports that implement slots. For Downstream Ports not connected to slots (where the Slot Implemented bit of the PCI Express Capabilities Register is 0b), this bit must return 1b.
5	RO 0b	Reserved
4	RO 0b	**Command Completed (CC):** If Command Completed notification is supported (as indicated by No Command Completed Support field of Slot Capabilities Register), this bit is set when a hot-plug command has completed and the Hot-Plug Controller is ready to accept a subsequent command. The Command Completed status bit is set as an indication to host software that the Hot-Plug Controller has processed the previous command and is ready to receive the next command; it provides no assurance that the action corresponding to the command is complete. If Command Completed notification is not supported, this bit must be hardwired to 0b.
3	RWC 0b	**Detect Changed (PDC):** This bit is set when the value reported in Presence Detect State is changed.
2	RO 0b	**MRL Sensor Changed (MSC):** If an MRL sensor is implemented, this bit is set when a MRL Sensor state change is detected. If an MRL sensor is not implemented, this bit must not be set.

Bit	Access & Default	Description
1	RO 0b	**Power Fault Detected (PFD):** If a Power Controller that supports power fault detection is implemented, this bit is set when the Power Controller detects a power fault at this slot. Note that, depending on hardware capability, it is possible that a power fault can be detected at any time, independent of the Power Controller Control setting or the occupancy of the slot. If power fault detection is not supported, this bit must not be set.
0	RO 0b	**Attention Button Pressed (ABP):** If an Attention Button is implemented, this bit is set when the attention button is pressed. If an Attention Button is not supported, this bit must not be set.

6.1.44 RCTL—Root Control

B/D/F/Type: 0/1/0/PCI
Address Offset: BC–BDh
Default Value: 0000h
Access: RO, RW
Size: 16 bits

This register allows control of PCI Express Root Complex specific parameters. The system error control bits in this register determine if corresponding SERRs are generated when our device detects an error (reported in this device's Device Status register) or when an error message is received across the link. Reporting of SERR as controlled by these bits takes precedence over the SERR Enable in the PCI Command Register.

Bit	Access & Default	Description
15:4	RO 000h	Reserved
3	RW 0b	**PME Interrupt Enable (PMEIE):** 0 = No interrupts are generated as a result of receiving PME messages. 1 = Enables interrupt generation upon receipt of a PME message as reflected in the PME Status bit of the Root Status Register. A PME interrupt is also generated if the PME Status bit of the Root Status Register is set from a cleared state.
2	RW 0b	**System Error on Fatal Error Enable (SEFEE):** This bit controls the Root Complex's response to fatal errors. 0 = No SERR generated on receipt of fatal error. 1 = SERR should be generated if a fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.

Bit	Access & Default	Description
1	RW 0b	**System Error on Non-Fatal Uncorrectable Error Enable (SENFUEE):** This bit controls the Root Complex's response to non-fatal errors. 0 = No SERR generated on receipt of non-fatal error. 1 = SERR should be generated if a non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
0	RW 0b	**System Error on Correctable Error Enable (SECEE):** This bit controls the Root Complex's response to correctable errors. 0 = No SERR generated on receipt of correctable error. 1 = SERR should be generated if a correctable error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.

6.1.45 RSTS—Root Status

B/D/F/Type: 0/1/0/PCI
Address Offset: C0–C3h
Default Value: 00000000h
Access: RO, RWC
Size: 32 bits

This register provides information about PCI Express Root Complex specific parameters.

Bit	Access & Default	Description
31:18	RO 0000h	Reserved
17	RO 0b	**PME Pending (PMEP):** 1 = Another PME is pending when the PME Status bit is set. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the Requestor ID appropriately. The PME pending bit is cleared by hardware if no more PMEs are pending.
16	RWC 0b	**PME Status (PMES):** 1 = PME was asserted by the requestor ID indicated in the PME Requestor ID field. Subsequent PMEs are kept pending until the status register is cleared by writing a 1 to this field.
15:0	RO 0000h	**PME Requestor ID (PMERID):** This field indicates the PCI requestor ID of the last PME requestor.

6.1.46 PEGLC—PCI Express*-G Legacy Control

B/D/F/Type: 0/1/0/PCI
Address Offset: EC–EFh
Default Value: 00000000h
Access: RW, RO
Size: 32 bits

This register controls functionality that is needed by Legacy (non-PCI Express aware) operating systems during run time.

Bit	Access & Default	Description
31:3	RO 00000000h	Reserved
2	RW 0b	**PME GPE Enable (PMEGPE):** 0 = Do not generate GPE PME message when PME is received. 1 = Generate a GPE PME message when PME is received (Assert_PMEGPE and Deassert_PMEGPE messages on DMI). This enables the (G)MCH to support PMEs on the PEG port under legacy operating systems.
1	RW 0b	**Hot-Plug GPE Enable (HPGPE):** 0 = Do not generate GPE Hot-Plug message when Hot-Plug event is received. 1 = Generate a GPE Hot-Plug message when Hot-Plug Event is received (Assert_HPGPE and Deassert_HPGPE messages on DMI). This enables the (G)MCH to support Hot-Plug on the PEG port under legacy operating systems.
0	RW 0b	**General Message GPE Enable (GENGPE):** 0 = Do not forward received GPE assert/de-assert messages. 1 = Forward received GPE assert/de-assert messages. These general GPE message can be received via the PEG port from an external Intel device (i.e., PxH) and will be subsequently forwarded to the ICH (via Assert_GPE and Deassert_GPE messages on DMI). For example, PxH might send this message if a PCI Express device is hot plugged into a PxH downstream port.

6.1.47 VCECH—Virtual Channel Enhanced Capability Header

B/D/F/Type: 0/1/0/MMR
Address Offset: 100–103h
Default Value: 14010002h
Access: RO
Size: 32 bits

This register indicates PCI Express device Virtual Channel capabilities. Extended capability structures for PCI Express devices are located in PCI Express extended configuration space and have different field definitions than standard PCI capability structures.

Bit	Access & Default	Description
31:20	RO 140h	**Pointer to Next Capability (PNC):** The Link Declaration Capability is the next in the PCI Express extended capabilities list.
19:16	RO 1h	**PCI Express Virtual Channel Capability Version (PCI EXPRESS*VCCV):** Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification.
15:0	RO 0002h	**Extended Capability ID (ECID):** Value of 0002 h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

6.1.48 PVCCAP1—Port VC Capability Register 1

B/D/F/Type: 0/1/0/MMR
Address Offset: 104–107h
Default Value: 00000000h
Access: RO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access & Default	Description
31:7	RO 0000000h	Reserved
6:4	RO 000b	**Low Priority Extended VC Count (LPEVCC):** This field indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3	RO 0b	Reserved
2:0	RO 000b	**Extended VC Count (EVCC):** This field indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device.

6.1.49 PVCCAP2—Port VC Capability Register 2

B/D/F/Type: 0/1/0/MMR
Address Offset: 108–10Bh
Default Value: 00000000h
Access: RO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access & Default	Description
31:24	RO 00h	**VC Arbitration Table Offset (VCATO):** This field indicates the location of the VC Arbitration Table. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the Virtual Channel Capability Structure. A value of 0 indicates that the table is not present (due to fixed VC priority).
23:8	RO 0000h	Reserved
7:0	RO 00h	Reserved

6.1.50 PVCCTL—Port VC Control

B/D/F/Type: 0/1/0/MMR
Address Offset: 10C–10Dh
Default Value: 0000h
Access: RO, RW
Size: 16 bits

Bit	Access & Default	Description
15:4	RO 000h	Reserved
3:1	RW 000b	**VC Arbitration Select (VCAS):** This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. Since there is no other VC supported than the default, this field is reserved.
0	RO 0b	Reserved

6.1.51 VC0RCAP—VC0 Resource Capability

B/D/F/Type: 0/1/0/MMR
Address Offset: 110–113h
Default Value: 00000000h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:16	RO 0000h	Reserved
15	RO 0b	**Reject Snoop Transactions (RSNPT):** 0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:0	RO 0000h	Reserved

6.1.52 VC0RCTL—VC0 Resource Control

B/D/F/Type: 0/1/0/MMR
Address Offset: 114–117h
Default Value: 800000FFh
Access: RO, RW
Size: 32 bits

This register controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access & Default	Description
31	RO 1b	**VC0 Enable (VC0E):** For VC0, this is hardwired to 1 and read only as VC0 can never be disabled.
30:27	RO 0h	Reserved
26:24	RO 000b	**VC0 ID (VC0ID):** Assigns a VC ID to the VC resource. For VC0, this is hardwired to 0 and read only.
23:8	RO 0000h	Reserved
7:1	RW 7Fh	**TC/VC0 Map (TCVC0M):** This field indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO 1b	**TC0/VC0 Map (TC0VC0M):** Traffic Class 0 is always routed to VC0.

6.1.53 VC0RSTS—VC0 Resource Status

B/D/F/Type: 0/1/0/MMR
Address Offset: 11A–11Bh
Default Value: 0002h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2	RO 0000h	Reserved
1	RO 1b	**VC0 Negotiation Pending (VC0NP):** 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	RO 0b	Reserved

6.1.54 RCLDECH—Root Complex Link Declaration Enhanced

B/D/F/Type: 0/1/0/MMR
Address Offset: 140–143h
Default Value: 00010005h
Access: RO
Size: 32 bits

This capability declares links from this element (PEG) to other elements of the root complex component to which it belongs. See PCI Express specification for link/topology declaration requirements.

Bit	Access & Default	Description
31:20	RO 000h	**Pointer to Next Capability (PNC):** This is the last capability in the PCI Express extended capabilities list
19:16	RO 1h	**Link Declaration Capability Version (LDCV):** Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification.
15:0	RO 0005h	**Extended Capability ID (ECID):** Value of 0005h identifies this linked list item (capability structure) as being for PCI Express Link Declaration Capability.

6.1.55 ESD—Element Self Description

B/D/F/Type: 0/1/0/MMR
Address Offset: 144–147h
Default Value: 02000100h
Access: RO, RWO
Size: 32 bits

This register provides information about the root complex element containing this Link Declaration Capability.

Bit	Access & Default	Description
31:24	RO 02h	**Port Number (PN):** This field specifies the port number associated with this element with respect to the component that contains this element. This port number value is utilized by the Express port of the component to provide arbitration to this Root Complex Element.
23:16	RWO 00h	**Component ID (CID):** This field identifies the physical component that contains this Root Complex Element.
15:8	RO 01h	**Number of Link Entries (NLE):** This field indicates the number of link entries following the Element Self Description. This field reports 1 (to Express port only as we don't report any peer-to-peer capabilities in our topology).
7:4	RO 0h	Reserved
3:0	RO 0h	**Element Type (ET):** This field indicates the type of the Root Complex Element. Value of 0h represents a root port.

6.1.56 LE1D—Link Entry 1 Description

B/D/F/Type: 0/1/0/MMR
Address Offset: 150–153h
Default Value: 00000000h
Access: RO, RWO
Size: 32 bits

This register provides the first part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
31:24	RO 00h	**Target Port Number (TPN):** This field specifies the port number associated with the element targeted by this link entry (Express Port). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	RWO 00h	**Target Component ID (TCID):** This field identifies the physical or logical component that is targeted by this link entry.
15:2	RO 0000h	Reserved
1	RO 0b	**Link Type (LTYP):** This field indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	RWO 0b	**Link Valid (LV):** 0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.

6.1.57 LE1A—Link Entry 1 Address

B/D/F/Type: 0/1/0/MMR
Address Offset: 158–15Fh
Default Value: 0000000000000000h
Access: RO, RWO
Size: 64 bits

This register provides the second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
63:32	RO 00000000h	Reserved
31:12	RWO 00000h	**Link Address (LA):** This field contains the memory-mapped base address of the RCRB that is the target element (Express Port) for this link entry.
11:0	RO 000h	Reserved

6.1.58 PEGSSTS—PCI Express*-G Sequence Status

B/D/F/Type: 0/1/0/MMR
Address Offset: 218–21Fh
Default Value: 0000000000000FFFh
Access: RO
Size: 64 bits

This register provides PCI Express status reporting that is required by the PCI Express specification.

Bit	Access & Default	Description
63:60	RO 0h	Reserved
59:48	RO 000h	**Next Transmit Sequence Number (NTSN):** This field indicates the value of the NXT_TRANS_SEQ counter. This counter represents the transmit Sequence number to be applied to the next TLP to be transmitted onto the Link for the first time.
47:44	RO 0h	Reserved
43:32	RO 000h	**Next Packet Sequence Number (NPSN):** This field indicates the packet sequence number to be applied to the next TLP to be transmitted or re-transmitted onto the Link.
31:28	RO 0h	Reserved
27:16	RO 000h	**Next Receive Sequence Number (NRSN):** This field is the sequence number associated with the TLP that is expected to be received next.
15:12	RO 0h	Reserved
11:0	RO FFFh	**Last Acknowledged Sequence Number (LASN):** This field is the sequence number associated with the last acknowledged TLP.

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7 Direct Memory Interface (DMI) Registers

This Root Complex Register Block (RCRB) controls the (G)MCH-ICH9 serial interconnect. The base address of this space is programmed in DMIBAR in D0:F0 configuration space. Table 7-1 provides an address map of the DMI registers listed by address offset in ascending order. Section 7.1 provides register bit descriptions.

Table 7-1. DMI Register Address Map

Address Offset	Register Symbol	Register Name	Default Value	Access
00–03h	DMIVCECH	DMI Virtual Channel Enhanced Capability	04010002h	RO
04–07h	DMIPVCCAP1	DMI Port VC Capability Register 1	00000001h	RWO, RO
08–0Bh	DMIPVCCAP2	DMI Port VC Capability Register 2	00000000h	RO
0C–0Dh	DMIPVCCTL	DMI Port VC Control	0000h	RO, RW
10–13h	DMIVC0RCAP	DMI VC0 Resource Capability	00000001h	RO
14–17h	DMIVC0RCTL0	DMI VC0 Resource Control	800000FFh	RO, RW
1A–1Bh	DMIVC0RSTS	DMI VC0 Resource Status	0002h	RO
1C–1Fh	DMIVC1RCAP	DMI VC1 Resource Capability	00008001h	RO
20–23h	DMIVC1RCTL1	DMI VC1 Resource Control	01000000h	RW, RO
26–27h	DMIVC1RSTS	DMI VC1 Resource Status	0002h	RO
84–87h	DMILCAP	DMI Link Capabilities	00012C41h	RO, RWO
88–89h	DMILCTL	DMI Link Control	0000h	RW, RO
8A–8Bh	DMILSTS	DMI Link Status	0001h	RO

7.1 Direct Memory Interface (DMI) Configuration Register Details

7.1.1 DMIVCECH—DMI Virtual Channel Enhanced Capability

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 00–03h
Default Value: 04010002h
Access: RO
Size: 32 bits

This register indicates DMI Virtual Channel capabilities.

Bit	Access & Default	Description
31:20	RO 040h	**Pointer to Next Capability (PNC):** This field contains the offset to the next PCI Express capability structure in the linked list of capabilities (Link Declaration Capability).
19:16	RO 1h	**PCI Express* Virtual Channel Capability Version (PCI EXPRESS*VCCV):** Hardwired to 1 to indicate compliances with the 1.1 version of the PCI Express specification.
15:0	RO 0002h	**Extended Capability ID (ECID):** Value of 0002h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

7.1.2 DMIPVCCAP1—DMI Port VC Capability Register 1

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 04–07h
Default Value: 00000001h
Access: RWO, RO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access & Default	Description
31:7	RO 0000000h	Reserved
6:4	RO 000b	**Low Priority Extended VC Count (LPEVCC):** This field indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3	RO 0b	Reserved
2:0	RWO 001b	**Extended VC Count (EVCC):** This field indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device. The Private Virtual Channel is not included in this count.

7.1.3 DMIPVCCAP2—DMI Port VC Capability Register 2

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 08–0Bh
Default Value: 00000000h
Access: RO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access & Default	Description
31:0	RO 00000000h	Reserved

7.1.4 DMIPVCCTL—DMI Port VC Control

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 0C–0Dh
Default Value: 0000h
Access: RO, RW
Size: 16 bits

Bit	Access & Default	Description
15:4	RO 000h	Reserved
3:1	RW 000b	**VC Arbitration Select (VCAS):** This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. See the PCI express specification for more details.
0	RO 0b	Reserved

7.1.5 DMIVC0RCAP—DMI VC0 Resource Capability

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 10–13h
Default Value: 00000001h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:16	RO 00000h	Reserved
15	RO 0b	**Reject Snoop Transactions (REJSNPT):** 0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:8	RO 00h	Reserved
7:0	RO 01h	**Port Arbitration Capability (PAC):** Having only bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.

7.1.6 DMIVC0RCTL0—DMI VC0 Resource Control

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 14–17h
Default Value: 800000FFh
Access: RO, RW
Size: 32 bits

This register controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access & Default	Description
31	RO 1b	**Virtual Channel 0 Enable (VC0E):** For VC0 this is hardwired to 1 and read only as VC0 can never be disabled.
30:27	RO 0h	Reserved
26:24	RO 000b	**Virtual Channel 0 ID (VC0ID):** Assigns a VC ID to the VC resource. For VC0 this is hardwired to 0 and read only.
23:20	RO 0h	Reserved
19:17	RW 000b	**Port Arbitration Select (PAS):** This field configures the VC resource to provide a particular Port Arbitration service. Valid value for this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource. Because only bit 0 of that field is asserted. This field will always be programmed to '1'.
16:8	RO 000h	Reserved
7:1	RW 7Fh	**Traffic Class / Virtual Channel 0 Map (TCVC0M):** This field indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO 1b	**Traffic Class 0 / Virtual Channel 0 Map (TC0VC0M):** Traffic Class 0 is always routed to VC0.

7.1.7 DMIVC0RSTS—DMI VC0 Resource Status

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 1A–1Bh
Default Value: 0002h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2	RO 0000h	Reserved.
1	RO 1b	**Virtual Channel 0 Negotiation Pending (VC0NP):** This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state. 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling). **BIOS Requirement:** Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0	RO 0b	Reserved

7.1.8 DMIVC1RCAP—DMI VC1 Resource Capability

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 1C–1Fh
Default Value: 00008001h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:16	RO 00000h	Reserved
15	RO 1b	**Reject Snoop Transactions (REJSNPT):** 0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:8	RO 00h	Reserved
7:0	RO 01h	**Port Arbitration Capability (PAC):** Having only bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.

7.1.9 DMIVC1RCTL1—DMI VC1 Resource Control

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 20–23h
Default Value: 01000000h
Access: RW, RO
Size: 32 bits

This register controls the resources associated with PCI Express Virtual Channel 1.

Bit	Access & Default	Description
31	RW 0b	**Virtual Channel 1 Enable (VC1E):** 0 = Virtual Channel is disabled. 1 = Virtual Channel is enabled.
30:27	RO 0h	Reserved
26:24	RW 001b	**Virtual Channel 1 ID (VC1ID):** This field assigns a VC ID to the VC resource. Assigned value must be non-zero. This field can not be modified when the VC is already enabled.
23:20	RO 0h	Reserved
19:17	RW 000b	**Port Arbitration Select (PAS):** This field configures the VC resource to provide a particular Port Arbitration service. Valid value for this field is a number corresponding to one of the asserted bits in the Port Arbitration Capability field of the VC resource.
16:8	RO 000h	Reserved
7:1	RW 00h	**Traffic Class / Virtual Channel 1 Map (TCVC1M):** This field indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO 0b	**Traffic Class 0 / Virtual Channel 1 Map (TC0VC1M):** Traffic Class 0 is always routed to VC0.

7.1.10 DMIVC1RSTS—DMI VC1 Resource Status

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 26–27h
Default Value: 0002h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2	RO 0000h	Reserved
1	RO 1b	**Virtual Channel 1 Negotiation Pending (VC1NP):** 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling).
0	RO 0b	Reserved

7.1.11 DMILCAP—DMI Link Capabilities

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 84–87h
Default Value: 00012C41h
Access: RO, RWO
Size: 32 bits

This register indicates DMI specific capabilities.

Bit	Access & Default	Description
31:18	RO 0000h	Reserved
17:15	RWO 010b	**L1 Exit Latency (L1SELAT):** This field indicates the length of time this Port requires to complete the transition from L1 to L0. 010b = 2 us to less than 4 us.
14:12	RWO 010b	**L0s Exit Latency (L0SELAT):** This field indicates the length of time this Port requires to complete the transition from L0s to L0. 010 = 128 ns to less than 256 ns
11:10	RO 11b	**Active State Link PM Support (ASLPMS):** L0s & L1 entry supported.
9:4	RO 04h	**Max Link Width (MLW):** This field indicates the maximum number of lanes supported for this link.
3:0	RO 1h	**Max Link Speed (MLS):** Hardwired to indicate 2.5 Gb/s.

7.1.12 DMILCTL—DMI Link Control

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 88–89h
Default Value: 0000h
Access: RW, RO
Size: 16 bits

This register allows control of DMI.

Bit	Access & Default	Description
15:8	RO 00h	Reserved
7	RW 0b	**Extended Synch (EXTSYNC):** 0 = Standard Fast Training Sequence (FTS). 1 = Forces the transmission of additional ordered sets when exiting the L0s state and when in the Recovery state.
6:3	RO 0h	Reserved
2	RW 0b	**Far-End Digital Loopback (FEDLB):**
1:0	RW 00b	**Active State Power Management Support (ASPMS):** This field controls the level of active state power management supported on the given link. 00 = Disabled 01 = L0s Entry Supported 10 = Reserved 11 = L0s and L1 Entry Supported

7.1.13 DMILSTS—DMI Link Status

B/D/F/Type: 0/0/0/DMIBAR
Address Offset: 8A–8Bh
Default Value: 0001h
Access: RO
Size: 16 bits

This register indicates DMI status.

Bit	Access & Default	Description
15:10	RO 00h	Reserved and Zero for future R/WC/S implementations. Software must use 0 for writes to these bits.
9:4	RO 00h	**Negotiated Width (NWID):** This field indicates negotiated link width. This field is valid only when the link is in the L0, L0s, or L1 states (after link width negotiation is successfully completed). 04h = X4 All other encodings are reserved.
3:0	RO 1h	**Negotiated Speed (NSPD):** This field indicates negotiated link speed. 1h = 2.5 Gb/s All other encodings are reserved.

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8 Integrated Graphics Device Registers (D2:F0,F1) (Intel® 82Q35, 82Q33, 82G33 GMCH Only)

The Integrated Graphics Device (IGD) registers are located in Device 2 (D0), Function 0 (F0) and Function 1 (F1). This chapter provides the descriptions for these registers. Section 8.1 provides the register descriptions for Device 2, Function 0. Section 8.2 provides the register descriptions for Device 2, Function 1.

8.1 Integrated Graphics Register Details (D2:F0)

Device 2, Function 0 contains registers for the internal graphics functions. Table 8-1 lists the PCI configuration registers in order of ascending offset address.

Function 0 can be VGA compatible or not, this is selected through bit 1 of GGC register (Device 0, offset 52h).

Note: The following sections describe Device 2 PCI configuration registers only.

Table 8-1. Integrated Graphics Device Register Address Map (D2:F0)

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID2	Vendor Identification	8086h	RO
02–03h	DID	Device Identification	29C2h	RO
04–05h	PCICMD2	PCI Command	0000h	RO, RW
06–07h	PCISTS2	PCI Status	0090h	RO
08h	RID2	Revision Identification	00h	RO
09–0Bh	CC	Class Code	030000h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	MLT2	Master Latency Timer	00h	RO
0Eh	HDR2	Header Type	80h	RO
10–13h	MMADR	Memory Mapped Range Address	00000000h	RO, RW
2C–2Dh	SVID2	Subsystem Vendor Identification	0000h	RWO
2E–2Fh	SID2	Subsystem Identification	0000h	RWO

Address Offset	Register Symbol	Register Name	Default Value	Access
30–33h	ROMADR	Video BIOS ROM Base Address	00000000h	RO
34h	CAPPOINT	Capabilities Pointer	90h	RO
3Eh	MINGNT	Minimum Grant	00h	RO
3Fh	MAXLAT	Maximum Latency	00h	RO
40–50h	CAPID0	Capability Identifier	000000000 000000001 000000000 10B0009h	RO
52–53h	MGGC	GMCH Graphics Control Register	0030h	RO
54–57h	DEVEN	Device Enable	000003DBh	RO
58–5Bh	SSRW	Software Scratch Read Write	00000000h	RW
5C–5Fh	BSM	Base of Stolen Memory	07800000h	RO
60–61h	HSRW	Hardware Scratch Read Write	0000h	RW
C0h	GDRST	Graphics Debug Reset	00h	RO, RW/L
D0–D1h	PMCAPID	Power Management Capabilities ID	0001h	RWO, RO
D2–D3h	PMCAP	Power Management Capabilities	0022h	RO
D4–D5h	PMCS	Power Management Control/Status	0000h	RO, RW
E0–E1h	SWSMI	Software SMI	0000h	RW
E4–E7h	ASLE	System Display Event Register	00000000h	RW
FC–FFh	ASLS	ASL Storage	00000000h	RW

8.1.1 VID2—Vendor Identification

B/D/F/Type: 0/2/0/PCI
Address Offset: 00–01h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 8086h	**Vendor Identification Number (VID):** PCI standard identification for Intel.

8.1.2 DID—Device Identification

B/D/F/Type: 0/2/0/PCI
Address Offset: 02–03h
Default Value: 29C2h
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 29C2h	**Device Identification Number (DID):** This is a 16 bit value assigned to the GMCH Graphic device.

8.1.3 PCICMD2—PCI Command

B/D/F/Type: 0/2/0/PCI
Address Offset: 04–05h
Default Value: 0000h
Access: RO, RW
Size: 16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.

Bit	Access & Default	Description
15:11	RO 00h	Reserved
10	RW 0b	**Interrupt Disable (INTDIS):** This bit disables the device from asserting INTx#. 0 = Enable the assertion of this device's INTx# signal. 1 = Disable the assertion of this device's INTx# signal. DO_INTx messages will not be sent to DMI.
9	RO 0b	**Fast Back-to-Back (FB2B):** Not Implemented. Hardwired to 0.
8	RO 0b	**SERR Enable (SERRE):** Not Implemented. Hardwired to 0.
7	RO 0b	**Address/Data Stepping Enable (ADSTEP):** Not Implemented. Hardwired to 0.
6	RO 0b	**Parity Error Enable (PERRE):** Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.

Bit	Access & Default	Description
5	RO 0b	**Video Palette Snooping (VPS):** This bit is hardwired to 0 to disable snooping.
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	RO 0b	**Special Cycle Enable (SCE):** This bit is hardwired to 0. The IGD ignores Special cycles.
2	RW 0b	**Bus Master Enable (BME):** This bit controls the IGD's response to bus master accesses. 0 = Disable IGD bus mastering. 1 = Enable the IGD to function as a PCI compliant master.
1	RW 0b	**Memory Access Enable (MAE):** This bit controls the IGD's response to memory space accesses. 0 = Disable. 1 = Enable.
0	RW 0b	**I/O Access Enable (IOAE):** This bit controls the IGD's response to I/O space accesses. 0 = Disable. 1 = Enable.

8.1.4 PCISTS2—PCI Status

B/D/F/Type: 0/2/0/PCI
Address Offset: 06–07h
Default Value: 0090h
Access: RO
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Since the IGD does not detect parity, this bit is always hardwired to 0.
14	RO 0b	**Signaled System Error (SSE):** The IGD never asserts SERR#, therefore this bit is hardwired to 0.
13	RO 0b	**Received Master Abort Status (RMAS):** The IGD never gets a Master Abort, therefore this bit is hardwired to 0.
12	RO 0b	**Received Target Abort Status (RTAS):** The IGD never gets a Target Abort, therefore this bit is hardwired to 0.
11	RO 0b	**Signaled Target Abort Status (STAS):** Hardwired to 0. The IGD does not use target abort semantics.
10:9	RO 00b	**DEVSEL Timing (DEVT):** N/A. These bits are hardwired to "00".
8	RO 0b	**Master Data Parity Error Detected (DPD):** Since Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection), this bit is hardwired to 0.
7	RO 1b	**Fast Back-to-Back (FB2B):** Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.
6	RO 0b	**User Defined Format (UDF):** Hardwired to 0.
5	RO 0b	**66 MHz PCI Capable (66C):** N/A - Hardwired to 0.
4	RO 1b	**Capability List (CLIST):** This bit is set to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.
3	RO 0b	**Interrupt Status (INTSTS):** This bit reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the devices INTx# signal be asserted.
2:0	RO 000b	Reserved

8.1.5 RID2—Revision Identification

B/D/F/Type: 0/2/0/PCI
Address Offset: 08h
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the revision number for Device #2 Functions 0 and 1.

Bit	Access & Default	Description
7:0	RO 00h	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the GMCH Device 2. Refer to the *Intel® 3 Series Express Chipset Family Specification Update* for the value of the Revision ID register.

8.1.6 CC—Class Code

B/D/F/Type: 0/2/0/PCI
Address Offset: 09–0Bh
Default Value: 030000h
Access: RO
Size: 24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Access & Default	Description
23:16	RO 03h	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the GMCH. This code has the value 03h, indicating a Display Controller.
15:8	RO 00h	**Sub-Class Code (SUBCC):** Value will be determined based on Device 0 GGC register, GMS and IVD fields. 00h = VGA compatible 80h = Non VGA (GMS = "0000" or IVD = "1")
7:0	RO 00h	**Programming Interface (PI):** 00h = Hardwired as a Display controller.

8.1.7 CLS—Cache Line Size

B/D/F/Type: 0/2/0/PCI
Address Offset: 0Ch
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support this register as a PCI slave.

Bit	Access & Default	Description
7:0	RO 00h	**Cache Line Size (CLS):** This field is hardwired to 0s. The IGD as a PCI compliant master does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size.

8.1.8 MLT2—Master Latency Timer

B/D/F/Type: 0/2/0/PCI
Address Offset: 0Dh
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

Bit	Access & Default	Description
7:0	RO 00h	**Master Latency Timer Count Value (MLTCV):** Hardwired to 0s.

8.1.9 HDR2—Header Type

B/D/F/Type: 0/2/0/PCI
Address Offset: 0Eh
Default Value: 80h
Access: RO
Size: 8 bits

This register contains the Header Type of the IGD.

Bit	Access & Default	Description
7	RO 1b	**Multi Function Status (MFUNC):** Indicates if the device is a Multi-Function Device. The Value of this register is determined by Device #0, offset 54h, DEVEN[4]. If Device 0 DEVEN[4] is set, the MFUNC bit is also set.
6:0	RO 00h	**Header Code (H):** This is a 7-bit value that indicates the Header Code for the IGD. This code has the value 00h, indicating a type 0 configuration space format.

8.1.10 GMADR—Graphics Memory Range Address

B/D/F/Type: 0/2/0/PCI
Address Offset: 18–1Bh
Default Value: 00000008h
Access: RW, RO, RW/L
Size: 32 bits

IGD graphics memory base address is specified in this register.

Bit	Access & Default	Description
31:29	RW 000b	**Memory Base Address (MBA):** Set by the OS, these bits correspond to address signals 31:29.
28	RW/L 0b	**512MB Address Mask (512ADMSK):** This Bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO), depending on the value of MSAC[1:0]. See MSAC (D2:F0, offset 62h) for details.
27	RW/L 0b	**256 MB Address Mask (256ADMSK):** This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO), depending on the value of MSAC[1:0]. See MSAC (D2:F0, offset 62h) for details.
26:4	RO 000000h	**Address Mask (ADM):** Hardwired to 0s to indicate at least 128 MB address range.
3	RO 1b	**Prefetchable Memory (PREFMEM):** Hardwired to 1 to enable prefetching.
2:1	RO 00b	**Memory Type (MEMTYP):** Hardwired to 0 to indicate 32-bit address.
0	RO 0b	**Memory/IO Space (MIOS):** Hardwired to 0 to indicate memory space.

8.1.11 IOBAR—I/O Base Address

B/D/F/Type: 0/2/0/PCI
Address Offset: 14–17h
Default Value: 00000001h
Access: RO, RW
Size: 32 bits

This register provides the Base offset of the I/O registers within Device 2. Bits 15:3 are programmable allowing the I/O Base to be located anywhere in 16 bit I/O Address Space. Bits 2:1 are fixed and return zero; bit 0 is hardwired to a one indicating that 8 bytes of I/O space are decoded. Access to the 8Bs of I/O space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed in PM states D1–D3 or if I/O Enable is clear or if Device 2 is turned off or if Internal graphics is disabled thru the fuse or fuse override mechanisms.

Note that access to this IO BAR is independent of VGA functionality within Device 2. Also note that this mechanism is available only through function 0 of Device 2 and is not duplicated in function 1.

If accesses to this IO bar is allowed then the GMCH claims all 8, 16 or 32 bit I/O cycles from the processor that falls within the 8B claimed.

Bit	Access & Default	Description
31:16	RO 0000h	Reserved
15:3	RW 0000h	**IO Base Address (IOBASE):** Set by the OS, these bits correspond to address signals 15:3.
2:1	RO 00b	**Memory Type (MEMTYPE):** Hardwired to 0s to indicate 32-bit address.
0	RO 1b	**Memory/IO Space (MIOS):** Hardwired to 1 to indicate I/O space.

8.1.12 SVID2—Subsystem Vendor Identification

B/D/F/Type: 0/2/0/PCI
Address Offset: 2C–2Dh
Default Value: 0000h
Access: RWO
Size: 16 bits

Bit	Access & Default	Description
15:0	RWO 0000h	**Subsystem Vendor ID (SUBVID):** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This register can only be cleared by a Reset.

8.1.13 SID2—Subsystem Identification

B/D/F/Type: 0/2/0/PCI
Address Offset: 2E–2Fh
Default Value: 0000h
Access: RWO
Size: 16 bits

Bit	Access & Default	Description
15:0	RWO 0000h	**Subsystem Identification (SUBID):** This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This register can only be cleared by a Reset.

8.1.14 ROMADR—Video BIOS ROM Base Address

B/D/F/Type: 0/2/0/PCI
Address Offset: 30–33h
Default Value: 00000000h
Access: RO
Size: 32 bits

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0s.

Bit	Access & Default	Description
31:18	RO 0000h	**ROM Base Address (RBA):** Hardwired to 0s.
17:11	RO 00h	**Address Mask (ADMSK):** Hardwired to 0s to indicate 256 KB address range.
10:1	RO 000h	Reserved**.** Hardwired to 0s.
0	RO 0b	**ROM BIOS Enable (RBE):** 0 = ROM not accessible.

8.1.15 CAPPOINT—Capabilities Pointer

B/D/F/Type: 0/2/0/PCI
Address Offset: 34h
Default Value: 90h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 90h	**Capabilities Pointer Value (CPV):** This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List, the MSI Capabilities ID registers at address 90h or the Power Management capability at D0h. This value is determined by the configuration in CAPL[0].

8.1.16 INTRLINE—Interrupt Line

B/D/F/Type: 0/2/0/PCI
Address Offset: 3Ch
Default Value: 00h
Access: RW
Size: 8 bits

Bit	Access & Default	Description
7:0	RW 00h	**Interrupt Connection (INTCON):** This field is used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates to which input of the system interrupt controller the device's interrupt pin is connected.

8.1.17 INTRPIN—Interrupt Pin

B/D/F/Type: 0/2/0/PCI
Address Offset: 3Dh
Default Value: 01h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 01h	**Interrupt Pin (INTPIN):** As a single function device, the IGD specifies INTA# as its interrupt pin. 01h = INTA#.

8.1.18 MINGNT—Minimum Grant

B/D/F/Type: 0/2/0/PCI
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Minimum Grant Value (MGV):** The IGD does not burst as a PCI compliant master.

8.1.19 MAXLAT—Maximum Latency

B/D/F/Type: 0/2/0/PCI
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Maximum Latency Value (MLV):** The IGD has no specific requirements for how often it needs to access the PCI bus.

8.1.20 CAPID0—Capability Identifier

B/D/F/Type: 0/2/0/PCI
Address Offset: 40–50h
Default Value: 00000000000000000100000000010B0009h
Access: RO
Size: 136 bits
BIOS Optimal Default 000000000000h

This register control of bits in this register are only required for customer visible SKU differentiation.

Bit	Access & Default	Description
135:28	RO 0s	Reserved
27:24	RO 1h	**CAPID Version (CAPIDV):** This field has the value 0001b to identify the first revision of the CAPID register definition.
23:16	RO 0bh	**CAPID Length (CAPIDL):** This field has the value 0bh to indicate the structure length (11 bytes).
15:8	RO 00h	**Next Capability Pointer (NCP):** This field is hardwired to 00h indicating the end of the capabilities linked list.
7:0	RO 09h	**Capability Identifier (CAP_ID):** This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

8.1.21 MGGC—GMCH Graphics Control Register

B/D/F/Type: 0/2/0/PCI
Address Offset: 52–53h
Default Value: 0030h
Access: RO
Size: 16 bits

All the Bits in this register are Intel® TXT lockable.

Bit	Access & Default	Description
15:10	RO 00h	Reserved
9:8	RO 0h	**GTT Graphics Memory Size (GGMS):** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. 00 = No memory pre-allocated. GTT cycles (Memory and I/O) are not claimed. 01 = No VT mode, 1 MB of memory pre-allocated for GTT. 10 = VT mode, 2 MB of memory pre-allocated for GTT. 11 = Reserved **Note:** This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.

Bit	Access & Default	Description
7:4	RO 0011b	**Graphics Mode Select (GMS):** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. 0000 = No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Memory and I/O), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80. 0001 = DVMT (UMA) mode, 1 MB of memory pre-allocated for frame buffer. 0010 = DVMT (UMA) mode, 4 MB of memory pre-allocated for frame buffer. 0011 = DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer. 0100 = DVMT (UMA) mode, 16 MB of memory pre-allocated for frame buffer. 0101 = DVMT (UMA) mode, 32 MB of memory pre-allocated for frame buffer. 0110 = DVMT (UMA) mode, 48 MB of memory pre-allocated for frame buffer. 0111 = DVMT (UMA) mode, 64 MB of memory pre-allocated for frame buffer. 1000 = DVMT (UMA) mode, 128 MB of memory pre-allocated for frame buffer. 1001 = DVMT (UMA) mode, 256 MB of memory pre-allocated for frame buffer. **Note:** This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set. **BIOS Requirement:** BIOS must not set this field to 000 if IVD (bit 1 of this register) is 0.
3:0	RO 0000b	Reserved

8.1.22 DEVEN—Device Enable

B/D/F/Type: 0/2/0/PCI
Address Offset: 54–57h
Default Value: 000003DBh
Access: RO
Size: 32 bits

This register allows for enabling/disabling of PCI devices and functions that are within the GMCH. The table below the bit definitions describes the behavior of all combinations of transactions to devices controlled by this register. All the bits in this register are Intel® TXT Lockable.

Bit	Access & Default	Description
31:15	RO 00000h	Reserved
14	RO 0b	**Chap Enable (D7EN):** 0 = Bus 0, Device 7 is disabled and not visible. 1 = Bus 0, Device 7 is enabled and visible. Non-production BIOS code should provide a setup option to enable Bus 0, Device 7. When enabled, Bus 0, Device 7 must be initialized in accordance to standard PCI device initialization procedures.
13:10	RO 0b	Reserved
9	RO 1b	**EP Function 3 (D3F3EN):** 0 = Bus 0, Device 3, Function 3 is disabled and hidden 1 = Bus 0, Device 3, Function 3 is enabled and visible If Device 3, Function 0 is disabled and hidden, then Device 3, Function 3 is also disabled and hidden independent of the state of this bit.
8	RO 1b	**EP Function 2 (D3F2EN):** 0 = Bus 0, Device 3, Function 2 is disabled and hidden 1 = Bus 0, Device 3, Function 2 is enabled and visible If Device 3, Function 0 is disabled and hidden, then Device 3, Function 2 is also disabled and hidden independent of the state of this bit.
7	RO 1b	**EP Function 1 (D3F1EN):** 0 = Bus 0, Device 3, Function 1 is disabled and hidden 1 = Bus 0, Device 3, Function 1 is enabled and visible. If this GMCH does not have ME capability (CAPID0[??] = 1), then Device 3, Function 1 is disabled and hidden independent of the state of this bit.

Bit	Access & Default	Description
6	RO 1b	**EP Function 0 (D3F0EN):** 0 = Bus 0, Device 3, Function 0 is disabled and hidden 1 = Bus 0, Device 3, Function 0 is enabled and visible. If this GMCH does not have ME capability (CAPID0[??] = 1), then Device 3, Function 0 is disabled and hidden independent of the state of this bit.
5	RO 0b	Reserved
4	RO 1b	**Internal Graphics Engine Function 1 (D2F1EN):** 0 = Bus 0, Device 2, Function 1 is disabled and hidden 1 = Bus 0, Device 2, Function 1 is enabled and visible If Device 2, Function 0 is disabled and hidden, then Device 2, Function 1 is also disabled and hidden independent of the state of this bit. If this component is not capable of Dual Independent Display (CAPID0[78] = 1), then this bit is hardwired to 0b to hide Device 2, Function 1.
3	RO 1b	**Internal Graphics Engine Function 0 (D2F0EN):** 0 = Bus 0, Device 2, Function 0 is disabled and hidden 1 = Bus 0, Device 2, Function 0 is enabled and visible If this GMCH does not have internal graphics capability (CAPID0[46] = 1), then Device 2, Function 0 is disabled and hidden independent of the state of this bit.
2	RO 0b	Reserved
1	RO 1b	**PCI Express Port (D1EN):** 0 = Bus 0, Device 1, Function 0 is disabled and hidden. 1 = Bus 0, Device 1, Function 0 is enabled and visible. Default value is determined by the device capabilities (see CAPID0 [44]), SDVO Presence hardware strap and the SDVO/PCIe Concurrent hardware strap. Device 1 is Disabled on Reset if the SDVO Presence strap was sampled high, and the SDVO/PCIe Concurrent strap was sampled low at the last assertion of PWROK, and is enabled by default otherwise.
0	RO 1b	**Host Bridge (D0EN):** Bus 0, Device 0, Function 0 may not be disabled and is therefore hardwired to 1.

8.1.23 SSRW—Software Scratch Read Write

B/D/F/Type: 0/2/0/PCI
Address Offset: 58–5Bh
Default Value: 00000000h
Access: RW
Size: 32 bits

Bit	Access & Default	Description
31:0	RW 00000000h	Reserved

8.1.24 BSM—Base of Stolen Memory

B/D/F/Type: 0/2/0/PCI
Address Offset: 5C–5Fh
Default Value: 07800000h
Access: RO
Size: 32 bits

Graphics Stolen Memory and TSEG are within DRAM space defined under TOLUD. From the top of low used DRAM, GMCH claims 1 to 64 MBs of DRAM for internal graphics if enabled.

The base of stolen memory will always be below 4 GB. This is required to prevent aliasing between stolen range and the reclaim region.

Bit	Access & Default	Description
31:20	RO 078h	**Base of Stolen Memory (BSM):** This register contains bits 31:20 of the base address of stolen DRAM memory. The host interface determines the base of Graphics Stolen memory by subtracting the graphics stolen memory size from TOLUD. See Device 0 TOLUD for more explanation.
19:0	RO 00000h	Reserved

8.1.25 HSRW—Hardware Scratch Read Write

B/D/F/Type: 0/2/0/PCI
Address Offset: 60–61h
Default Value: 0000h
Access: RW
Size: 16 bits

Bit	Access & Default	Description
15:0	RW 0000h	Reserved

8.1.26 MC—Message Control

B/D/F/Type: 0/2/0/PCI
Address Offset: 92–93h
Default Value: 0000h
Access: RO, RW
Size: 16 bits

System software can modify bits in this register, but the device is prohibited from doing so. If the device writes the same message multiple times, only one of those messages is ensured to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

Bit	Access & Default	Description
15:8	RO 00h	Reserved
7	RO 0b	**64 Bit Capable (64BCAP):** Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message address register and is incapable of generating a 64-bit memory address. This may need to change in future implementations when addressable system memory exceeds the 32b / 4 GB limit.
6:4	RW 000b	**Multiple Message Enable (MME):** System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. The encoding is the same as for the MMC field (Bits 3:1).
3:1	RO 000b	**Multiple Message Capable (MMC):** System Software reads this field to determine the number of messages being requested by this device. 000 = 1 All of the following are reserved in this implementation 001 = 2 010 = 4 011 = 8 100 = 16 101 = 32 110 = Reserved 111 = Reserved
0	RW 0b	**MSI Enable (MSIEN):** This bit controls the ability of this device to generate MSIs.

8.1.27 MA—Message Address

B/D/F/Type: 0/2/0/PCI
Address Offset: 94–97h
Default Value: 00000000h
Access: RW, RO
Size: 32 bits

Bit	Access & Default	Description
31:2	RW 00000000h	**Message Address (MESSADD):** Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
1:0	RO 00b	**Force DWord Align (FDWORD):** Hardwired to 0 so that addresses assigned by system software are always aligned on a DWord address boundary.

8.1.28 MD—Message Data

B/D/F/Type: 0/2/0/PCI
Address Offset: 98–99h
Default Value: 0000h
Access: RW
Size: 16 bits

Bit	Access & Default	Description
15:0	RW 0000h	**Message Data (MESSDATA):** Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.

8.1.29 GDRST—Graphics Debug Reset

B/D/F/Type: 0/2/0/PCI
Address Offset: C0h
Default Value: 00h
Access: RO, RW
Size: 8 bits

Bit	Access & Default	Description
7:4	RO 0h	Reserved
3:2	RW 00b	**Graphics Reset Domain (GRDOM):** 00 = Full Graphics Reset will be performed (both render and display clock domain resets asserted 01 = Reserved (Invalid Programming) 10 = Reserved (Invalid Programming) 11 = Reserved (Invalid Programming)
1	RO 0b	Reserved
0	RW 0b	**Graphics Reset Enable (GR):** Setting this bit asserts graphics-only reset. The clock domains to be reset are determined by GRDOM. Hardware resets this bit when the reset is complete. Setting this bit without waiting for it to clear, is undefined behavior. Once this bit is set to a 1, all GFX core MMIO registers are returned to power on default state. All Ring buffer pointers are reset, command stream fetches are dropped and ongoing render pipeline processing is halted, state machines and State Variables returned to power on default state. If the Display is reset, all display engines are halted (garbage on screen). VGA memory is not available, Store DWords and interrupts are not assured to be completed. Device 2 I/O registers are not available. When issuing the graphics reset, disable the cursor, display, and overlay engines using the MMIO registers. Wait 1 us. Issue the graphics reset by setting this bit to 1. Device 2 Configuration registers continue to be available while graphics reset is asserted. This bit is hardware auto-clear.

8.1.30 PMCAPID—Power Management Capabilities ID

B/D/F/Type: 0/2/0/PCI
Address Offset: D0–D1h
Default Value: 0001h
Access: RWO, RO
Size: 16 bits

Bit	Access & Default	Description
15:8	RWO 00h	**Next Capability Pointer (NEXT_PTR):** This field contains a pointer to the next item in the capabilities list. BIOS is responsible for writing this to the FLR Capability when applicable.
7:0	RO 01h	**Capability Identifier (CAP_ID):** SIG defines this ID is 01h for power management.

8.1.31 PMCAP—Power Management Capabilities

B/D/F/Type: 0/2/0/PCI
Address Offset: D2–D3h
Default Value: 0022h
Access: RO
Size: 16 bits

This register is a Mirror of Function 0 with the same read/write attributes. The hardware implements a single physical register common to both functions 0 and 1.

Bit	Access & Default	Description
15:11	RO 00h	**PME Support (PMES):** This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10	RO 0b	**D2 Support (D2):** The D2 power management state is not supported. This bit is hardwired to 0.
9	RO 0b	**D1 Support (D1):** Hardwired to 0 to indicate that the D1 power management state is not supported.
8:6	RO 000b	Reserved
5	RO 1b	**Device Specific Initialization (DSI):** Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
4	RO 0b	Reserved
3	RO 0b	**PME Clock (PMECLK):** Hardwired to 0 to indicate IGD does not support PME# generation.
2:0	RO 010b	**Version (VER):** Hardwired to 010b to indicate that there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the PCI Power Management Interface Specification.

8.1.32 PMCS—Power Management Control/Status

B/D/F/Type: 0/2/0/PCI
Address Offset: D4–D5h
Default Value: 0000h
Access: RO, RW
Size: 16 bits

Bit	Access & Default	Description
15	RO 0b	**PME Status (PMESTS):** This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).
14:13	RO 00b	**Data Scale (DSCALE):** The IGD does not support data register. This bit always returns 00 when read, write operations have no effect.
12:9	RO 0h	**Data Select (DSEL):** The IGD does not support data register. This bit always returns 0h when read, write operations have no effect.
8	RO 0b	**PME Enable (PME_EN):** This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2	RO 00h	Reserved
1:0	RW 00b	**Power State (PWRSTAT):** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values. 00 = D0 (Default) 01 = D1 (Not Supported) 10 = D2 (Not Supported) 11 = D3

8.1.33 SWSMI—Software SMI

B/D/F/Type: 0/2/0/PCI
Address Offset: E0–E1h
Default Value: 0000h
Access: RW
Size: 16 bits

As long as there is the potential that DVO port legacy drivers exist which expect this register at this address, D2, F0 address E0h–E1h must be reserved for this register.

Bit	Access & Default	Description
15:8	RW 00h	**Software Scratch Bits (SWSB):**
7:1	RW 00h	**Software Flag (SWF):** Used to indicate caller and SMI function desired, as well as return result.
0	RW 0b	**GMCH Software SMI Event (GSSMIE):** When Set this bit will trigger an SMI. Software must write a "0" to clear this bit.

8.2 IGD Configuration Register Details (D2:F1)

The Integrated Graphics Device registers are located in Device 2 (D2), Function 0 (F0) and Function 1 (F1). This section provides the descriptions for the D2:F1 registers. Table 8-2 provides an address map of the D2:F1registers listed in ascending order by address offset. Detailed bit descriptions follow the table.

Table 8-2. Integrated Graphics Device Register Address Map (D2:F1)

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID2	Vendor Identification	8086h	RO
02–03h	DID2	Device Identification	29C3h	RO
04–05h	PCICMD2	PCI Command	0000h	RO, RW
06–07h	PCISTS2	PCI Status	0090h	RO
08h	RID2	Revision Identification	00h	RO
09–0Bh	CC	Class Code Register	038000h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	MLT2	Master Latency Timer	00h	RO
0Eh	HDR2	Header Type	80h	RO
10–13h	MMADR	Memory Mapped Range Address	00000000h	RW, RO
2C–2Dh	SVID2	Subsystem Vendor Identification	0000h	RO
2E–2Fh	SID2	Subsystem Identification	0000h	RO
30–33h	ROMADR	Video BIOS ROM Base Address	00000000h	RO
34h	CAPPOINT	Capabilities Pointer	D0h	RO
3Eh	MINGNT	Minimum Grant	00h	RO
3Fh	MAXLAT	Maximum Latency	00h	RO
40–50h	CAPID0	Mirror of Dev0 Capability Identifier	0000000000 0000000100 000000010 B0009h	RO
52–53h	MGGC	Mirror of Dev 0 GMCH Graphics Control Register	0030h	RO
54–57h	DEVEN	Device Enable	000003DBh	RO
58–5Bh	SSRW	Mirror of Fun 0 Software Scratch Read Write	00000000h	RO
5C–5Fh	BSM	Mirror of Func0 Base of Stolen Memory	07800000h	RO
60–61h	HSRW	Mirror of Dev2 Func0 Hardware Scratch Read Write	0000h	RO

Address Offset	Register Symbol	Register Name	Default Value	Access
62h	MSAC	Mirror of Dev2 Func0 Multi Size Aperture Control	02h	RO
C0h	GDRST	Mirror of Dev2 Func0 Graphics Reset	00h	RO
C1–C3h	MI_GFX_CG_DIS	Mirror of Fun 0 MI GFX Unit Level Clock Ungating	000000h	RO
C4–C7h	RSVD	Reserved	00000000h	RO
C8h	RSVD	Reserved	00h	RO
CA–CBh	RSVD	Reserved	0000h	RO
CC–CDh	GCDGMBUS	Mirror of Dev2 Func0 Graphics Clock Frequency Register for GMBUS unit	0000h	RO
D0–D1h	PMCAPID	Mirror of Fun 0 Power Management Capabilities ID	0001h	RO
D2–D3h	PMCAP	Mirror of Fun 0 Power Management Capabilities	0022h	RO
D4–D5h	PMCS	Power Management Control/Status	0000h	RO, RW
D8–DBh	RSVD	Reserved	00000000h	RO
E0–E1h	SWSMI	Mirror of Func0 Software SMI	0000h	RO
E4–E7h	ASLE	Mirror of Dev2 Func0 System Display Event Register	00000000h	RO
F0–F3h	GCFGC	Mirror of Dev2 Func0 Graphics Clock Frequency and Gating Control	00000000h	RO/P, RO
F4–F7h	RSVD	Mirror of Fun 0 Reserved for LBB-Legacy Backlight Brightness	00000000h	RO
FC–FFh	ASLS	ASL Storage	00000000h	RW

8.2.1 VID2—Vendor Identification

B/D/F/Type: 0/2/1/PCI
Address Offset: 00–01h
Default Value: 8086h
Access: RO
Size: 16 bits

This register, combined with the Device Identification register, uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 8086h	**Vendor Identification Number (VID):** PCI standard identification for Intel.

8.2.2 DID2—Device Identification

B/D/F/Type: 0/2/1/PCI
Address Offset: 02–03h
Default Value: 29C3h
Access: RO
Size: 16 bits

This register is unique in Function 1 (the Function 0 DID is separate). This difference in Device ID is necessary for allowing distinct Plug and Play enumeration of function 1 when both function 0 and function 1 have the same class code.

Bit	Access & Default	Description
15:0	RO 29C3h	**Device Identification Number (DID):** This is a 16 bit value assigned to the GMCH Graphic device Function 1

8.2.3 PCICMD2—PCI Command

B/D/F/Type: 0/2/1/PCI
Address Offset: 04–05h
Default Value: 0000h
Access: RO, RW
Size: 16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.

Bit	Access & Default	Description
15:10	RO 0s	Reserved
9	RO 0b	**Fast Back-to-Back (FB2B):** Not Implemented. Hardwired to 0.
8	RO 0b	**SERR Enable (SERRE):** Not Implemented. Hardwired to 0.
7	RO 0b	**Address/Data Stepping Enable (ADSTEP):** Not Implemented. Hardwired to 0.
6	RO 0b	**Parity Error Enable (PERRE):** Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	RO 0b	**VGA Palette Snoop Enable (VGASNOOP):** This bit is hardwired to 0 to disable snooping.
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	RO 0b	**Special Cycle Enable (SCE):** This bit is hardwired to 0. The IGD ignores Special cycles.
2	RW 0b	**Bus Master Enable (BME):** 0 = Disable IGD bus mastering. 1 = Enable the IGD to function as a PCI compliant master.
1	RW 0b	**Memory Access Enable (MAE):** This bit controls the IGD's response to memory space accesses. 0 = Disable. 1 = Enable.
0	RW 0b	**I/O Access Enable (IOAE):** This bit controls the IGD's response to I/O space accesses. 0 = Disable. 1 = Enable.

8.2.4 PCISTS2—PCI Status

B/D/F/Type: 0/2/1/PCI
Address Offset: 06–07h
Default Value: 0090h
Access: RO
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Since the IGD does not detect parity, this bit is always hardwired to 0.
14	RO 0b	**Signaled System Error (SSE):** The IGD never asserts SERR#, therefore this bit is hardwired to 0.
13	RO 0b	**Received Master Abort Status (RMAS):** The IGD never gets a Master Abort, therefore this bit is hardwired to 0.
12	RO 0b	**Received Target Abort Status (RTAS):** The IGD never gets a Target Abort, therefore this bit is hardwired to 0.
11	RO 0b	**Signaled Target Abort Status (STAS):** Hardwired to 0. The IGD does not use target abort semantics.
10:9	RO 00b	**DEVSEL Timing (DEVT):** N/A. These bits are hardwired to "00".
8	RO 0b	**Master Data Parity Error Detected (DPD):** Since Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection), this bit is hardwired to 0.
7	RO 1b	**Fast Back-to-Back (FB2B):** Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.
6	RO 0b	**User Defined Format (UDF):** Hardwired to 0.
5	RO 0b	**66 MHz PCI Capable (66C):** N/A - Hardwired to 0.
4	RO 1b	**Capability List (CLIST):** This bit is set to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.
3	RO 0b	**Interrupt Status (INTSTS):** Hardwired to 0.
2:0	RO 000b	Reserved

8.2.5 RID2—Revision Identification

B/D/F/Type: 0/2/1/PCI
Address Offset: 08h
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the revision number for Device 2 Functions 0 and 1.

Bit	Access & Default	Description
7:0	RO 00h	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the GMCH Device 2. Refer to the *Intel® 3 Series Express Chipset Family Specification Update* for the value of the Revision ID register.

8.2.6 CC—Class Code Register

B/D/F/Type: 0/2/1/PCI
Address Offset: 09–0Bh
Default Value: 038000h
Access: RO
Size: 24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Access & Default	Description
23:16	RO 03h	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the GMCH. This code has the value 03h, indicating a Display Controller.
15:8	RO 80h	**Sub-Class Code (SUBCC):** 80h = Non VGA
7:0	RO 00h	**Programming Interface (PI):** 00h = Hardwired as a Display controller.

8.2.7 CLS—Cache Line Size

B/D/F/Type: 0/2/1/PCI
Address Offset: 0Ch
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support this register as a PCI slave.

Bit	Access & Default	Description
7:0	RO 00h	**Cache Line Size (CLS):** This field is hardwired to 0s. The IGD as a PCI compliant master does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size.

8.2.8 MLT2—Master Latency Timer

B/D/F/Type: 0/2/1/PCI
Address Offset: Dh
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

Bit	Access & Default	Description
7:0	RO 00h	**Master Latency Timer Count Value (MLTCV):** Hardwired to 0s.

8.2.9 HDR2—Header Type

B/D/F/Type: 0/2/1/PCI
Address Offset: 0Eh
Default Value: 80h
Access: RO
Size: 8 bits

This register contains the Header Type of the IGD.

Bit	Access & Default	Description
7	RO 1b	**Multi Function Status (MFUNC):** Indicates if the device is a Multi-Function Device. The Value of this register is determined by Device 0, offset 54h, DEVEN[4]. If Device 0 DEVEN[4] is set, the MFUNC bit is also set.
6:0	RO 00h	**Header Code (H):** This is a 7-bit value that indicates the Header Code for the IGD. This code has the value 00h, indicating a type 0 configuration space format.

8.2.10 MMADR—Memory Mapped Range Address

B/D/F/Type: 0/2/1/PCI
Address Offset: 10–13h
Default Value: 00000000h
Access: RW, RO
Size: 32 bits

This register requests allocation for the IGD registers and instruction ports. The allocation is for 512 KB and the base address is defined by bits 31:19.

Bit	Access & Default	Description
31:19	RW 0000h	**Memory Base Address (MBA):** Set by the OS, these bits correspond to address signals 31:19.
18:4	RO 0000h	**Address Mask (ADMSK):** Hardwired to 0s to indicate 512 KB address range.
3	RO 0b	**Prefetchable Memory (PREFMEM):** Hardwired to 0 to prevent prefetching.
2:1	RO 00b	**Memory Type (MEMTYP):** Hardwired to 0s to indicate 32-bit address.
0	RO 0b	**Memory / IO Space (MIOS):** Hardwired to 0 to indicate memory space.

8.2.11 SVID2—Subsystem Vendor Identification

B/D/F/Type: 0/2/1/PCI
Address Offset: 2C–2Dh
Default Value: 0000h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:0	RO 0000h	**Subsystem Vendor ID (SUBVID):** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This register can only be cleared by a Reset.

8.2.12 SID2—Subsystem Identification

B/D/F/Type: 0/2/1/PCI
Address Offset: 2E–2Fh
Default Value: 0000h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:0	RO 0000h	**Subsystem Identification (SUBID):** This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This register can only be cleared by a Reset.

8.2.13 ROMADR—Video BIOS ROM Base Address

B/D/F/Type: 0/2/1/PCI
Address Offset: 30–33h
Default Value: 00000000h
Access: RO
Size: 32 bits

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0s.

Bit	Access & Default	Description
31:18	RO 0000h	**ROM Base Address (RBA):** Hardwired to 0s.
17:11	RO 00h	**Address Mask (ADMSK):** Hardwired to 0s to indicate 256 KB address range.
10:1	RO 000h	Reserved**.** Hardwired to 0s.
0	RO 0b	**ROM BIOS Enable (RBE):** 0 = ROM not accessible.

8.2.14 CAPPOINT—Capabilities Pointer

B/D/F/Type: 0/2/1/PCI
Address Offset: 34h
Default Value: D0h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO D0h	**Capabilities Pointer Value (CPV):** This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List, the MSI Capabilities ID registers at the Power Management capability at D0h.

8.2.15 MINGNT—Minimum Grant

B/D/F/Type: 0/2/1/PCI
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Minimum Grant Value (MGV):** The IGD does not burst as a PCI compliant master.

8.2.16 MAXLAT—Maximum Latency

B/D/F/Type: 0/2/1/PCI
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Maximum Latency Value (MLV):** The IGD has no specific requirements for how often it needs to access the PCI bus.

8.2.17 CAPID0—Mirror of Dev0 Capability Identifier

B/D/F/Type: 0/2/1/PCI
Address Offset: 40–50h
Default Value: 00000000000000000100000000010B0009h
Access: RO
Size: 136 bits
BIOS Optimal Default 000000000000h

This register control of bits in this register are only required for customer visible SKU differentiation.

Bit	Access & Default	Description
7:0	RO 09h	**Capability Identifier (CAP_ID):** This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

8.2.18 MGGC—Mirror of Dev 0 GMCH Graphics Control Register

B/D/F/Type: 0/2/1/PCI
Address Offset: 52–53h
Default Value: 0030h
Access: RO
Size: 16 bits

All the Bits in this register are Intel® TXT lockable.

Bit	Access & Default	Description
15:10	RO 00h	Reserved
9:8	RO 0h	**GTT Graphics Memory Size (GGMS):** This field is used to select the amount of main memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. 00 = No memory pre-allocated. GTT cycles (Memory and I/O) are not claimed. 01 = No VT mode, 1 MB of memory pre-allocated for GTT. 10 = VT mode, 2 MB of memory pre-allocated for GTT. 11 = reserved **Note:** This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set.

Bit	Access & Default	Description
7:4	RO 0011b	**Graphics Mode Select (GMS)** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. 0000 = No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Memory and I/O), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80h. 0001 = DVMT (UMA) mode, 1 MB of memory pre-allocated for frame buffer. 0010 = DVMT (UMA) mode, 4 MB of memory pre-allocated for frame buffer. 0011 = DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer. 0100 = DVMT (UMA) mode, 16 MB of memory pre-allocated for frame buffer. 0101 = DVMT (UMA) mode, 32 MB of memory pre-allocated for frame buffer. 0110 = DVMT (UMA) mode, 48 MB of memory pre-allocated for frame buffer. 0111 = DVMT (UMA) mode, 64 MB of memory pre-allocated for frame buffer. 1000 = DVMT (UMA) mode, 128 MB of memory pre-allocated for frame buffer. 1001 = DVMT (UMA) mode, 256 MB of memory pre-allocated for frame buffer. **Note:** This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set. **BIOS Requirement:** BIOS must not set this field to 000 if IVD (bit 1 of this register) is 0.
3:2	RO 00b	Reserved
1	RO 0b	**IGD VGA Disable (IVD):** 0 = Enable. Device 2 (IGD) claims VGA memory and I/O cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1 = Disable. Device 2 (IGD) does not claim VGA cycles (Memory and I/O), and the Sub- Class Code field within Device 2, function 0 Class Code register is 80h. **BIOS Requirement:** BIOS must not set this bit to 0 if the GMS field (bits 6:4 of this register) pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0[38] = 1) or via a register (DEVEN[3] = 0).
0	RO 0b	Reserved

8.2.19 DEVEN—Device Enable

B/D/F/Type: 0/2/1/PCI
Address Offset: 54–57h
Default Value: 000003DBh
Access: RO
Size: 32 bits

This register allows for enabling/disabling of PCI devices and functions that are within the GMCH. The table below the bit definitions describes the behavior of all combinations of transactions to devices controlled by this register. All the bits in this register are Intel® TXT Lockable.

Bit	Access & Default	Description
31:15	RO 00000h	Reserved
14	RO 0b	**Chap Enable (D7EN):** 0 = Bus0:Device7 is disabled and not visible. 1 = Bus0:Device7 is enabled and visible. Non-production BIOS code should provide a setup option to enable Bus0:Device7. When enabled, Bus0:Device7 must be initialized in accordance to standard PCI device initialization procedures.
13:10	RO 0s	Reserved
9	RO 1b	**EP Function 3 (D3F3EN):** 0 = Bus0:Device3:Function3 is disabled and hidden 1 = Bus0:Device3:Function 3 is enabled and visible If Device3:Function0 is disabled and hidden, then Device3:Function3 is also disabled and hidden independent of the state of this bit.
8	RO 1b	**EP Function 2 (D3F2EN):** 0 = Bus0:Device3:Function2 is disabled and hidden 1 = Bus0:Device3:Function2 is enabled and visible If Device3:Function0 is disabled and hidden, then Device3:Function2 is also disabled and hidden independent of the state of this bit.
7	RO 1b	**EP Function 1 (D3F1EN):** 0 = Bus0:Device3:Function1 is disabled and hidden 1 = Bus0:Device3:Function1 is enabled and visible. If this GMCH does not have ME capability (CAPID0[??] = 1), then Device3:Function1 is disabled and hidden independent of the state of this bit.
6	RO 1b	**EP Function 0 (D3F0EN):** 0 = Bus0:Device3:Function0 is disabled and hidden 1 = Bus0:Device3:Function0 is enabled and visible. If this GMCH does not have ME capability (CAPID0[??] = 1), then Device3:Function0 is disabled and hidden independent of the state of this bit.
5	RO 0b	Reserved

Bit	Access & Default	Description
4	RO 1b	**Internal Graphics Engine Function 1 (D2F1EN):** 0 = Bus 0:Device2:Function1 is disabled and hidden 1 = Bus0:Device2:Function1 is enabled and visible If Device2:Function0 is disabled and hidden, then Device2:Function1 is also disabled and hidden independent of the state of this bit. If this component is not capable of Dual Independent Display (CAPID0[78] = 1), then this bit is hardwired to 0b to hide Device2:Function1.
3	RO 1b	**Internal Graphics Engine Function 0 (D2F0EN):** 0 = Bus0:Device2:Function0 is disabled and hidden 1 = Bus0:Device2:Function0 is enabled and visible If this GMCH does not have internal graphics capability (CAPID0[46] = 1), then Device2:Function0 is disabled and hidden independent of the state of this bit.
2	RO	Reserved
1	RO 1b	**PCI Express Port (D1EN):** 0 = Bus0:Device1:Function0 is disabled and hidden. 1 = Bus0:Device1:Function0 is enabled and visible. Default value is determined by the device capabilities (see CAPID0 [44]), SDVO Presence hardware strap and the SDVO/PCIe Concurrent hardware strap. Device 1 is Disabled on Reset if the SDVO Presence strap was sampled high, and the SDVO/PCIe Concurrent strap was sampled low at the last assertion of PWROK, and is enabled by default otherwise.
0	RO 1b	**Host Bridge (D0EN):** Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.

8.2.20 SSRW—Mirror of Fun 0 Software Scratch Read Write

B/D/F/Type: 0/2/1/PCI
Address Offset: 58–5Bh
Default Value: 00000000h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:0	RO 00000000h	Reserved

8.2.21 BSM—Mirror of Func0 Base of Stolen Memory

B/D/F/Type: 0/2/1/PCI
Address Offset: 5C–5Fh
Default Value: 07800000h
Access: RO
Size: 32 bits

Graphics Stolen Memory and TSEG are within DRAM space defined under TOLUD. From the top of low used DRAM, GMCH claims 1 to 64 MBs of DRAM for internal graphics if enabled.

The base of stolen memory will always be below 4 GB. This is required to prevent aliasing between stolen range and the reclaim region.

Bit	Access & Default	Description
31:20	RO 078h	**Base of Stolen Memory (BSM):** This register contains bits 31:20 of the base address of stolen DRAM memory. The host interface determines the base of Graphics Stolen memory by subtracting the graphics stolen memory size from TOLUD. See Device 0 TOLUD for more explanation.
19:0	RO 00000h	Reserved

8.2.22 HSRW—Mirror of Dev2 Func0 Hardware Scratch Read Write

B/D/F/Type: 0/2/1/PCI
Address Offset: 60–61h
Default Value: 0000h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:0	RO 0000h	Reserved

8.2.23 GDRST—Mirror of Dev2 Func0 Graphics Reset

B/D/F/Type: 0/2/1/PCI
Address Offset: C0h
Default Value: 00h
Access: RO
Size: 8 bits

This register is a mirror of the Graphics Reset Register in Device 2.

Bit	Access & Default	Description
7:4	RO 0h	Reserved
3:2	RO 00b	**Graphics Reset Domain (GRDOM):** 00 = Full Graphics Reset will be performed (both render and display clock domain resets asserted 01 = Reserved (Invalid Programming) 10 = Reserved (Invalid Programming) 11 = Reserved (Invalid Programming)
1	RO 0b	Reserved

Bit	Access & Default	Description
0	RO 0b	**Graphics Reset (GDR):** Setting this bit asserts graphics-only reset. The clock domains to be reset are determined by GRDOM. Hardware resets this bit when the reset is complete. Setting this bit without waiting for it to clear, is undefined behavior. Once this bit is set to a 1, all GFX core MMIO registers are returned to power on default state. All Ring buffer pointers are reset, command stream fetches are dropped and ongoing render pipeline processing is halted, state machines and State Variables returned to power on default state. If the Display is reset, all display engines are halted (garbage on screen). VGA memory is not available; Store DWords and interrupts are not ensured to be completed. Device #2 IO registers are not available. Device 2 Configuration registers continue to be available while Graphics reset is asserted. This bit is hardware auto-clear.

8.2.24 PMCAPID—Mirror of Fun 0 Power Management Capabilities ID

B/D/F/Type: 0/2/1/PCI
Address Offset: D0–D1h
Default Value: 0001h
Access: RO
Size: 16 bits

This register is a mirror of function 0 with the same R/W attributes. The hardware implements a single physical register common to both functions 0 and 1.

Bit	Access & Default	Description
15:8	RO 00h	**Next Capability Pointer (NEXT_PTR):** This contains a pointer to next item in capabilities list. This is the final capability in the list and must be set to 00h.
7:0	RO 01h	**Capability Identifier (CAP_ID):** SIG defines this ID is 01h for power management.

8.2.25 PMCAP—Mirror of Fun 0 Power Management Capabilities

B/D/F/Type: 0/2/1/PCI
Address Offset: D2–D3h
Default Value: 0022h
Access: RO
Size: 16 bits

This register is a Mirror of Function 0 with the same read/write attributes. The hardware implements a single physical register common to both functions 0 and 1.

Bit	Access & Default	Description
15:11	RO 00h	**PME Support (PMES):** This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10	RO 0b	**D2 Support (D2):** The D2 power management state is not supported. This bit is hardwired to 0.
9	RO 0b	**D1 Support (D1):** Hardwired to 0 to indicate that the D1 power management state is not supported.
8:6	RO 000b	Reserved
5	RO 1b	**Device Specific Initialization (DSI):** Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
4	RO 0b	Reserved
3	RO 0b	**PME Clock (PMECLK):** Hardwired to 0 to indicate IGD does not support PME# generation.
2:0	RO 010b	**Version (VER):** Hardwired to 010b to indicate that there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the PCI Power Management Interface Specification.

8.2.26 PMCS—Power Management Control/Status

B/D/F/Type: 0/2/1/PCI
Address Offset: D4–D5h
Default Value: 0000h
Access: RO, RW
Size: 16 bits

Bit	Access & Default	Description
15	RO 0b	**PME Status (PMESTS):** This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).
14:13	RO 00b	**Data Scale (DSCALE):** The IGD does not support data register. This bit always returns 0 when read, write operations have no effect.
12:9	RO 0h	**Data Select (DATASEL):** The IGD does not support data register. This bit always returns 0 when read, write operations have no effect.
8	RO 0b	**PME Enable (PME_EN):** This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2	RO 00h	Reserved
1:0	RW 00b	**Power State (PWRSTAT):** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values. 00 = D0 (Default) 01 = D1 (Not Supported) 10 = D2 (Not Supported) 11 = D3

8.2.27 SWSMI—Mirror of Func0 Software SMI

B/D/F/Type: 0/2/1/PCI
Address Offset: E0–E1h
Default Value: 0000h
Access: RO
Size: 16 bits

As long as there is the potential that DVO port legacy drivers exist which expect this register at this address, D2:F0 address E0h–E1h must be reserved for this register.

Bit	Access & Default	Description
15:8	RO 00h	**Software Scratch Bits (SWSB):**
7:1	RO 00h	**Software Flag (SWF):** This field is used to indicate caller and SMI function desired, as well as return result.
0	RO 0b	**GMCH Software SMI Event (GSSMIE):** When Set, this bit will trigger an SMI. Software must write a 0 to clear this bit.

§

9 Intel® Management Engine (ME) Subsystem Registers (D3:F0,F1,F2,F3)

9.1 Host Embedded Controller Interface (HECI1) Configuration Register Details (D3:F0)

Table 9-1. HECI Function in ME Subsystem Register Address Map

Address Offset	Register Symbol	Register Name	Default Value	Access
00–03h	ID	Identifiers	29C48086h	RO
04–05h	CMD	Command	0000h	RO, RW
06–07h	STS	Device Status	0010h	RO
08h	RID	Revision ID	00h	RO
09–0Bh	CC	Class Code	078000h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HTYPE	Header Type	80h	RO
0Fh	BIST	Built In Self Test	00h	RO
10–17h	HECI_MBAR	HECI MMIO Base Address	0000000000000004h	RW, RO
2C–2Fh	SS	Sub System Identifiers	00000000h	RWO
34h	CAP	Capabilities Pointer	50h	RO
3C–3Dh	INTR	Interrupt Information	0100h	RO, RW
3Eh	MGNT	Minimum Grant	00h	RO
3Fh	MLAT	Maximum Latency	00h	RO
40–43h	HFS	Host Firmware Status	00000000h	RO
50–51h	PID	PCI Power Management Capability ID	8C01h	RO
52–53h	PC	PCI Power Management Capabilities	C803h	RO
54–55h	PMCS	PCI Power Management Control And Status	0008h	RWC, RO, RW

Address Offset	Register Symbol	Register Name	Default Value	Access
8C–8Dh	MID	Message Signaled Interrupt Identifiers	0005h	RO
8E–8Fh	MC	Message Signaled Interrupt Message Control	0080h	RO, RW
90–93h	MA	Message Signaled Interrupt Message Address	00000000h	RW, RO
94–97h	MUA	Message Signaled Interrupt Upper Address (Optional)	00000000h	RW
98–99h	MD	Message Signaled Interrupt Message Data	0000h	RW
A0h	HIDM	HECI Interrupt Delivery Mode	00h	RW

9.1.1 ID— Identifiers

B/D/F/Type: 0/3/0/PCI
Address Offset: 00–03h
Default Value: 29C48086h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:16	RO 29C4h	**Device ID (DID):** Indicates what device number assigned by Intel.
15:0	RO 8086h	**Vendor ID (VID):** 16-bit field which indicates Intel is the vendor, assigned by the PCI SIG.

9.1.2 CMD— Command

B/D/F/Type: 0/3/0/PCI
Address Offset: 04–05h
Default Value: 0000h
Access: RO, RW
Size: 16 bits

Bit	Access & Default	Description
15:11	RO 00000b	Reserved
10	RW 0b	**Interrupt Disable (ID):** Disables this device from generating PCI line based interrupts. This bit does not have any effect on MSI operation.
9	RO 0b	**Fast Back-to-Back Enable (FBE):** Not implemented, hardwired to 0.
8	RO 0b	**SERR# Enable (SEE):** Not implemented, hardwired to 0.
7	RO 0b	**Wait Cycle Enable (WCC):** Not implemented, hardwired to 0.
6	RO 0b	**Parity Error Response Enable (PEE):** Not implemented, hardwired to 0.
5	RO 0b	**VGA Palette Snooping Enable (VGA):** Not implemented, hardwired to 0
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Not implemented, hardwired to 0.
3	RO 0b	**Special Cycle Enable (SCE):** Not implemented, hardwired to 0.
2	RW 0b	**Bus Master Enable (BME):** This bit controls the HECI host controller's ability to act as a system memory master for data transfers. When this bit is cleared, HECI bus master activity stops and any active DMA engines return to an idle condition. 1 = Enable 0 = Disable. HECI is blocked from generating MSI to the host processor. Note that this bit does not block HECI accesses to ME-UMA (i.e., writes or reads to the host and ME circular buffers through the read window and write window registers still cause ME backbone transactions to ME-UMA).
1	RW 0b	**Memory Space Enable (MSE):** This bit controls access to the HECI host controller's memory mapped register space. 0 = Disable 1= Enable
0	RO 0b	**I/O Space Enable (IOSE):** Not implemented, hardwired to 0.

9.1.3 STS— Device Status

B/D/F/Type: 0/3/0/PCI
Address Offset: 06–07h
Default Value: 0010h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Not implemented, hardwired to 0.
14	RO 0b	**Signaled System Error (SSE):** Not implemented, hardwired to 0.
13	RO 0b	**Received Master-Abort (RMA):** Not implemented, hardwired to 0.
12	RO 0b	**Received Target Abort (RTA):** Not implemented, hardwired to 0.
11	RO 0b	**Signaled Target-Abort (STA):** Not implemented, hardwired to 0.
10:9	RO 00b	**DEVSEL# Timing (DEVT):** These bits are hardwired to 00.
8	RO 0b	**Master Data Parity Error Detected (DPD):** Not implemented, hardwired to 0.
7	RO 0b	**Fast Back-to-Back Capable (FBC):** Not implemented, hardwired to 0.
6	RO 0b	Reserved
5	RO 0b	**66 MHz Capable (C66):** Not implemented, hardwired to 0.
4	RO 1b	**Capabilities List (CL):** Indicates the presence of a capabilities list, hardwired to 1.
3	RO 0b	**Interrupt Status (IS):** Indicates the interrupt status of the device 0 = Not asserted 1 = Asserted
2:0	RO 000b	Reserved

9.1.4 RID— Revision ID

B/D/F/Type: 0/3/0/PCI
Address Offset: 08h
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Revision ID (RID):** Indicates stepping of the HECI host controller. Refer to the *Intel® 3 Series Express Chipset Family Specification Update* for the value of the Revision ID register.

9.1.5 CC— Class Code

B/D/F/Type: 0/3/0/PCI
Address Offset: 09–0Bh
Default Value: 078000h
Access: RO
Size: 24 bits

Bit	Access & Default	Description
23:16	RO 07h	**Base Class Code (BCC):** Indicates the base class code of the HECI host controller device.
15:8	RO 80h	**Sub Class Code (SCC):** Indicates the sub class code of the HECI host controller device.
7:0	RO 00h	**Programming Interface (PI):** Indicates the programming interface of the HECI host controller device.

9.1.6 CLS— Cache Line Size

B/D/F/Type: 0/3/0/PCI
Address Offset: 0Ch
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Cache Line Size (CLS):** Not implemented, hardwired to 0.

9.1.7 MLT— Master Latency Timer

B/D/F/Type: 0/3/0/PCI
Address Offset: 0Dh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Master Latency Timer (MLT):** Not implemented, hardwired to 0.

9.1.8 HTYPE— Header Type

B/D/F/Type: 0/3/0/PCI
Address Offset: 0Eh
Default Value: 80h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7	RO 1b	**Multi-Function Device (MFD):** Indicates the HECI host controller is part of a multi-function device.
6:0	RO 0000000b	**Header Layout (HL):** Indicates that the HECI host controller uses a target device layout.

9.1.9 HECI_MBAR— HECI MMIO Base Address

B/D/F/Type: 0/3/0/PCI
Address Offset: 10–17h
Default Value: 0000000000000004h
Access: RW, RO
Size: 64 bits

Bit	Access & Default	Description
63:4	RW 00000000 0000000h	**Base Address (BA):** Base address of register memory space. Bits 63:4 correspond to address bits 63:4.
3	RO 0b	**Prefetchable (PF):** Indicates that this range is not pre-fetchable
2:1	RO 10b	**Type (TP):** Indicates that this range can be mapped anywhere in 64-bit address space.
0	RO 0b	**Resource Type Indicator (RTE):** Indicates a request for register memory space.

9.1.10 SS— Sub System Identifiers

B/D/F/Type: 0/3/0/PCI
Address Offset: 2C–2Fh
Default Value: 00000000h
Access: RWO
Size: 32 bits

Bit	Access & Default	Description
31:16	RWO 0000h	**Subsystem ID (SSID):** Indicates the sub-system identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This field can only be cleared by PLTRST#.
15:0	RWO 0000h	**Subsystem Vendor ID (SSVID):** Indicates the sub-system vendor identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This field can only be cleared by PLTRST#.

9.1.11 CAP— Capabilities Pointer

B/D/F/Type: 0/3/0/PCI
Address Offset: 34h
Default Value: 50h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 50h	**Capability Pointer (CP):** Indicates the first capability pointer offset. It points to the PCI power management capability offset.

9.1.12 INTR— Interrupt Information

B/D/F/Type: 0/3/0/PCI
Address Offset: 3C–3Dh
Default Value: 0100h
Access: RO, RW
Size: 16 bits

Bit	Access & Default	Description
15:8	RO 01h	**Interrupt Pin (IPIN):** This indicates the interrupt pin the HECI host controller uses. The value of 01h selects INTA# interrupt pin. **Note:** As HECI is an internal device in the GMCH, the INTA# pin is implemented as an INTA# message to the ICH9.
7:0	RW 00h	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

9.1.13 MGNT— Minimum Grant

B/D/F/Type: 0/3/0/PCI
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Grant (GNT):** Not implemented, hardwired to 0.

9.1.14 MLAT— Maximum Latency

B/D/F/Type: 0/3/0/PCI
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Latency (LAT):** Not implemented, hardwired to 0.

9.1.15 HFS— Host Firmware Status

B/D/F/Type: 0/3/0/PCI
Address Offset: 40–43h
Default Value: 00000000h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:0	RO 00000000h	**Firmware Status Host Access (FS_HA):** Indicates current status of the firmware for the HECI controller. This field is the host's read only access to the FS field in the ME Firmware Status AUX register.

9.1.16 PID— PCI Power Management Capability ID

B/D/F/Type: 0/3/0/PCI
Address Offset: 50–51h
Default Value: 8C01h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:8	RO 8Ch	**Next Capability (NEXT):** Indicates the location of the next capability item in the list. This is the Message Signaled Interrupts capability.
7:0	RO 01h	**Cap ID (CID):** Indicates that this pointer is a PCI power management.

9.1.17 PC— PCI Power Management Capabilities

B/D/F/Type: 0/3/0/PCI
Address Offset: 52–53h
Default Value: C803h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:11	RO 11001b	**PME_Support (PSUP):** Indicates the states that can generate PME#. HECI can assert PME# from any D-state except D1 or D2 which are not supported by HECI.
10	RO 0b	**D2_Support (D2S):** The D2 state is not supported for the HECI host controller.
9	RO 0b	**D1_Support (D1S):** The D1 state is not supported for the HECI host controller.
8:6	RO 000b	**Aux_Current (AUXC):** Reports the maximum Suspend well current required when in the D3COLD state. Value of TBD is reported.
5	RO 0b	**Device Specific Initialization (DSI):** Indicates whether device-specific initialization is required.
4	RO 0b	Reserved
3	RO 0b	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
2:0	RO 011b	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.

9.1.18 PMCS— PCI Power Management Control And Status

B/D/F/Type: 0/3/0/PCI
Address Offset: 54–55h
Default Value: 0008h
Access: RWC, RO, RW
Size: 16 bits

Bit	Access & Default	Description
15	RWC 0b	**PME Status (PMES):** 1 = The PME Status bit in HECI space can be set to 1 by ME FW. 0 = This bit is cleared by host processor writing a 1 to it. ME cannot clear this bit. Host processor writes with value 0 have no effect on this bit. This bit is reset to 0 by MRST#
14:9	RO 000000b	Reserved.
8	RW 0b	**PME Enable (PMEE):** This bit is read/write, under control of host software. It does not directly have an effect on PME events. However, this bit is shadowed into AUX space so ME FW can monitor it. The ME FW is responsible for ensuring that FW does not cause the PME-S bit to transition to 1 while the PMEE bit is 0, indicating that host software had disabled PME. 0 = Disable 1 = Enable This bit is reset to 0 by MRST#.
7:4	RO 0000b	Reserved
3	RO 1b	**No_Soft_Reset (NSR):** This bit indicates that when the HECI host controller is transitioning from D3hot to D0 due to power state command, it does not perform and internal reset. Configuration context is preserved.
2	RO 0b	Reserved
1:0	RW 00b	**Power State (PS):** This field is used both to determine the current power state of the HECI host controller and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state The D1 and D2 states are not supported for this HECI host controller. When in the D3HOT state, the configuration space is available, but the register memory spaces are not. Additionally, interrupts are blocked.

9.1.19 MID— Message Signaled Interrupt Identifiers

B/D/F/Type: 0/3/0/PCI
Address Offset: 8C–8Dh
Default Value: 0005h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:8	RO 00h	**Next Pointer (NEXT):** Indicates the next item in the list. This can be other capability pointers (such as PCI-X or PCI-Express) or it can be the last item in the list.
7:0	RO 05h	**Capability ID (CID):** Capabilities ID indicates MSI.

9.1.20 MC— Message Signaled Interrupt Message Control

B/D/F/Type: 0/3/0/PCI
Address Offset: 8E–8Fh
Default Value: 0080h
Access: RO, RW
Size: 16 bits

Bit	Access & Default	Description
15:8	RO 00h	Reserved
7	RO 1b	**64 Bit Address Capable (C64):** Specifies whether capable of generating 64-bit messages. 0 = Not capable 1 = Capable
6:4	RO 000b	**Multiple Message Enable (MME):** Not implemented, hardwired to 0.
3:1	RO 000b	**Multiple Message Capable (MMC):** Not implemented, hardwired to 0.
0	RW 0b	**MSI Enable (MSIE):** 0 = Disable 1 = MSI is enabled and traditional interrupt pins are not used to generate interrupts.

9.1.21 MA— Message Signaled Interrupt Message Address

B/D/F/Type: 0/3/0/PCI
Address Offset: 90–93h
Default Value: 00000000h
Access: RW, RO
Size: 32 bits

Bit	Access & Default	Description
31:2	RW 00000000h	**Address (ADDR):** This field provides the lower 32 bits of the system specified message address, always DWord aligned. MSI is not translated in Vtd; therefore, to avoid sending bad MSI with address, bit [31:20] will be masked internally to generate 12'hFEE regardless of content in register. Register attribute remains as RW.
1:0	RO 00b	Reserved

9.1.22 MUA— Message Signaled Interrupt Upper Address (Optional)

B/D/F/Type: 0/3/0/PCI
Address Offset: 94–97h
Default Value: 00000000h
Access: RW
Size: 32 bits

Bit	Access & Default	Description
31:0	RW 00000000h	**Upper Address (UADDR):** This field provides the upper 32 bits of the system specified message address. This register is optional and only implemented if MC.C64=1. MSI is not translated in Vtd, therefore, in order to avoid sending bad MSI with address bit [3:0] will be masked internally to generate 4'h0 regardless of content in register. Register attribute remains as RW.

9.1.23 MD— Message Signaled Interrupt Message Data

B/D/F/Type: 0/3/0/PCI
Address Offset: 98–99h
Default Value: 0000h
Access: RW
Size: 16 bits

Bit	Access & Default	Description
15:0	RW 0000h	**Data (Data):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the FSB during the data phase of the MSI memory write transaction.

9.1.24 HIDM—HECI Interrupt Delivery Mode

B/D/F/Type: 0/3/0/PCI
Address Offset: A0h
Default Value: 00h
Access: RW
Size: 8 bits
BIOS Optimal Default 00h

This register is used to select interrupt delivery mechanism for HECI to Host processor interrupts.

Bit	Access & Default	Description
7:2	RO 0h	Reserved
1:0	RW 00b	**HECI Interrupt Delivery Mode (HIDM):** These bits control what type of interrupt the HECI will send when ME FW writes to set the M_IG bit in AUX space. They are interpreted as follows: 00 = Generate Legacy or MSI interrupt 01 = Generate SCI 10 = Generate SMI

9.2 HECI2 Configuration Register Details (D3:F1) (Intel® 82Q35 and 82Q33 GMCH only)

Table 9-2. Second HECI Function in ME Subsystem Register Address Map

Address Offset	Register Symbol	Register Name	Default Value	Access
00–03h	ID	Identifiers	29C58086h	RO
04–05h	CMD	Command	0000h	RO, RW
06–07h	STS	Device Status	0010h	RO
08h	RID	Revision ID	00h	RO
09–0Bh	CC	Class Code	078000h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HTYPE	Header Type	80h	RO
10–17h	HECI_MBAR	HECI MMIO Base Address	0000000000000004h	RO, RW
2C–2Fh	SS	Sub System Identifiers	00000000h	RWO
34h	CAP	Capabilities Pointer	50h	RO
3C–3Dh	INTR	Interrupt Information	0400h	RW, RO
3Eh	MGNT	Minimum Grant	00h	RO
3Fh	MLAT	Maximum Latency	00h	RO
40–43h	HFS	Host Firmware Status	00000000h	RO
50–51h	PID	PCI Power Management Capability ID	8C01h	RO
52–53h	PC	PCI Power Management Capabilities	C803h	RO
54–55h	PMCS	PCI Power Management Control And Status	0008h	RO, RW, RWC
8C–8Dh	MID	Message Signaled Interrupt Identifiers	0005h	RO
8E–8Fh	MC	Message Signaled Interrupt Message Control	0080h	RW, RO
90–93h	MA	Message Signaled Interrupt Message Address	00000000h	RW, RO
94–97h	MUA	Message Signaled Interrupt Upper Address (Optional)	00000000h	RW
98–99h	MD	Message Signaled Interrupt Message Data	0000h	RW
A0h	HIDM	HECI Interrupt Delivery Mode	00h	RW

9.2.1 ID— Identifiers

B/D/F/Type: 0/3/1/PCI
Address Offset: 00–03h
Default Value: 29758086h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:16	RO 2975h	**Device ID (DID):** Indicates what device number assigned by Intel.
15:0	RO 8086h	**Vendor ID (VID):** 16-bit field which indicates Intel is the vendor, assigned by the PCI SIG.

9.2.2 CMD— Command

B/D/F/Type: 0/3/1/PCI
Address Offset: 04–05h
Default Value: 0000h
Access: RO, RW
Size: 16 bits

Bit	Access & Default	Description
15:11	RO 00000b	Reserved
10	RW 0b	**Interrupt Disable (ID):** Disables this device from generating PCI line based interrupts. This bit does not have any effect on MSI operation. 0 = Enable 1 = Disable
9	RO 0b	**Fast Back-to-Back Enable (FBE):** Not implemented, hardwired to 0.
8	RO 0b	**SERR# Enable (SEE):** Not implemented, hardwired to 0.
7	RO 0b	**Wait Cycle Enable (WCC):** Not implemented, hardwired to 0.
6	RO 0b	**Parity Error Response Enable (PEE):** Not implemented, hardwired to 0.
5	RO 0b	**VGA Palette Snooping Enable (VGA):** Not implemented, hardwired to 0
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Not implemented, hardwired to 0.
3	RO 0b	**Special Cycle Enable (SCE):** Not implemented, hardwired to 0.

Bit	Access & Default	Description
2	RW 0b	**Bus Master Enable (BME):** This bit controls the HECI host controller's ability to act as a system memory master for data transfers. When this bit is cleared, HECI bus master activity stops and any active DMA engines return to an idle condition. 0 = Disable. HECI is blocked from generating MSI to the host processor. 1 = Enable. Note that this bit does not block HECI accesses to ME-UMA (i.e., writes or reads to the host and ME circular buffers through the read window and write window registers still cause ME backbone transactions to ME-UMA).
1	RW 0b	**Memory Space Enable (MSE):** This bit controls access to the HECI host controller's memory mapped register space. 0 = Disable 1 = Enable
0	RO 0b	**I/O Space Enable (IOSE):** Not implemented, hardwired to 0.

9.2.3 STS— Device Status

B/D/F/Type: 0/3/1/PCI
Address Offset: 06–07h
Default Value: 0010h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15	RO	**Detected Parity Error (DPE):** Not implemented, hardwired to 0.
14	RO 0b	**Signaled System Error (SSE):** Not implemented, hardwired to 0.
13	RO 0b	**Received Master-Abort (RMA):** Not implemented, hardwired to 0.
12	RO 0b	**Received Target Abort (RTA):** Not implemented, hardwired to 0.
11	RO 0b	**Signaled Target-Abort (STA):** Not implemented, hardwired to 0.
10:9	RO 00b	**DEVSEL# Timing (DEVT):** These bits are hardwired to 00.
8	RO 0b	**Master Data Parity Error Detected (DPD):** Not implemented, hardwired to 0.
7	RO 0b	**Fast Back-to-Back Capable (FBC):** Not implemented, hardwired to 0.
6	RO 0b	Reserved
5	RO 0b	**66 MHz Capable (C66):** Not implemented, hardwired to 0.
4	RO 1b	**Capabilities List (CL):** Indicates the presence of a capabilities list, hardwired to 1.
3	RO 0b	**Interrupt Status (IS):** Indicates the interrupt status of the device. 0 = Not asserted 1 = Asserted
2:0	RO 000b	Reserved

9.2.4 RID— Revision ID

B/D/F/Type: 0/3/1/PCI
Address Offset: 08h
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Revision ID (RID):** Indicates stepping of the HECI host controller. Refer to the *Intel® 3 Series Express Chipset Family Specification Update* for the value of the Revision ID register.

9.2.5 CC— Class Code

B/D/F/Type: 0/3/1/PCI
Address Offset: 09–0Bh
Default Value: 078000h
Access: RO
Size: 24 bits

Bit	Access & Default	Description
23:16	RO 07h	**Base Class Code (BCC):** Indicates the base class code of the HECI host controller device.
15:8	RO 80h	**Sub Class Code (SCC):** Indicates the sub class code of the HECI host controller device.
7:0	RO 00h	**Programming Interface (PI):** Indicates the programming interface of the HECI host controller device.

9.2.6 CLS— Cache Line Size

B/D/F/Type: 0/3/1/PCI
Address Offset: 0Ch
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Cache Line Size (CLS):** Not implemented, hardwired to 0.

9.2.7 MLT— Master Latency Timer

B/D/F/Type: 0/3/1/PCI
Address Offset: 0Dh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Master Latency Timer (MLT):** Not implemented, hardwired to 0.

9.2.8 HTYPE— Header Type

B/D/F/Type: 0/3/1/PCI
Address Offset: 0Eh
Default Value: 80h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7	RO 1b	**Multi-Function Device (MFD):** Indicates the HECI host controller is part of a multi-function device.
6:0	RO 0000000b	**Header Layout (HL):** Indicates that the HECI host controller uses a target device layout.

9.2.9 HECI_MBAR— HECI MMIO Base Address

B/D/F/Type: 0/3/1/PCI
Address Offset: 10–17h
Default Value: 0000000000000004h
Access: RO, RW
Size: 64 bits

This register allocates space for the HECI memory mapped registers defined in Section 1.5.6.

Bit	Access & Default	Description
63:4	RW 00000000 0000000h	**Base Address (BA):** Base address of register memory space.
3	RO 0b	**Prefetchable (PF):** Indicates that this range is not pre-fetchable
2:1	RO 10b	**Type (TP):** Indicates that this range can be mapped anywhere in 32-bit address space
0	RO 0b	**Resource Type Indicator (RTE):** Indicates a request for register memory space.

9.2.10 SS— Sub System Identifiers

B/D/F/Type: 0/3/1/PCI
Address Offset: 2C–2Fh
Default Value: 00000000h
Access: RWO
Size: 32 bits

Bit	Access & Default	Description
31:16	RWO 0000h	**Subsystem ID (SSID):** This field indicates the sub-system identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This field can only be cleared by PLTRST#.
15:0	RWO 0000h	**Subsystem Vendor ID (SSVID):** This field indicates the sub-system vendor identifier. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This field can only be cleared by PLTRST#.

9.2.11 CAP— Capabilities Pointer

B/D/F/Type: 0/3/1/PCI
Address Offset: 34h
Default Value: 50h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 50h	**Capability Pointer (CP):** This field indicates the first capability pointer offset. It points to the PCI power management capability offset.

9.2.12 INTR— Interrupt Information

B/D/F/Type: 0/3/1/PCI
Address Offset: 3C–3Dh
Default Value: 0400h
Access: RW, RO
Size: 16 bits

Bit	Access & Default	Description
15:8	RO 04h	**Interrupt Pin (IPIN):** This field indicates the interrupt pin the HECI host controller uses. The value of 01h selects INTA# interrupt pin. **Note:** As HECI is an internal device in the GMCH, the INTA# pin is implemented as an INTA# message to the ICH9.
7:0	RW 00h	**Interrupt Line (ILINE):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register.

9.2.13 MGNT— Minimum Grant

B/D/F/Type: 0/3/1/PCI
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Grant (GNT):** Not implemented, hardwired to 0.

9.2.14 MLAT— Maximum Latency

B/D/F/Type: 0/3/1/PCI
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	**Latency (LAT):** Not implemented, hardwired to 0.

9.2.15 HFS— Host Firmware Status

B/D/F/Type: 0/3/1/PCI
Address Offset: 40–43h
Default Value: 00000000h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:0	RO 00000000h	**Firmware Status Host Access (FS_HA):** This field indicates current status of the firmware for the HECI controller. This field is the host's read only access to the FS field in the ME Firmware Status AUX register.

9.2.16 PID— PCI Power Management Capability ID

B/D/F/Type: 0/3/1/PCI
Address Offset: 50–51h
Default Value: 8C01h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:8	RO 8Ch	**Next Capability (NEXT):** This field indicates the location of the next capability item in the list. This is the Message Signaled Interrupts capability.
7:0	RO 01h	**Cap ID (CID):** This field indicates that this pointer is a PCI power management.

9.2.17 PC— PCI Power Management Capabilities

B/D/F/Type: 0/3/1/PCI
Address Offset: 52–53h
Default Value: C803h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:11	RO 11001b	**PME_Support (PSUP):** This field indicates the states that can generate PME#. HECI can assert PME# from any D-state except D1 or D2 which are not supported by HECI.
10	RO 0b	**D2_Support (D2S):** The D2 state is not supported for the HECI host controller.
9	RO 0b	**D1_Support (D1S):** The D1 state is not supported for the HECI host controller.
8:6	RO 000b	**Aux_Current (AUXC):** This field reports the maximum Suspend well current required when in the D3COLD state. Value of TBD is reported.
5	RO 0b	**Device Specific Initialization (DSI):** Indicates whether device-specific initialization is required.
4	RO 0b	Reserved
3	RO 0b	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
2:0	RO 011b	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specification.

9.2.18 PMCS— PCI Power Management Control And Status

B/D/F/Type: 0/3/1/PCI
Address Offset: 54–55h
Default Value: 0008h
Access: RO, RW, RWC
Size: 16 bits

Bit	Access & Default	Description
15	RWC 0b	**PME Status (PMES):** The PME Status bit in HECI space can be set to 1 by ME FW performing a write into AUX register to set PMES. This bit is cleared by host processor writing a 1 to it. ME FW cannot clear this bit. Host processor writes with value 0 have no effect on this bit. This bit is reset to 0 by MRST#.
14:9	RO 000000b	Reserved.
8	RW 0b	**PME Enable (PMEE):** This bit is read/write, under control of host software. It does not directly have an effect on PME events. However, this bit is shadowed into AUX space so ME FW can monitor it. The ME FW is responsible for ensuring that FW does not cause the PME-S bit to transition to 1 while the PMEE bit is 0, indicating that host software had disabled PME. This bit is reset to 0 by MRST#.
7:4	RO 0000b	Reserved
3	RO 1b	**No_Soft_Reset (NSR):** This bit indicates that when the HECI host controller is transitioning from D3hot to D0 due to power state command, it does not perform an internal reset. Configuration context is preserved: Reserved.
2	RO 0b	Reserved
1:0	RW 00b	**Power State (PS):** This field is used both to determine the current power state of the HECI host controller and to set a new power state. 00 = D0 state 11 = D3HOT state The D1 and D2 states are not supported for this HECI host controller. When in the D3HOT state, the configuration space is available, but the register memory spaces are not. Additionally, interrupts are blocked.

9.2.19 MID— Message Signaled Interrupt Identifiers

B/D/F/Type: 0/3/1/PCI
Address Offset: 8C–8Dh
Default Value: 0005h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:8	RO 00h	**Next Pointer (NEXT):** This field indicates the next item in the list. This can be other capability pointers (such as PCI-X or PCI-Express) or it can be the last item in the list.
7:0	RO 05h	**Capability ID (CID):** Capabilities ID indicates MSI.

9.2.20 MC— Message Signaled Interrupt Message Control

B/D/F/Type: 0/3/1/PCI
Address Offset: 8E–8Fh
Default Value: 0080h
Access: RW, RO
Size: 16 bits

Bit	Access & Default	Description
15:8	RO 00h	Reserved
7	RO 1b	**64 Bit Address Capable (C64):** This bit specifies whether device is capable of generating 64-bit messages.
6:4	RO 000b	**Multiple Message Enable (MME):** Not implemented, hardwired to 0.
3:1	RO 000b	**Multiple Message Capable (MMC):** Not implemented, hardwired to 0.
0	RW 0b	**MSI Enable (MSIE):** 0 = Disable 1 = Enable. MSI is enabled and traditional interrupt pins are not used to generate interrupts.

9.2.21 MA— Message Signaled Interrupt Message Address

B/D/F/Type: 0/3/1/PCI
Address Offset: 90–93h
Default Value: 00000000h
Access: RW, RO
Size: 32 bits

Bit	Access & Default	Description
31:2	RW 00000000h	**Address (ADDR):** This field provides the lower 32 bits of the system specified message address, always DWord aligned. MSI is not translated in Vtd, therefore, in order to avoid sending bad MSI with address bit [31:20] will be masked internally to generate 12'hFEE regardless of content in register. Register attribute remains as RW.
1:0	RO 00b	Reserved

9.2.22 MUA— Message Signaled Interrupt Upper Address (Optional)

B/D/F/Type: 0/3/1/PCI
Address Offset: 94–97h
Default Value: 00000000h
Access: RW
Size: 32 bits

Bit	Access & Default	Description
31:0	RW 00000000h	**Upper Address (UADDR):** Upper 32 bits of the system specified message address. This register is optional and only implemented if MC.C64=1. MSI is not translated in Vtd, therefore, in order to avoid sending bad MSI with address bit [3:0] will be masked internally to generate 4'h0 regardless of content in register. Register attribute remains as RW.

9.2.23 MD— Message Signaled Interrupt Message Data

B/D/F/Type: 0/3/1/PCI
Address Offset: 98–99h
Default Value: 0000h
Access: RW
Size: 16 bits

Bit	Access & Default	Description
15:0	RW 0000h	**Data (Data):** This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the FSB during the data phase of the MSI memory write transaction.

9.2.24 HIDM—HECI Interrupt Delivery Mode

B/D/F/Type: 0/3/1/PCI
Address Offset: A0h
Default Value: 00h
Access: RW
Size: 8 bits
BIOS Optimal Default 00h

This register is used to select interrupt delivery mechanism for HECI to Host processor interrupts.

Bit	Access & Default	Description
7:2	RO 0h	Reserved
1:0	RW 00b	**HECI Interrupt Delivery Mode (HIDM):** These bits control what type of interrupt the HECI will send when ME FW writes to set the M_IG bit in AUX space. They are interpreted as follows: 00 = Generate Legacy or MSI interrupt 01 = Generate SCI 10 = Generate SMI

9.3 IDE Function for Remote Boot and Installations PT IDER Register Details (D3:F2) (Intel® 82Q35 and 82Q33 GMCH Only)

Table 9-3. IDE Function for Remote Boot and Installations PT IDER Register Address Map

Address Offset	Register Symbol	Register Name	Default Value	Access
00–3h	ID	Identification	29C68086h	RO
04–5h	CMD	Command Register	0000h	RO, RW
06–7h	STS	Device Status	00B0h	RO
08h	RID	Revision ID	00h	RO
09–Bh	CC	Class Codes	010185h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HTYPE	Header Type	00h	RO
10–13h	PCMDBA	Primary Command Block IO Bar	00000001h	RO, RW
14–17h	PCTLBA	Primary Control Block Base Address	00000001h	RO, RW
18–1Bh	SCMDBA	Secondary Command Block Base Address	00000001h	RO, RW
1C–1Fh	SCTLBA	Secondary Control Block base Address	00000001h	RO, RW
20–23h	LBAR	Legacy Bus Master Base Address	00000001h	RO, RW
24–27h	RSVD	Reserved	00000000h	RO
2C–2Fh	SS	Sub System Identifiers	00008086h	RWO
30–33h	EROM	Expansion ROM Base Address	00000000h	RO
34h	CAP	Capabilities Pointer	C8h	RO
3C–3Dh	INTR	Interrupt Information	0300h	RW, RO
3Eh	MGNT	Minimum Grant	00h	RO
3Fh	MLAT	Maximum Latency	00h	RO
C8–C9h	PID	PCI Power Management Capability ID	D001h	RO
CA–CBh	PC	PCI Power Management Capabilities	0023h	RO
CC–CFh	PMCS	PCI Power Management Control and Status	00000000h	RO, RW, RO/V
D0–D1h	MID	Message Signaled Interrupt Capability ID	0005h	RO
D2–D3h	MC	Message Signaled Interrupt Message Control	0080h	RO, RW

Address Offset	Register Symbol	Register Name	Default Value	Access
D4–D7h	MA	Message Signaled Interrupt Message Address	00000000h	RO, RW
D8–DBh	MAU	Message Signaled Interrupt Message Upper Address	00000000h	RO, RW
DC–DDh	MD	Message Signaled Interrupt Message Data	0000h	RW

9.3.1 ID—Identification

B/D/F/Type: 0/3/2/PCI
Address Offset: 00–03h
Default Value: 29C68086h
Access: RO
Size: 32 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
31:16	RO 29C6h	**Device ID (DID):** Assigned by Manufacturer, identifies the type of Device.
15:0	RO 8086h	**Vendor ID (VID):** 16-bit field which indicates the company vendor as Intel.

9.3.2 CMD—Command Register

B/D/F/Type: 0/3/2/PCI
Address Offset: 04–05h
Default Value: 0000h
Access: RO, RW
Size: 16 bits

This register provides basic control over the device's ability to respond to and perform Host system related accesses.

Note: Reset: Host System reset or D3->D0 transition of function.

Bit	Access & Default	Description
15:11	RO 00h	Reserved
10	RW 0b	**Interrupt Disable (ID):** This disables pin-based INTx# interrupts. This bit has no effect on MSI operation. 0 = Enable. Internal INTx# messages are generated if there is an interrupt ***and*** MSI is not enabled. 1 = Disable. Internal INTx# messages will not be generated.
9	RO 0b	**Fast back-to-back enable (FBE):** Reserved
8	RO 0b	**SERR# Enable (SEE):** The PT function never generates an SERR#. This bit is reserved.
7	RO 0b	**Wait Cycle Enable (WCC):** Reserved
6	RO 0b	**Parity Error Response Enable (PEE):** No Parity detection in PT functions. This bit is reserved.
5	RO 0b	**VGA Palette Snooping Enable (VGA):** Reserved
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Reserved
3	RO 0b	**Special Cycle enable (SCE):** Reserved
2	RW 0b	**Bus Master Enable (BME):** This bit controls the PT function's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands. 0 = Disable 1 = Enable
1	RO 0b	**Memory Space Enable (MSE):** PT function does not contain target memory space.
0	RW 0b	**I/O Space enable (IOSE):** This bit controls access to the PT function's target I/O space. 0 = Disable 1 = Enable

9.3.3 STS—Device Status

B/D/F/Type: 0/3/2/PCI
Address Offset: 06–07h
Default Value: 00B0h
Access: RO
Size: 16 bits

This register is used by the function to reflect its PCI status to the host for the functionality that it implements.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** No parity error on its interface.
14	RO 0b	**Signaled System Error (SSE):** The PT function will never generate an SERR#.
13	RO 0b	**Received Master-Abort Status (RMA):** Reserved
12	RO 0b	**Received Target-Abort Status (RTA):** Reserved
11	RO 0b	**Signaled Target-Abort Status (STA):** The PT Function will never generate a target abort. This bit is reserved.
10:9	RO 0b	**DEVSEL# Timing Status (DEVT):** Controls the device select time for the PT function's PCI interface.
8	RO 0b	**Master Data Parity Error Detected) (DPD):** PT function (IDER), as a master, does not detect a parity error. Other PT function is not a master and hence this bit is reserved also.
7	RO 1b	**Fast back to back capable (RSVD):** Reserved
6	RO 0b	Reserved
5	RO 1b	**66MHz capable (RSVD):**
4	RO 1b	**Capabilities List (CL):** This bit indicates that there is a capabilities pointer implemented in the device.
3	RO 0b	**Interrupt Status (IS):** This bit reflects the state of the interrupt in the function. Setting of the Interrupt Disable bit to 1 has no affect on this bit. Only when this bit is a 1 and ID bit is 0 is the INTc interrupt asserted to the Host
2:0	RO 000b	Reserved

9.3.4 RID—Revision ID

B/D/F/Type: 0/3/2/PCI
Address Offset: 08h
Default Value: 00h
Access: RO
Size: 8 bits

This register specifies a device specific revision.

Bit	Access & Default	Description
7:0	RO 00h	**Revision ID (RID):** Refer to the *Intel® 3 Series Express Chipset Family Specification Update* for the value of the Revision ID register.

9.3.5 CC—Class Codes

B/D/F/Type: 0/3/2/PCI
Address Offset: 09–0Bh
Default Value: 010185h
Access: RO
Size: 24 bits

This register identifies the basic functionality of the device (i.e., IDE mass storage).

Bit	Access & Default	Description
23:0	RO 010185h	**Programming Interface BCC SCC (PI BCC SCC):**

9.3.6 CLS—Cache Line Size

B/D/F/Type: 0/3/2/PCI
Address Offset: 0Ch
Default Value: 00h
Access: RO
Size: 8 bits

This register defines the system cache line size in DWORD increments. This register is mandatory for master that use the Memory-Write and Invalidate command.

Bit	Access & Default	Description
7:0	RO 00h	**Cache Line Size (CLS):** All writes to system memory are memory writes.

9.3.7 MLT—Master Latency Timer

B/D/F/Type: 0/3/2/PCI
Address Offset: 0Dh
Default Value: 00h
Access: RO
Size: 8 bits

This register defines the minimum number of PCI clocks the bus master can retain ownership of the bus whenever it initiates new transactions.

Bit	Access & Default	Description
7:0	RO 00h	**Master Latency Timer (MLT):** Not implemented since the function is in (G)MCH.

9.3.8 HTYPE—Header Type

B/D/F/Type: 0/3/2/PCI
Address Offset: 0Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	Reserved

9.3.9 PCMDBA—Primary Command Block IO Bar

B/D/F/Type: 0/3/2/PCI
Address Offset: 10–13h
Default Value: 00000001h
Access: RO, RW
Size: 32 bits

This 8-byte I/O space is used in Native Mode for the Primary Controller's Command Block (i.e., BAR0).

Note: Reset: Host system Reset or D3->D0 transition of the function.

Bit	Access & Default	Description
31:16	RO 0000h	Reserved
15:3	RW 0000h	**Base Address (BAR):** This field provides the base address of the BAR0 I/O space (8 consecutive I/O locations)
2:1	RO 00b	Reserved
0	RO 1b	**Resource Type Indicator (RTE):** Indicates a request for I/O space.

9.3.10 PCTLBA—Primary Control Block Base Address

B/D/F/Type: 0/3/2/PCI
Address Offset: 14–17h
Default Value: 00000001h
Access: RO, RW
Size: 32 bits

This 4-byte I/O space is used in Native Mode for the Primary Controller's Control Block (i.e., BAR1).

Note: Reset: Host system Reset or D3->D0 transition of the function.

Bit	Access & Default	Description
31:16	RO 0000h	Reserved
15:2	RW 0000h	**Base Address (BAR):** This field provides the base address of the BAR1 I/O space (4 consecutive I/O locations)
1	RO 0b	Reserved
0	RO 1b	**Resource Type Indicator (RTE):** Indicates a request for I/O space

9.3.11 SCMDBA—Secondary Command Block Base Address

B/D/F/Type: 0/3/2/PCI
Address Offset: 18–1Bh
Default Value: 00000001h
Access: RO, RW
Size: 32 bits

This 8-byte I/O space is used in Native Mode for the secondary Controller's Command Block. Secondary Channel is not implemented and reads return 7F7F7F7Fh and all writes are ignored.

Note: Reset: Host System Reset or D3->D0 transition of the function.

Bit	Access & Default	Description
31:16	RO 0000h	Reserved
15:3	RW 0000h	**Base Address (BAR):** This field provides the base address of the I/O space (8 consecutive I/O locations)
2:1	RO 00b	Reserved
0	RO 1b	**Resource Type Indicator (RTE):** Indicates a request for I/O space

9.3.12 SCTLBA—Secondary Control Block base Address

B/D/F/Type: 0/3/2/PCI
Address Offset: 1C–1Fh
Default Value: 00000001h
Access: RO, RW
Size: 32 bits

This 4-byte I/O space is used in Native Mode for Secondary Controller's Control block. Secondary Channel is not implemented and reads return 7F7F7F7Fh and all writes are ignored.

Note: Reset: Host System Reset or D3->D0 transition.

Bit	Access & Default	Description
31:16	RO 0000h	Reserved
15:2	RW 0000h	**Base Address (BAR):** This field provides the base address of the I/O space (4 consecutive I/O locations)
1	RO 0b	Reserved
0	RO 1b	**Resource Type Indicator (RTE):** Indicates a request for I/O space

9.3.13 LBAR—Legacy Bus Master Base Address

B/D/F/Type: 0/3/2/PCI
Address Offset: 20–23h
Default Value: 00000001h
Access: RO, RW
Size: 32 bits

This Bar is used to allocate I/O space for the SFF-8038i mode of operation (a.k.a. Bus Master IDE).

Note: Reset: Host system Reset or D3->D0 transition.

Bit	Access & Default	Description
31:16	RO 0000h	Reserved
15:4	RW 000h	**Base Address (BA):** This field provides the base address of the I/O space (16 consecutive I/O locations).
3:1	RO 000b	Reserved
0	RO 1b	**Resource Type Indicator (RTE):** Indicates a request for I/O space.

9.3.14 SS—Sub System Identifiers

B/D/F/Type: 0/3/2/PCI
Address Offset: 2C–2Fh
Default Value: 00008086h
Access: RWO
Size: 32 bits

These registers are used to uniquely identify the add-in card or the subsystem that the device resides within.

Note: Reset: Host System Reset.

Bit	Access & Default	Description
31:16	RWO 0000h	**Subsystem ID (SSID):** This field is written by BIOS. No hardware action taken on this value.
15:0	RWO 8086h	**Subsystem Vendor ID (SSVID):** This field is written by BIOS. No hardware action taken on this value.

9.3.15 EROM—Expansion ROM Base Address

B/D/F/Type: 0/3/2/PCI
Address Offset: 30–33h
Default Value: 00000000h
Access: RO
Size: 32 bits

This optional register is not implemented.

Bit	Access & Default	Description
31:11	RO 000000h	**Expansion ROM Base Address (ERBAR):**
10:1	RO 000h	Reserved
0	RO 0b	**Enable (EN):** Enable expansion ROM Access

9.3.16 CAP—Capabilities Pointer

B/D/F/Type: 0/3/2/PCI
Address Offset: 34h
Default Value: C8h
Access: RO
Size: 8 bits

This optional register is used to point to a linked list of new capabilities implemented by the device.

Bit	Access & Default	Description
7:0	RO C8h	**Capability Pointer (CP):** This field indicates that the first capability pointer offset is offset C8h (the power management capability)

9.3.17 INTR—Interrupt Information

B/D/F/Type: 0/3/2/PCI
Address Offset: 3C–3Dh
Default Value: 0300h
Access: RW, RO
Size: 16 bits

See definitions in the registers below.

Note: Reset: Host System Reset or D3->D0 reset of the function.

Bit	Access & Default	Description
15:8	RO 03h	**Interrupt Pin (IPIN):** a value of 0x1/0x2/0x3/0x4 indicates that this function implements legacy interrupt on INTA/INTB/INTC/INTD, respectively **Function** **Value** **INTx** (2 IDE) 03h INTC
7:0	RW 00h	**Interrupt Line (ILINE):** The value written in this register indicates which input of the system interrupt controller, the device's interrupt pin is connected. This value is used by the OS and the device driver, and has no affect on the hardware.

9.3.18 MGNT—Minimum Grant

B/D/F/Type: 0/3/2/PCI
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

This optional register is not implemented.

Bit	Access & Default	Description
7:0	RO 00h	Reserved

9.3.19 MLAT—Maximum Latency

B/D/F/Type: 0/3/2/PCI
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

This optional register is not implemented.

Bit	Access & Default	Description
7:0	RO 00h	Reserved

9.3.20 PID—PCI Power Management Capability ID

B/D/F/Type: 0/3/2/PCI
Address Offset: C8–C9h
Default Value: D001h
Access: RO
Size: 16 bits

See register definitions below

Bit	Access & Default	Description
15:8	RO D0h	**Next Capability (NEXT):** The value of D0h points to the MSI capability.
7:0	RO 01h	**Cap ID (CID):** Indicates that this pointer is a PCI power management.

9.3.21 PC—PCI Power Management Capabilities

B/D/F/Type: 0/3/2/PCI
Address Offset: CA–CBh
Default Value: 0023h
Access: RO
Size: 16 bits

This register implements the power management capabilities of the function.

Bit	Access & Default	Description
15:11	RO 00000b	**PME Support (PME):** Indicates no PME# in the PT function.
10	RO 0b	**D2 Support (D2S):** The D2 state is not Supported.
9	RO 0b	**D1 Support (D1S):** The D1 state is not supported.
8:6	RO 000b	**Aux Current (AUXC):** PME# from D3 (cold) state is not supported, therefore this field is 000b.
5	RO 1b	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
4	RO 0b	Reserved
3	RO 0b	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
2:0	RO 011b	**Version (VS):** Indicates support for revision 1.2 of the PCI power management specification.

9.3.22 PMCS—PCI Power Management Control and Status

B/D/F/Type: 0/3/2/PCI
Address Offset: CC–CFh
Default Value: 00000000h
Access: RO, RW, RO/V
Size: 32 bits
BIOS Optimal Default 0000h

This register implements the PCI PM Control and Status Register to allow PM state transitions and Wake up.

Note the NSR bit of this register. All registers (PCI configuration and Device Specific) marked with D3->D0 transition reset will only do so if this bit reads a 0. If this bit is a 1, the D3->D0 transition will not reset the registers.

Note: Reset: Host System Reset or D3->D0 transition.

Bit	Access & Default	Description
31:16	RO 0h	Reserved
15	RO 0b	**PME Status (PMES):** Not supported.
14:9	RO 00h	Reserved
8	RO 0b	**PME Enable (PMEE):** Not Supported
7:4	RO 0000b	Reserved
3	RO/V 0b	**No Soft Reset (NSR):** 1 = Indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. 0 = Devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full re-initialization sequence is needed to return the device to D0 Initialized. When this bit is 0, device performs internal reset. When this bit is 1, Device does not perform internal reset.
2	RO 0b	Reserved
1:0	RW 00b	**Power State (PS):** This field is used both to determine the current power state of the PT function and to set a new power state. The values are: 00 = D0 state 11 = $D3_{HOT}$ state When in the $D3_{HOT}$ state, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. If software attempts to write a 10 or 01 to these bits, the write will be ignored.

9.3.23 MID—Message Signaled Interrupt Capability ID

B/D/F/Type: 0/3/2/PCI
Address Offset: D0–D1h
Default Value: 0005h
Access: RO
Size: 16 bits

Message Signaled Interrupt is a feature that allows the device/function to generate an interrupt to the host by performing a DWORD memory write to a system specified address with system specified data. This register is used to identify and configure an MSI capable device.

Bit	Access & Default	Description
15:8	RO 00h	**Next Pointer (NEXT):** Value indicates this is the last item in the capabilities list.
7:0	RO 05h	**Capability ID (CID):** Capabilities ID value indicates device is capable of generating an MSI.

9.3.24 MC—Message Signaled Interrupt Message Control

B/D/F/Type: 0/3/2/PCI
Address Offset: D2–D3h
Default Value: 0080h
Access: RO, RW
Size: 16 bits

This register provides System Software control over MSI.

Note: Reset: Host System Reset or D3->D0 transition.

Bit	Access & Default	Description
15:8	RO 00h	Reserved
7	RO 1b	**64 Bit Address Capable (C64):** Capable of generating 64-bit and 32-bit messages
6:4	RW 000b	**Multiple Message Enable (MME):** These bits are R/W for software compatibility, but only one message is ever sent by the PT function
3:1	RO 000b	**Multiple Message Capable (MMC):** Only one message is required
0	RW 0b	**MSI Enable (MSIE):** If set MSI is enabled and traditional interrupt pins are not used to generate interrupts

9.3.25 MA—Message Signaled Interrupt Message Address

B/D/F/Type: 0/3/2/PCI
Address Offset: D4–D7h
Default Value: 00000000h
Access: RO, RW
Size: 32 bits

This register specifies the DWord aligned address programmed by system software for sending MSI.

Note: Reset: Host system Reset or D3->D0 transition.

Bit	Access & Default	Description
31:2	RW 00000000h	**Address (ADDR):** Lower 32 bits of the system specified message address, always DWORD aligned Force host MSI address to 0_FEEx_XXXXh before sending to backbone, regardless of values programmed in MA and MUA registers under respective PCI Configuration Space. Note that the MA and MUA registers should continued to be RW (no change to registers implementation, just hardcode 0_FEEh as bit[35:20] for MSI cycles to backbone).
1:0	RO 00b	Reserved

9.3.26 MAU—Message Signaled Interrupt Message Upper Address

B/D/F/Type: 0/3/2/PCI
Address Offset: D8–DBh
Default Value: 00000000h
Access: RO, RW
Size: 32 bits

This register provides the upper 32 bits of the message address for the 64bit address capable device.

Note: Reset: Host system Reset or D3->D0 transition.

Bit	Access & Default	Description
31:4	RO 0000000h	Reserved
3:0	RW 0000b	**Address (ADDR):** Upper 4 bits of the system specified message address

9.3.27 MD—Message Signaled Interrupt Message Data

B/D/F/Type: 0/3/2/PCI
Address Offset: DC–DDh
Default Value: 0000h
Access: RW
Size: 16 bits

This 16-bit field is programmed by system software if MSI is enabled.

Note: Reset: Host system Reset or D3->D0 transition.

Bit	Access & Default	Description
15:0	RW 0000h	**Data (DATA):** This content is driven onto the lower word of the data bus of the MSI memory write transaction

9.4 Serial Port for Remote Keyboard and Text KT Redirection Register Details (D3:F3) (Intel® 82Q35 and 82Q33 GMCH Only)

Table 9-4. Serial Port for Remote Keyboard and Text KT Redirection Register Address Map

Address Offset	Register Symbol	Register Name	Default Value	Access
00–03h	ID	Identification	29C78086h	RO
04–05h	CMD	Command Register	0000h	RO, RW
06–07h	STS	Device Status	00B0h	RO
08h	RID	Revision ID	00h	RO
09–0Bh	CC	Class Codes	070002h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HTYPE	Header Type	00h	RO
10–13h	KTIBA	KT IO Block Base Address	00000001h	RO, RW
14–17h	KTMBA	KT Memory Block Base Address	00000000h	RO, RW
2C–2Fh	SS	Sub System Identifiers	00008086h	RWO
30–33h	EROM	Expansion ROM Base Address	00000000h	RO
34h	CAP	Capabilities Pointer	C8h	RO
3C–3Dh	INTR	Interrupt Information	0200h	RW, RO
3Eh	MGNT	Minimum Grant	00h	RO
3Fh	MLAT	Maximum Latency	00h	RO
C8–C9h	PID	PCI Power Management Capability ID	D001h	RO
CA–CBh	PC	PCI Power Management Capabilities	0023h	RO
CC–CFh	PMCS	PCI Power Management Control and Status	00000000h	RO/V, RO, RW
D0–D1h	MID	Message Signaled Interrupt Capability ID	0005h	RO
D2–D3h	MC	Message Signaled Interrupt Message Control	0080h	RO, RW
D4–D7h	MA	Message Signaled Interrupt Message Address	00000000h	RO, RW
D8–DBh	MAU	Message Signaled Interrupt Message Upper Address	00000000h	RO, RW
DC–DDh	MD	Message Signaled Interrupt Message Data	0000h	RW

9.4.1 ID—Identification

B/D/F/Type: 0/3/3/PCI
Address Offset: 00-03h
Default Value: 29C78086h
Access: RO
Size: 32 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
31:16	RO 29C7h	**Device ID (DID):** Assigned by manufacturer, identifies the device
15:0	RO 8086h	**Vendor ID (VID):** 16-bit field which indicates the company vendor as Intel

9.4.2 CMD—Command Register

B/D/F/Type: 0/3/3/PCI
Address Offset: 04-05h
Default Value: 0000h
Access: RO, RW
Size: 16 bits

This register provides basic control over the device's ability to respond to and perform Host system related accesses.

Note: Reset: Host System reset or D3->D0 transition.

Bit	Access & Default	Description
15:11	RO 00h	Reserved
10	RW 0b	**Interrupt Disable (ID):** This bit disables pin-based INTx# interrupts. This bit has no effect on MSI operation. 0 = Enable. Internal INTx# messages are generated if there is an interrupt ***and*** MSI is not enabled. 1 = Disable. Internal INTx# messages will not be generated.
9	RO 0b	**Fast back-to-back enable (FBE):** Reserved
8	RO 0b	**SERR# Enable (SEE):** The PT function never generates an SERR#. This bit is Reserved.
7	RO 0b	**Wait Cycle Enable (WCC):** Reserved

Bit	Access & Default	Description
6	RO 0b	**Parity Error Response Enable (PEE):** No Parity detection in PT functions. This bit is Reserved.
5	RO 0b	**VGA Palette Snooping Enable (VGA):** Reserved
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Reserved
3	RO 0b	**Special Cycle enable (SCE):** Reserved
2	RW 0b	**Bus Master Enable (BME):** Controls the KT function's ability to act as a master for data transfers. This bit does not impact the generation of completions for split transaction commands. For KT, the only bus mastering activity is MSI generation. 0 = Disable 1 = Enable
1	RW 0b	**Memory Space Enable (MSE):** This bit controls Access to the PT function's target memory space. 0 = Disable 1 = Enable
0	RW 0b	**I/O Space enable (IOSE):** This bit controls access to the PT function's target I/O space. 0 = Disable 1 = Enable

9.4.3 STS—Device Status

B/D/F/Type: 0/3/3/PCI
Address Offset: 06-07h
Default Value: 00B0h
Access: RO
Size: 16 bits

This register is used by the function to reflect its PCI status to the host for the functionality that it implements.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** No parity error on its interface
14	RO 0b	**Signaled System Error (SSE):** The PT function will never generate a SERR#.
13	RO 0b	**Received Master-Abort Status (RMA):** Reserved
12	RO 0b	**Received Target-Abort Status (RTA):** Reserved
11	RO 0b	**Signaled Target-Abort Status (STA):** The PT Function will never generate a target abort. This bit is Reserved.
10:9	RO 00b	**DEVSEL# Timing Status (DEVT):** Controls the device select time for the PT function's PCI interface.
8	RO 0b	**Master Data Parity Error Detected) (DPD):** PT function (IDER), as a master, does not detect a parity error. Other PT function is not a master and hence this bit is reserved.
7	RO 1b	**Fast back to back capable (FB2B):** Reserved
6	RO 0b	Reserved
5	RO 1b	**66MHz capable (RSVD):**
4	RO 1b	**Capabilities List (CL):** Indicates that there is a capabilities pointer implemented in the device.
3	RO 0b	**Interrupt Status (IS):** This bit reflects the state of the interrupt in the function. Setting of the Interrupt Disable bit to 1 has no affect on this bit. Only when this bit is a 1 and ID bit is 0 is the INTB interrupt asserted to the Host.
2:0	RO 000b	Reserved

9.4.4 RID—Revision ID

B/D/F/Type: 0/3/3/PCI
Address Offset: 08h
Default Value: 00h
Access: RO
Size: 8 bits

This register specifies a device specific revision.

Bit	Access & Default	Description
7:0	RO 00h	**Revision ID (RID):** Indicates stepping of the silicon. Refer to the *Intel® 3 Series Express Chipset Family Specification Update* for the value of the Revision ID register.

9.4.5 CC—Class Codes

B/D/F/Type: 0/3/3/PCI
Address Offset: 09-0Bh
Default Value: 070002h
Access: RO
Size: 24 bits

This register identifies the basic functionality of the device i.e. Serial Com Port.

Bit	Access & Default	Description
23:0	RO 070002h	**Programming Interface BCC SCC (PI BCC SCC):**

9.4.6 CLS—Cache Line Size

B/D/F/Type: 0/3/3/PCI
Address Offset: 0Ch
Default Value: 00h
Access: RO
Size: 8 bits

This register defines the system cache line size in DWORD increments. This register is mandatory for master that uses the Memory-Write and Invalidate command.

Bit	Access & Default	Description
7:0	RO 00h	**Cache Line Size (CLS):** All writes to system memory are Memory Writes.

9.4.7 MLT—Master Latency Timer

B/D/F/Type: 0/3/3/PCI
Address Offset: 0Dh
Default Value: 00h
Access: RO
Size: 8 bits

This register defines the minimum number of PCI clocks the bus master can retain ownership of the bus whenever it initiates new transactions.

Bit	Access & Default	Description
7:0	RO 00h	**Master Latency Timer (MLT):** Not implemented since the function is in (G)MCH.

9.4.8 HTYPE—Header Type

B/D/F/Type: 0/3/3/PCI
Address Offset: 0Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00h	Reserved

9.4.9 KTIBA—KT IO Block Base Address

B/D/F/Type: 0/3/3/PCI
Address Offset: 10–13h
Default Value: 00000001h
Access: RO, RW
Size: 32 bits

This register provides the base address for the 8-byte I/O space for KT.

Note: Reset: Host system Reset or D3->D0 transition.

Bit	Access & Default	Description
31:16	RO 0000h	Reserved
15:3	RW 0000h	**Base Address (BAR):** This field provides the base address of the I/O space (8 consecutive I/O locations)
2:1	RO 00b	Reserved
0	RO 1b	**Resource Type Indicator (RTE):** Indicates a request for I/O space

9.4.10 KTMBA—KT Memory Block Base Address

B/D/F/Type: 0/3/3/PCI
Address Offset: 14–17h
Default Value: 00000000h
Access: RO, RW
Size: 32 bits

This register provides the base address of memory-mapped space.

Note: Reset: Host system Reset or D3->D0 transition.

Bit	Access & Default	Description
31:12	RW 00000h	**Base Address (BAR):** This field provides the base address of the memory-mapped IO BAR
11:4	RO 00h	Reserved
3	RO 0b	**Prefetchable (PF):** Indicates that this range is not pre-fetchable.
2:1	RO 00b	**Type (TP):** Indicates that this range can be mapped anywhere in 32-bit address space.
0	RO 0b	**Resource Type Indicator (RTE):** Indicates a request for register memory space.

9.4.11 SS—Sub System Identifiers

B/D/F/Type: 0/3/3/PCI
Address Offset: 2C–2Fh
Default Value: 00008086h
Access: RWO
Size: 32 bits

This registers are used to uniquely identify the add-in card or the subsystem that the device resides within.

Note: Reset: Host system Reset.

Bit	Access & Default	Description
31:16	RWO 0000h	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken on this value.
15:0	RWO 8086h	**Subsystem Vendor ID (SSVID):** This is written by BIOS. No hardware action taken on this value.

9.4.12 EROM—Expansion ROM Base Address

B/D/F/Type: 0/3/3/PCI
Address Offset: 30–33h
Default Value: 00000000h
Access: RO
Size: 32 bits

This optional register is not implemented.

Bit	Access & Default	Description
31:11	RO 000000h	**Expansion ROM Base Address (ERBAR):**
10:1	RO 000h	Reserved
0	RO 0b	**Enable (EN):** Enable expansion ROM Access

9.4.13 CAP—Capabilities Pointer

B/D/F/Type: 0/3/3/PCI
Address Offset: 34h
Default Value: C8h
Access: RO
Size: 8 bits

This optional register is used to point to a linked list of new capabilities implemented by the device.

Bit	Access & Default	Description
7:0	RO C8h	**Capability Pointer (CP):** This field indicates that the first capability pointer offset is offset c8h (the power management capability)

9.4.14 INTR—Interrupt Information

B/D/F/Type: 0/3/3/PCI
Address Offset: 3C–3Dh
Default Value: 0200h
Access: RW, RO
Size: 16 bits

See individual Registers below.

Note: Reset: Host System Reset or D3->D0 reset of the function.

Bit	Access & Default	Description
15:8	RO 02h	**Interrupt Pin (IPIN):** a value of 0x1/0x2/0x3/0x4 indicates that this function implements legacy interrupt on INTA/INTB/INTC/INTD, respectively **Function** **Value** **INTx** (3 KT/Serial Port) 02h INTB
7:0	RW 00h	**Interrupt Line (ILINE):** The value written in this field indicates which input of the system interrupt controller, the device's interrupt pin is connected to. This value is used by the OS and the device driver, and has no affect on the hardware.

9.4.15 MGNT—Minimum Grant

B/D/F/Type: 0/3/3/PCI
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

This optional register is not implemented.

Bit	Access & Default	Description
7:0	RO 00h	Reserved

9.4.16 MLAT—Maximum Latency

B/D/F/Type: 0/3/3/PCI
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

This optional register is not implemented.

Bit	Access & Default	Description
7:0	RO 00h	Reserved

9.4.17 PID—PCI Power Management Capability ID

B/D/F/Type: 0/3/3/PCI
Address Offset: C8–C9h
Default Value: D001h
Access: RO
Size: 16 bits

See register definitions below.

Bit	Access & Default	Description
15:8	RO D0h	**Next Capability (NEXT):** The value of D0h points to the MSI capability
7:0	RO 01h	**Cap ID (CID):** This field indicates that this pointer is a PCI power management

9.4.18 PC—PCI Power Management Capabilities

B/D/F/Type: 0/3/3/PCI
Address Offset: CA–CBh
Default Value: 0023h
Access: RO
Size: 16 bits

This register implements the power management capabilities of the function.

Bit	Access & Default	Description
15:11	RO 00000b	**PME Support (PME):** Indicates no PME# in the PT function.
10	RO 0b	**D2 Support (D2S):** The D2 state is not Supported.
9	RO 0b	**D1 Support (D1S):** The D1 state is not supported.
8:6	RO 000b	**Aux Current (AUXC):** PME# from D3 (cold) state is not supported; therefore, this field is 000b.
5	RO 1b	**Device Specific Initialization (DSI):** Indicates that no device-specific initialization is required.
4	RO 0b	Reserved
3	RO 0b	**PME Clock (PMEC):** Indicates that PCI clock is not required to generate PME#.
2:0	RO 011b	**Version (VS):** Indicates support for revision 1.2 of the PCI power management specification.

9.4.19 PMCS—PCI Power Management Control and Status

B/D/F/Type:	0/3/3/PCI
Address Offset:	CC–CFh
Default Value:	00000000h
Access:	RO/V, RO, RW
Size:	32 bits
BIOS Optimal Default	0000h

This register implements the PCI PM Control and Status Register to allow PM state transitions and Wake up.

Note: Note the NSR bit of this register. All registers (PCI configuration and Device Specific) marked with D3->D0 transition reset will only do so if this bit reads a 0. If this bit is a 1, the D3->D0 transition will not reset the registers.

Note: Reset: Host System Reset or D3->D0 transition.

Bit	Access & Default	Description
31:16	RO 0h	Reserved
15	RO 0b	**PME Status (PMES):** This bit is set when a PME event is to be requested. Not supported
14:9	RO 00h	Reserved
8	RO 0b	**PME Enable (PMEE):** Not Supported
7:4	RO 0h	Reserved
3	RO/V 0b	**No Soft Reset (NSR):** 1 = Indicates that devices transitioning from D3hot to D0 because of PowerState commands do not perform an internal reset. Configuration Context is preserved. Upon transition from the D3hot to the D0 Initialized state, no additional operating system intervention is required to preserve Configuration Context beyond writing the PowerState bits. 0 = Devices do perform an internal reset upon transitioning from D3hot to D0 via software control of the PowerState bits. Configuration Context is lost when performing the soft reset. Upon transition from the D3hot to the D0 state, full re-initialization sequence is needed to return the device to D0 Initialized. When this bit is 0, device performs internal reset. When this bit is 1, device does not perform internal reset.
2	RO 0b	Reserved

Bit	Access & Default	Description
1:0	RW 00b	**Power State (PS):** This field is used both to determine the current power state of the PT function and to set a new power state. 00 = D0 state 11 = $D3_{HOT}$ state When in the $D3_{HOT}$ state, the controller's configuration space is available, but the I/O and memory spaces are not. Additionally, interrupts are blocked. If software attempts to write a 10 or 01 to these bits, the write will be ignored.

9.4.20 MID—Message Signaled Interrupt Capability ID

B/D/F/Type: 0/3/3/PCI
Address Offset: D0–D1h
Default Value: 0005h
Access: RO
Size: 16 bits

Message Signaled Interrupt is a feature that allows the device/function to generate an interrupt to the host by performing a DWORD memory write to a system specified address with system specified data. This register is used to identify and configure an MSI capable device.

Bit	Access & Default	Description
15:8	RO 00h	**Next Pointer (NEXT):** Value indicates this is the last item in the list.
7:0	RO 05h	**Capability ID (CID):** value of Capabilities ID indicates device is capable of generating MSI.

9.4.21 MC—Message Signaled Interrupt Message Control

B/D/F/Type: 0/3/3/PCI
Address Offset: D2–D3h
Default Value: 0080h
Access: RO, RW
Size: 16 bits

This register provides System Software control over MSI.

Note: Reset: Host System Reset or D3->D0 transition.

Bit	Access & Default	Description
15:8	RO 00h	Reserved
7	RO 1b	**64 Bit Address Capable (C64):** Capable of generating 64-bit and 32-bit messages.
6:4	RW 000b	**Multiple Message Enable (MME):** These bits are R/W for software compatibility, but only one message is ever sent by the PT function.
3:1	RO 000b	**Multiple Message Capable (MMC):** Only one message is required.
0	RW 0b	**MSI Enable (MSIE):** 0 = Disable. 1 = Enable. Traditional interrupt pins are not used to generate interrupts.

9.4.22 MA—Message Signaled Interrupt Message Address

B/D/F/Type: 0/3/3/PCI
Address Offset: D4–D7h
Default Value: 00000000h
Access: RO, RW
Size: 32 bits

This register specifies the DWord aligned address programmed by system software for sending MSI.

Note: Reset: Host system Reset or D3->D0 transition.

Bit	Access & Default	Description
31:2	RW 00000000h	**Address (ADDR):** This field provides the lower 32 bits of the system specified message address, always DWord aligned. Force host MSI address to 0_FEEx_XXXXh before sending to backbone, regardless of values programmed in MA and MUA registers under respective PCI Configuration Space. Note that the MA and MUA registers should continued to be RW (no change to registers implementation, just hardcode 0_FEE as bit[35:20] for MSI cycles to backbone).
1:0	RO 00b	Reserved

9.4.23 MAU—Message Signaled Interrupt Message Upper Address

B/D/F/Type: 0/3/3/PCI
Address Offset: D8–DBh
Default Value: 00000000h
Access: RO, RW
Size: 32 bits

This register provides the upper 32 bits of the message address for the 64bit address capable device.

Note: Reset: Host system Reset or D3->D0 transition.

Bit	Access & Default	Description
31:4	RO 0000000h	Reserved
3:0	RW 0000b	**Address (ADDR):** This field provides the upper 4 bits of the system specified message address.

9.4.24 MD—Message Signaled Interrupt Message Data

B/D/F/Type:	0/3/3/PCI
Address Offset:	DC–DDh
Default Value:	0000h
Access:	RW
Size:	16 bits

This 16-bit field is programmed by system software if MSI is enabled.

Note: Reset: Host system Reset or D3->D0 transition.

Bit	Access & Default	Description
15:0	RW 0000h	**Data (DATA):** This MSI data is driven onto the lower word of the data bus of the MSI memory write transaction.

10 Functional Description

10.1 Host Interface

The (G)MCH supports the Intel® Core™2 Duo desktop processor subset of the Enhanced Mode Scaleable Bus. The cache line size is 64 bytes. Source synchronous transfer is used for the address and data signals. The address signals are double pumped and a new address can be generated every other bus clock. At 200/267/333 MHz bus clock the address signals run at 667 MT/s. The data is quad pumped and an entire 64B cache line can be transferred in two bus clocks. At 200/266/333 MHz bus clock, the data signals run at 800/1066/1333 MT/s for a maximum bandwidth of 6.4/8.5/10.6 GB/s.

10.1.1 FSB IOQ Depth

The Scalable Bus supports up to 12 simultaneous outstanding transactions.

10.1.2 FSB OOQ Depth

The (G)MCH supports only one outstanding deferred transaction on the FSB.

10.1.3 FSB GTL+ Termination

The (G)MCH integrates GTL+ termination resistors on die.

10.1.4 FSB Dynamic Bus Inversion

The (G)MCH supports Dynamic Bus Inversion (DBI) when driving and when receiving data from the processor. DBI limits the number of data signals that are driven to a low voltage on each quad pumped data phase. This decreases the worst-case power consumption of the (G)MCH. FSB_DINVB_3:0 indicate if the corresponding 16 bits of data are inverted on the bus for each quad pumped data phase.

FSB_DINVB_3:0	Data Bits
FSB_DINVB_0	FSB_DB_15:0
FSB_DINVB_1	FSB_DB_31:16
FSB_DINVB_2	FSB_DB_47:32
FSB_DINVB_3	FSB_DB_63:48

When the processor or the (G)MCH drives data, each 16-bit segment is analyzed. If more than 8 of the 16 signals would normally be driven low on the bus, the corresponding HDINV# signal will be asserted, and the data will be inverted prior to being driven on the bus. Whenever the processor or the (G)MCH receives data, it monitors FSB_DINVB_3:0 to determine if the corresponding data segment should be inverted.

10.1.4.1 APIC Cluster Mode Support

APIC Cluster mode support is required for backwards compatibility with existing software, including various operating systems. As one example, beginning with Microsoft Windows 2000, there is a mode (boot.ini) that allows an end user to enable the use of cluster addressing support of the APIC.

- The (G)MCH supports three types of interrupt re-direction:
  - Physical
  - Flat-Logical
  - Clustered-Logical

10.2 System Memory Controller

The 82G33 GMCH and 82P35 MCH system memory controllers support both DDR2 and DDR3 protocols with two independent 64 bit wide channels; each accessing one or two DIMMs. The (G)MCH supports a maximum of two un-buffered, non-ECC DDR2 or DDR3 DIMMs per channel; thus, allowing up to four device ranks per channel. The 82Q35 GMCH and 82Q33 GMCH only support DDR2.

Note: References in this section to DDR3 are for the 82G33 GMCH and 82P35 only.

10.2.1 System Memory Organization Modes

The system memory controller supports three memory organization modes, Single Channel, Dual Channel Symmetric, and Dual Channel Asymmetric.

10.2.2 Single Channel Mode

In this mode, all memory cycles are directed to a single channel. Single channel mode is used when either Channel A or Channel B DIMMs are populated in any order, but not both.

10.2.3 Dual Channel Symmetric Mode

This mode provides maximum performance on real applications. Addresses are ping-ponged between the channels after each cache line (64 byte boundary). If there are two requests, and the second request is to an address on the opposite channel from the first, that request can be sent before data from the first request has returned. If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are ensured to be on opposite channels.

Dual channel symmetric mode is used when both Channel A and Channel B DIMMs are populated in any order with the total amount of memory in each channel being the same, but the DRAM device technology and width may vary from one channel to the other.

Table 10-1 is a sample dual channel symmetric memory configuration showing the rank organization.

Table 10-1. Sample System Memory Dual Channel Symmetric Organization Mode with Intel® Flex Memory Mode Enabled

Rank	Channel 0 population	Cumulative top address in Channel 0	Channel 1 population	Cumulative top address in Channel 1
Rank 3	0 MB	2560 MB	0 MB	2560 MB
Rank 2	256 MB	2560 MB	256 MB	2560 MB
Rank 1	512 MB	2048 MB	512 MB	2048 MB
Rank 0	512 MB	1024 MB	512 MB	1024 MB

10.2.4 Dual Channel Asymmetric Mode with Intel® Flex Memory Mode Enabled

This mode trades performance for system design flexibility. Unlike the previous mode, addresses start in channel 0 and stay there until the end of the highest rank in channel 0, and then addresses continue from the bottom of channel 1 to the top. Normal applications are unlikely to make requests that alternate between addresses that are on opposite channels with this memory organization; so, in most cases, bandwidth will be limited to that of a single channel.

Dual channel asymmetric mode is used when both Channel A and Channel B DIMMs are populated in any order with the total amount of memory in each channel being different.

Table 10-2 is a sample dual channel asymmetric memory configuration showing the rank organization:

Table 10-2. Sample System Memory Dual Channel Asymmetric Organization Mode with Intel® Flex Memory Mode Disabled

Rank	Channel 0 population	Cumulative top address in Channel 0	Channel 1 population	Cumulative top address in Channel 1
Rank 3	0 MB	1280 MB	0 MB	2304 MB
Rank 2	256 MB	1280 MB	0 MB	2304 MB
Rank 1	512 MB	1024 MB	512 MB	2304 MB
Rank 0	512 MB	512 MB	512 MB	1792 MB

10.2.5 System Memory Technology Supported

The (G)MCH supports the following DDR2 and DDR3 Data Transfer Rates, DIMM Modules, and DRAM Device Technologies:

- DDR2 Data Transfer Rates: 667 (PC2-5300) and 800 (PC2-6400)
- DDR3 Data Transfer Rates: 800 (PC3-6400) and 1066 (PC3-8500)
- DDR2 DIMM Modules:
  - Raw Card C - Single Sided x16 un-buffered non-ECC
  - Raw Card D - Single Sided x8 un-buffered non-ECC
  - Raw Card E - Double Sided x8 un-buffered non-ECC
- DDR3 DIMM Modules:
  - Raw Card A - Single Sided x8 un-buffered non-ECC
  - Raw Card B - Double Sided x8 un-buffered non-ECC
  - Raw Card C - Single Sided x16 un-buffered non-ECC
  - Raw Card F - Double Sided x16 un-buffered non-ECC
- DDR2 and DDR3 DRAM Device Technology: 512 MB and 1 GB

Table 10-3 Supported DIMM Module Configurations

Memory Type	Raw Card Version	DIMM Capacity	DRAM Device Technology	DRAM Organization	# of DRAM Devices	# of Physical Device Ranks	# of Row/Col Address Bits	# of Banks Inside DRAM	Page Size
DDR2 667 and 800	C	256 MB	512 Mb	32M X 16	4	1	13/10	4	8K
		512 MB	1 Gb	64M X 16	4	1	13/10	8	8K
	D	512 MB	512 Mb	64M X 8	8	1	14/10	4	8K
		1 GB	1 Gb	128M X 8	8	1	14/10	8	8K
	E	1 GB	512 Mb	64M X 8	16	2	14/10	4	8K
		2 GB	1 Gb	128M X 8	16	2	14/10	8	8K
DDR3 800 and 1066	A	512 MB	512 Mb	64M X 8	8	1	13/10	8	8K
		1 GB	1 Gb	128M X 8	8	1	14/10	8	8K
	B	1 GB	512 Mb	64M X 8	16	2	13/10	8	8K
		2 GB	1 Gb	128M X 8	16	2	14/10	8	8K
	C	256 MB	512 Mb	32M X 16	4	1	12/10	8	8K
		512 MB	1 Gb	64M X 16	4	1	13/10	8	8K
	F	512 MB	512 Mb	32M X 16	8	2	12/10	8	8K
		1 GB	1 Gb	64M X 16	8	2	13/10	8	8K

10.3 PCI Express*

See Section 1.3.4 for list of PCI Express features, and the PCI Express specification for further details.

This (G)MCH is part of a PCI Express root complex. This means it connects a host processor/memory subsystem to a PCI Express hierarchy. The control registers for this functionality are located in device 1 configuration space and two Root Complex Register Blocks (RCRBs). The DMI RCRB contains registers for control of the ICH9 attach ports.

10.3.1 PCI Express* Architecture

The PCI Express architecture is specified in layers. Compatibility with the PCI addressing model (a load-store architecture with a flat address space) is maintained to ensure that all existing applications and drivers operate unchanged. The PCI Express configuration uses standard mechanisms as defined in the PCI Plug-and-Play specification. The initial speed of 1.25 GHz (250 MHz internally) results in 2.5 GB/s/direction which provides a 250 MB/s communications channel in each direction (500 MB/s total) that is close to twice the data rate of classic PCI per lane.

10.3.2 Transaction Layer

The upper layer of the PCI Express architecture is the Transaction Layer. The Transaction Layer's primary responsibility is the assembly and disassembly of Transaction Layer Packets (TLPs). TLPs are used to communicate transactions, such as read and write, as well as certain types of events. The Transaction Layer also manages flow control of TLPs.

10.3.3 Data Link Layer

The middle layer in the PCI Express stack, the Data Link Layer, serves as an intermediate stage between the Transaction Layer and the Physical Layer. Responsibilities of Data Link Layer include link management, error detection, and error correction.

10.3.4 Physical Layer

The Physical Layer includes all circuitry for interface operation, including driver and input buffers, parallel-to-serial and serial-to-parallel conversion, PLL(s), and impedance matching circuitry.

10.4 Intel® Serial Digital Video Output (SDVO) (Intel® 82Q35, 82Q33, 82G33 GMCH Only)

The SDVO signals on the GMCH are multiplexed with the PCI Express x16 port pins. The Intel® SDVO Port is the second generation of digital video output from compliant Intel® GMCHs. The electrical interface is based on the PCI Express interface, though the protocol and timings are completely unique. Whereas PCI Express runs at a fixed frequency, the frequency of the SDVO interface is dependant upon the active display resolution and timing. The port can be dynamically configured in several modes to support display configurations.

Essentially, an SDVO port will transmit display data in a high speed, serial format across differential AC coupled signals. An SDVO port consists of a sideband differential clock pair and a number of differential data pairs.

10.4.1 Intel® SDVO Capabilities

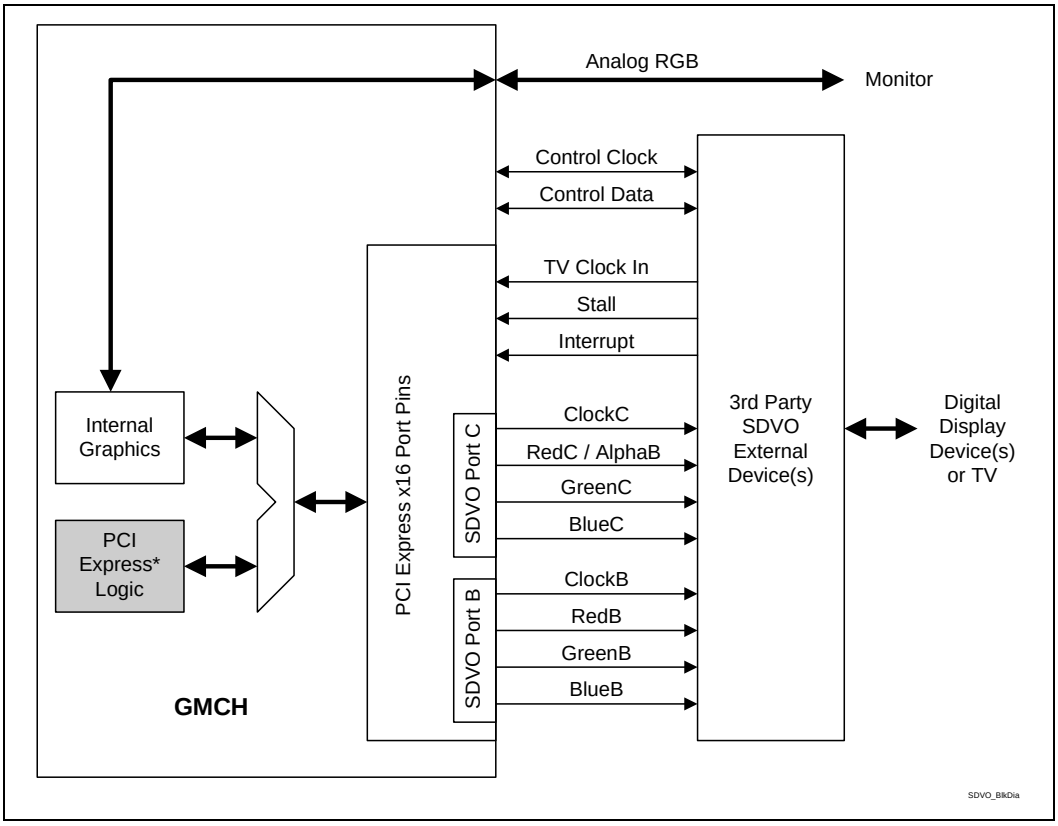
SDVO ports can support a variety of display types including LVDS, DVI, Analog CRT, TV-Out and external CE type devices. The GMCH uses an external SDVO device to translate from SDVO protocol and timings to the desired display format and timings.

The Internal Graphics Controller can have one or two SDVO ports multiplexed on the x16 PCI Express interface. When an external x16 PCI Express graphics accelerator is not in use, an ADD2 card may be plugged into the x16 connector or if a x16 slot is not present, the SDVO(s) may be located ‘down’ on the motherboard to access the multiplexed SDVO ports and provide a variety of digital display options.

The ADD2/Media Expansion card is designed to fit in a x16 PCI Express connector. The ADD2/Media Expansion card can support one or two devices. If a single channel SDVO device is used, it should be attached to the channel B SDVO pins. The ADD2 card can support two separate SDVO devices when the interface is in Dual Independent or Dual Simultaneous Standard modes. The Media Expansion card adds Video in capabilities.

The SDVO port defines a two-wire point-to-point communication path between the SDVO device and GMCH. The SDVO control clock and data provide similar functionality to I^2C. However unlike I^2C, this interface is intended to be point-to-point (from the GMCH to the SDVO device) and requires the SDVO device to act as a switch and direct traffic from the SDVO control bus to the appropriate receiver. Additionally, this control bus will be able to run at faster speeds (up to 1 MHz) than a traditional I^2C interface would.

Figure 10-1. sDVO Conceptual Block Diagram



10.4.2 Intel® SDVO Modes

The port can be dynamically configured in several modes:

- **Standard**. This mode provides baseline SDVO functionality. It supports Pixel Rates between 25 MP/s and 225 MP/s. It uses three data pairs to transfer RGB data.
- **Dual Standard**. This mode uses Standard data streams across both SDVOB and SDVOC. Both channels can only run in Standard mode (3 data pairs) and each channel supports Pixel Rates between 25 MP/s and 225 MP/s.
  - Dual Independent Standard. In Dual Independent Standard mode, each SDVO channel sees a different pixel stream. The data stream across SDVOB is not the same as the data stream across SDVOC.
  - Dual Simultaneous Standard. In Dual Simultaneous Standard mode, both SDVO channels see the same pixel stream. The data stream across SDVOB is the same as the data stream across SDVOC. The display timings will be identical, but the transfer timings may not be (i.e., SDVOB clocks and data may not be perfectly aligned with SDVOC clock and data as seen at the SDVO device(s)). Since this mode uses just a single data stream, it uses a single pixel pipeline within the GMCH.

10.4.3 PCI Express* and Internal Graphics Simultaneous Operation

10.4.3.1 Standard PCI Express* Cards and Internal Graphics

BIOS control of simultaneous operation is needed to ensure the PCI Express is configured appropriately.

10.4.3.2 Media Expansion Cards (Concurrent SDVO and PCI Express*)

SDVO lane reversal is supported in the (G)MCH. This functionality allows current SDVO ADD2 cards to work in current ATX and BTX systems instead of requiring a separate card. The GMCH allows SDVO and PCI Express to operate concurrently on the PCI Express Port. The card, which plugs into the x16 connector in this case, is called a Media Expansion card. It uses 4 or 8 lanes for SDVO and up to 8 lanes of standard PCI Express.

For the GMCH, the only supported PCI Express width when SDVO is present is x1.

This concurrency is supported in reversed and non-reversed configurations. Mirroring / Reversing is always about the axis.

Table 10-4. Concurrent SDVO / PCI Express* Configuration Strap Controls

Configuration #	Description	Slot Reversed Strap	SDVO Present Strap	SDVO/PCI Express* Concurrent Strap
1	PCI Express* not reversed	—	—	—
2	PCI Express* Reversed	Yes	—	—
3	SDVO (ADD2) not reversed	—	Yes	—
4	SDVO (ADD2) Reversed	Yes	Yes	—
5	SDVO & PCI Express* (MEDIA EXPANSION) not reversed	—	Yes	Yes
6	SDVO & PCI Express* (MEDIA EXPANSION) Reversed	Yes	Yes	Yes

Notes:
1. The Configuration #s refer to the following figures (no intentional relation to validation configurations).
2. Configurations 4, 5, and 6 (required addition of SDVO/PCI Express* Concurrent Strap).

Figure 10-2. Concurrent savon / PCI Express* Non-Reversed Configurations

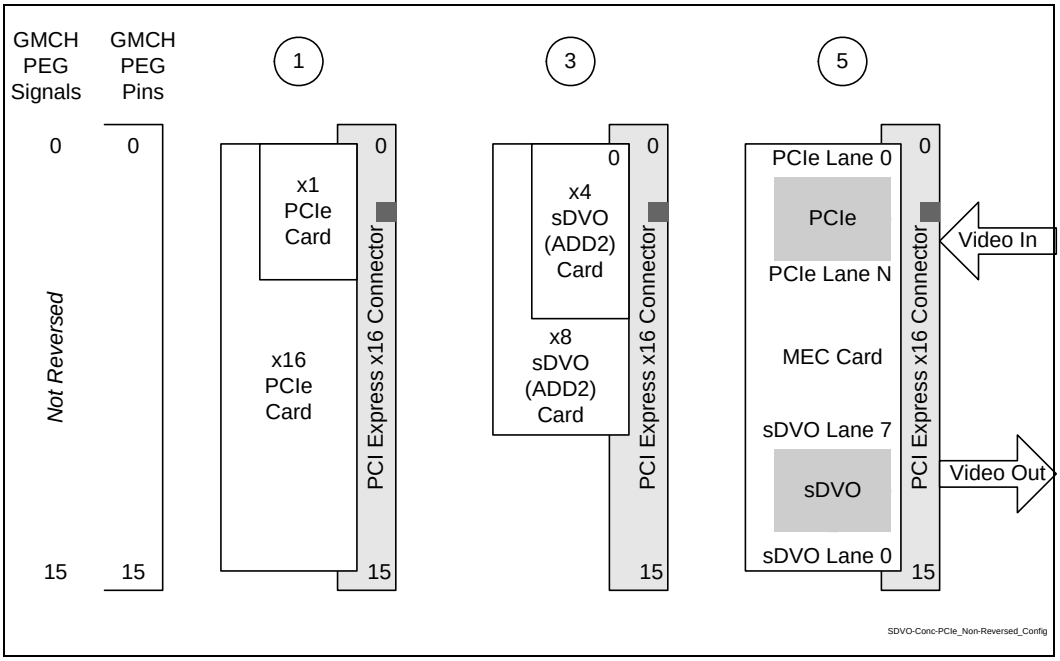
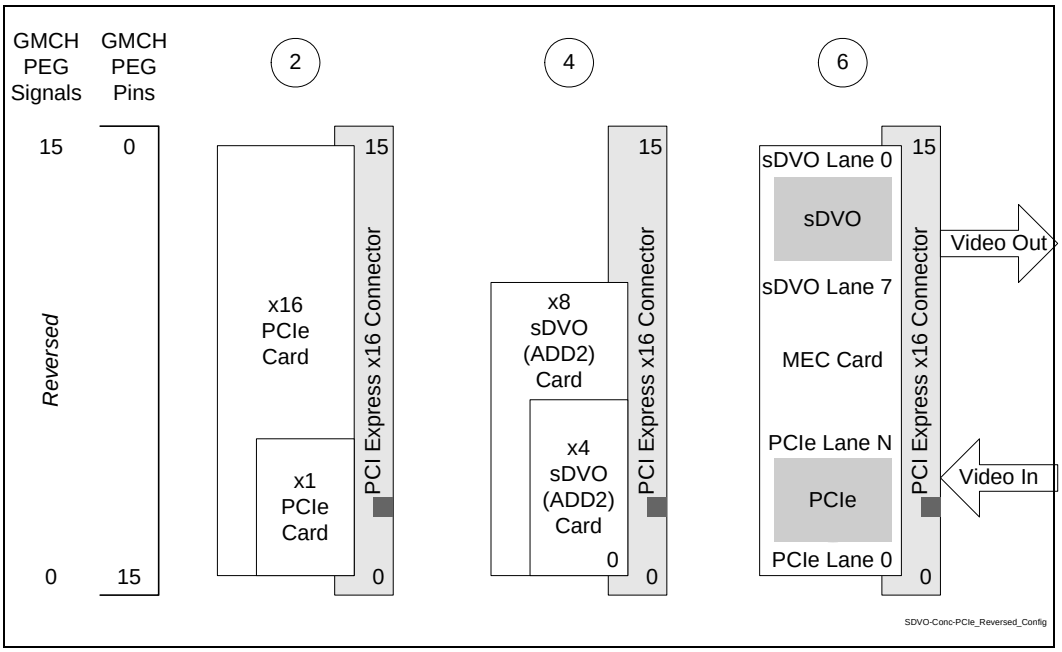


Figure 10-3. Concurrent SDVO / PCI Express* Reversed Configurations



10.5 Integrated Graphics Controller (Intel® 82Q35, 82Q33, 82G33 GMCH Only)

The major components in the Integrated Graphics Device (IGD) are the engines, planes, pipes, and ports. The GMCH has a 3D/2D instruction processing unit to control the 3D and 2D engines. The IGD's 3D and 2D engines are fed with data through the memory controller. The output of the engines are surfaces sent to memory that are then retrieved and processed by the GMCH planes.

The GMCH contains a variety of planes, such as display, overlay, cursor and VGA. A plane consists of rectangular shaped image that has characteristics such as source, size, position, method, and format. These planes get attached to source surfaces that are rectangular memory surfaces with a similar set of characteristics. They are also associated with a particular destination pipe.

A pipe consists of a set of combined planes and a timing generator. The GMCH has two independent display pipes, allowing for support of two independent display streams. A port is the destination for the result of the pipe. The GMCH contains three display ports; 1 analog (DAC) and two digital (SDVO ports B and C). The ports will be explained in more detail later in this chapter.

The entire IGD is fed with data from its memory controller. The GMCH's graphics performance is directly related to the amount of bandwidth available. If the engines are not receiving data fast enough from the memory controller (e.g., single-channel DDR3 1066), the rest of the IGD will also be affected.

The rest of this chapter will focus on explaining the IGD components, their limitations, and dependencies.

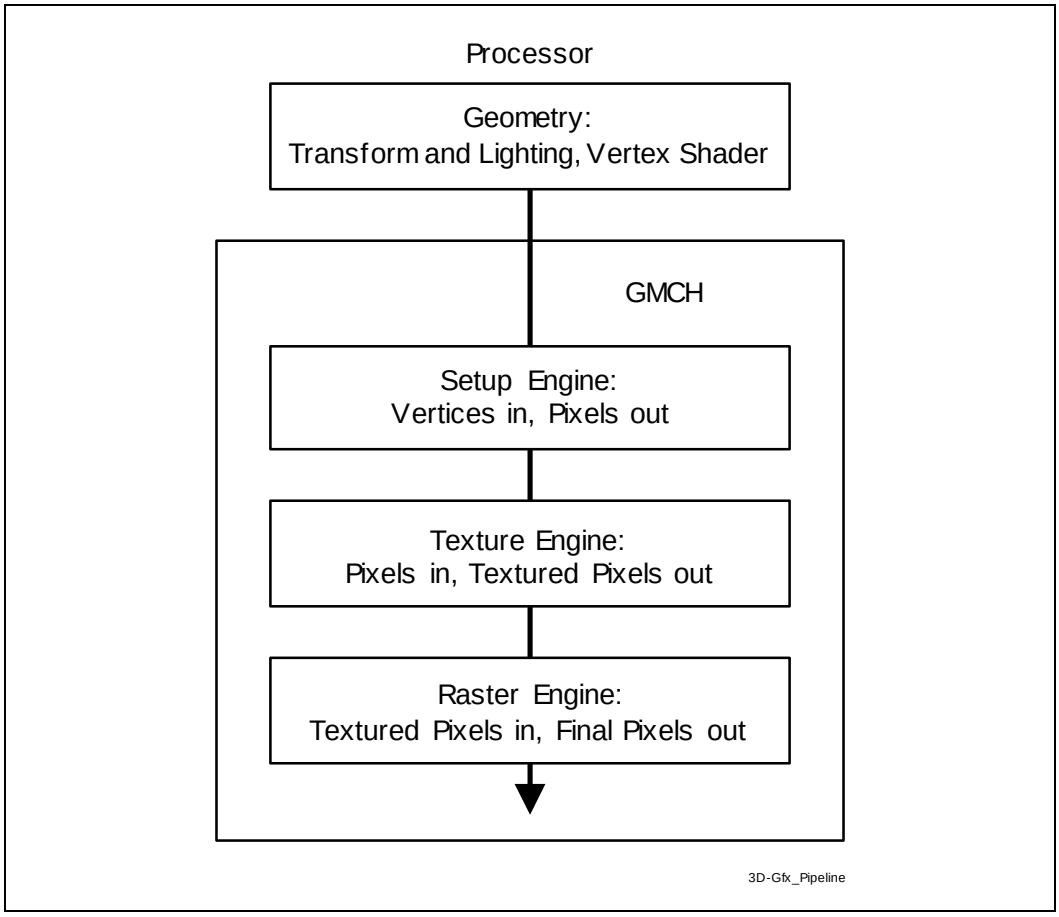
10.5.1 3D Graphics Pipeline

The GMCH graphics is the next step in the evolution of integrated graphics. In addition to running the graphics engine at 400 MHz, the GMCH graphics has two pixel pipelines that provide a 1.3 GB/s fill rate that enables an excellent consumer gaming experience.

The 3D graphics pipeline for the GMCH has a deep pipelined architecture in which each stage can simultaneously operate on different primitives or on different portions of the same primitive. The 3D graphics pipeline is divided into four major stages: geometry processing, setup (vertex processing), texture application, and rasterization.

The GMCH graphics is optimized for use with current and future Intel® processors for advance software based transform and lighting techniques (geometry processing) as defined by the Microsoft DirectX* API. The other three stages of 3D processing are handled on the integrated graphics device. The setup stage is responsible for vertex processing; converting vertices to pixels. The texture application stage applies textures to pixels. The rasterization engine takes textured pixels and applies lighting and other environmental affects to produce the final pixel value. From the rasterization stage, the final pixel value is written to the frame buffer in memory so it can be displayed.

Figure 10-4. Integrated 3D Graphics Pipeline



10.5.2 3D Engine

The 3D engine on the GMCH has been designed with a deep pipelined architecture, where performance is maximized by allowing each stage of the pipeline to simultaneously operate on different primitives or portions of the same primitive. The GMCH supports Perspective-Correct Texture Mapping, Multitextures, Bump-Mapping, Cubic Environment Maps, Bilinear, Trilinear and Anisotropic MIP mapped filtering, Gouraud shading, Alpha-blending, Vertex, and Per Pixel Fog and Z/W Buffering.

The 3D pipeline subsystem performs the 3D rendering acceleration. The main blocks of the pipeline are the setup engine, scan converter, texture pipeline, and raster pipeline. A typical programming sequence would be to send instructions to set the state of the pipeline followed by rending instructions containing 3D primitive vertex data.

The engines' performance is dependent on the memory bandwidth available. Systems that have more bandwidth available will outperform systems with less bandwidth. The engines' performance is also dependent on the core clock frequency. The higher the frequency, the more data is processed.

10.5.3 Texture Engine

The GMCH allows an image, pattern, or video to be placed on the surface of a 3D polygon. The texture processor receives the texture coordinate information from the setup engine and the texture blend information from the scan converter. The texture processor performs texture color or ChromaKey matching, texture filtering (anisotropic, trilinear, and bilinear interpolation), and YUV-to-RGB conversions.

10.5.4 Raster Engine

The raster engine is where the color data (such as, fogging, specular RGB, texture map blending, etc.) is processed. The final color of the pixel is calculated and the RGBA value combined with the corresponding components resulting from the texture engine. These textured pixels are modified by the specular and fog parameters. These specular highlighted, fogged, textured pixels are color blended with the existing values in the frame buffer. In parallel, stencil, alpha, and depth buffer tests are conducted that determine whether the frame and depth buffers will be updated with the new pixel values.

10.6 Display Interfaces (Intel® 82Q35, 82Q33, 82G33 Only GMCH)

The GMCH have three display ports; one analog and two digital. Each port can transmit data according to one or more protocols. The digital ports are connected to an external device that converts one protocol to another. Examples of these are TV encoders, external DACs, LVDS transmitters, HDMI transmitters, and TMDS transmitters. Each display port has control signals that may be used to control, configure and/or determine the capabilities of an external device.

The GMCH has one dedicated display port, the analog port. SDVO ports B and C are multiplexed with the PCI Express Graphics (PEG) interface and are not available if an external PEG device is in use. When a system uses a PEG connector, SDVO ports B and C can be used via an ADD2 (Advanced Digital Display 2) or MEC (Media Expansion Card).

- The (G)MCH's analog port uses an integrated 350 MHz RAMDAC that can directly drive a standard progressive scan analog monitor up to a resolution of 2048x1536 pixels with 32-bit color at 75 Hz.
- The GMCH's SDVO ports are each capable of driving a 225MP pixel rate. Each port is capable of driving a digital display up to 1920x1200 @ 60Hz.

The GMCH is compliant with DVI Specification 1.0. When combined with a DVI compliant external device and connector, the GMCH has a high speed interface to a digital display (e.g., flat panel or digital CRT).

The GMCH is compliant with HDMI. When combined with a HDMI compliant external device and connector, the external HDMI device can supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable.

10.6.1 Analog Display Port Characteristics

The analog display port provides a RGB signal output along with a HSYNC and VSYNC signal. There is an associated DDC signal pair that is implemented using GPIO pins dedicated to the analog port. The intended target device is for a CRT based monitor with a VGA connector. Display devices such as LCD panels with analog inputs may work satisfactory but no functionality added to the signals to enhance that capability.

Table 10-1. Analog Port Characteristics

Signal	Port Characteristic	Support
RGB	Voltage Range	0.7 V p-p only
	Monitor Sense	Analog Compare
	Analog Copy Protection	No
	Sync on Green	No
HSYNC VSYNC	Voltage	2.5 V
	Enable/Disable	Port control
	Polarity adjust	VGA or port control
	Composite Sync Support	No
	Special Flat Panel Sync	No
	Stereo Sync	No
DDC	Voltage	Externally buffered to 5 V
	Control	Through GPIO interface

10.6.1.1 Integrated RAMDAC

The display function contains a RAM-based Digital-to-Analog Converter (RAMDAC) that transforms the digital data from the graphics and video subsystems to analog data for the CRT monitor. The GMCH's integrated 350 MHz RAMDAC supports resolutions up to 2048 x 1536 @ 75 Hz. Three 8-bit DACs provide the R, G, and B signals to the monitor.

10.6.1.2 Sync Signals

HSYNC and VSYNC signals are digital and conform to TTL signal levels at the connector. Since these levels cannot be generated internal to the device, external level shifting buffers are required. These signals can be polarity adjusted and individually disabled in one of the two possible states. The sync signals should power up disabled in the high state. No composite sync or special flat panel sync support will be included.

10.6.1.3 VESA / VGA Mode

VESA/VGA mode provides compatibility for pre-existing software that set the display mode using the VGA CRTC registers. Timings are generated based on the VGA register values and the timing generator registers are not used.

10.6.1.4 DDC (Display Data Channel)

DDC is a standard defined by VESA. Its purpose is to allow communication between the host system and display. Both configuration and control information can be exchanged allowing plug- and-play systems to be realized. Support for DDC 1 and 2 is implemented. The GMCH uses the DDC_CLK and DDC_DATA signals to communicate with the analog monitor. The GMCH generates these signals at 2.5 V. External pull-up resistors and level shifting circuitry should be implemented on the board.

The GMCH implements a hardware GMBus controller that can be used to control these signals allowing for transactions speeds up to 400 kHz.

10.6.2 Digital Display Interface

The GMCH has several options for driving digital displays. The GMCH contains two SDVO ports that are multiplexed on the PEG interface. When an external PEG graphics accelerator is not present, the GMCH can use the multiplexed SDVO ports to provide extra digital display options. These additional digital display capabilities may be provided through an ADD2/Media Expansion Card, which is designed to plug in to a PCI Express connector.

10.6.2.1 Multiplexed Digital Display Channels – Intel® SDVOB and Intel® SDVOC

The GMCH has the capability to support digital display devices through two SDVO ports multiplexed with the PEG signals. When an external graphics accelerator is used via the PEG port, these SDVO ports are not available.

The shared SDVO ports each support a pixel clock up to 200 MHz and can support a variety of transmission devices.

SDVOCTRLDATA is an open-drain signal that will act as a strap during reset to tell the GMCH whether the interface is a PCI Express interface or an SDVO interface. When implementing SDVO, either via ADD2 cards or with a down device, a pull-up is placed on this line to signal to the GMCH to run in SDVO mode and for proper GMBus operation.

10.6.2.2 ADD2/Media Expansion Card (MEC)

When an Intel® 3 Series Express Chipset platform uses a PEG connector, the multiplexed SDVO ports may be used via an ADD2 or MEC card. The ADD2 card will be designed to fit a standard PCI Express (x16) connector.

10.6.2.3 TMDS Capabilities

The GMCH is compliant with DVI Specification 1.0. When combined with a DVI compliant external device and connector, the GMCH has a high speed interface to a digital display (e.g., flat panel or digital CRT). The GMCH can drive a flat panel up to 1920x1200 or a dCRT/HDTV up to 1400x1050. Flat Panel is a fixed resolution display. The GMCH supports panel fitting in the transmitter, receiver, or an external device, but has no native panel fitting capabilities. The GMCH will however, provide unscaled mode where the display is centered on the panel.

10.6.2.4 HDMI Capabilities

The GMCH is compliant with HDMI. When combined with a HDMI compliant external device and connector, the external HDMI device can support standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable. The GMCH has a high speed interface to a digital display (e.g., flat panel or digital TV). The GMCH can drive a digital TV up to 1600x1200.

10.6.2.5 LVDS Capabilities

The GMCH may use the multiplexed SDVO ports to drive an LVDS transmitter. Flat Panel is a fixed resolution display. The GMCH supports panel fitting in the transmitter, receiver or an external device, but has no native panel fitting capabilities. The GMCH will however, provide unscaled mode where the display is centered on the panel. The GMCH supports scaling in the LVDS transmitter through the SDVO stall input pair.

10.6.2.6 TV-IN Capabilities

The GMCH in conjunction with ADD2/Media Expansion Card can function as a TV-Tuner card capable of taking in both analog or HD signals.

10.6.2.7 TV-Out Capabilities

Although traditional TVs are not digital displays, the GMCH uses a digital display channel to communicate with a TV-Out transmitter. For that reason, the GMCH considers a TV-Output to be a digital display. The GMCH supports NTSC/PAL/SECAM standard definition formats. The GMCH will generate the proper timing for the external encoder. The external encoder is responsible for generation of the proper format signal. Since the multiplexed SDVO interface is a NTSC/PAL/SECAM display on the TV-out port can be configured to be the boot device. It is necessary to ensure that appropriate BIOS support is provided. If EasyLink is supported in the GMCH, then this mechanism could be used to interrogate the display device.

The TV-out interface on GMCH allows an external TV encoder device to drive a pixel clock signal on SDVO_TVClk[+/-] that the GMCH uses as a reference frequency. The frequency of this clock is dependent on the output resolution required.

10.6.2.7.1 Flicker Filter and Overscan Compensation

The overscan compensation scaling and the flicker filter is done in the external TV encoder chip. Care must be taken to allow for support of TV sets with high performance de-interlacers and progressive scan displays connected to by way of a non-interlaced signal. Timing will be generated with pixel granularity to allow more overscan ratios to be supported.

10.6.2.7.2 Analog Content Protection

Analog content protection will be provided through the external encoder using Macrovision 7.01. DVD software must verify the presence of a Macrovision TV encoder before playback continues. Simple attempts to disable the Macrovision operation must be detected.

10.6.2.7.3 Connectors

Target TV connectors support includes the CVBS, S-Video, Component, HDMI and SCART connectors. The external TV encoder in use will determine the method of support.

10.6.2.8 Control Bus

Communication to SDVO registers and if used, ADD2/MEC PROMs and monitor DDCs, are accomplished by using the SDVO_CTRLDATA and SDVO_CTRLCLK signals through the SDVO device. These signals run up to 1 MHz and connect directly to the SDVO device. The SDVO device is then responsible for routing the DDC and PROM data streams to the appropriate location. Consult SDVO device datasheets for level shifting requirements of these signals.

Intel® SDVO Modes

The port can be dynamically configured in several modes:

- **Standard**. This mode provides baseline SDVO functionality. It supports pixel rates between 25 MP/s and 225 MP/s. It uses three data pairs to transfer RGB data.
- **Dual Standard**. This mode provides Standard data streams across both SDVOB and SDVOC. Both channels can only run in Standard mode (3 data pairs) and each channel supports Pixel Rates between 25 MP/s and 225 MP/s.
  - Dual Independent Standard. In Dual Independent Standard mode, each SDVO channel will transmit a different pixel stream. The data stream across SDVOB will not be the same as the data stream across SDVOC.
  - Dual Simultaneous Standard. In Dual Simultaneous Standard mode, both SDVO channels will transmit the same pixel stream. The data stream across SDVOB will be the same as the data stream across SDVOC. The display timings will be identical, but the transfer timings may not be (i.e., SDVOB clocks and data may not be perfectly aligned with SDVOC clock and data as seen at the SDVO device(s)). Since this uses just a single data stream, it uses a single pixel pipeline within the GMCH.

10.6.3 Multiple Display Configurations

Microsoft Windows* 2000, Windows* XP, and Windows* Vista* operating systems provide support for multi-monitor display. Since the GMCH has several display ports available for its two display pipes, it can support up to two different images on different display devices. Timings and resolutions for these two images may be different. The GMCH supports Dual Display Clone, Dual Display Twin, and Extended Desktop.

Dual Display Clone uses both display pipes to drive the same content, at the same resolution and color depth to two different displays. This configuration allows for different refresh rates on each display.

Dual Display Twin uses one of the display pipes to drive the same content, at the same resolution, color depth, and refresh rates to two different displays.

Extended Desktop uses both display pipes to drive different content, at potentially different resolutions, refresh rates, and color depths to two different displays. This configuration allows for a larger Windows Desktop by using both displays as a work surface.

Note: The GMCH is also incapable of operating in parallel with an external PCI Express graphics device. The GMCH can, however, work in conjunction with a PCI graphics adapter.

10.7 Power Management

10.7.1 ACPI

The GMCH supports ACPI 2.0 system power states S0, S1, S3, and S5; and processor C0, C1, and C2 states. During S3, the GMCH VCC core, PCI Express, and processor VTT voltage rails are powered down – also known as S3-Cold.

Table 10-5. Intel® G33 and P35 Express Chipset (G)MCH Voltage Rails

Host State	VCC	VCC_CL	VCC_DDR DDR2/DDR3	VCC_CKDDR DDR2/DDR3	VCC_EXP
S0	1.25V	1.25V	1.8V / 1.5V	1.8V / 1.5V	1.25V
S1	1.25V	1.25V	1.8V / 1.5V	1.8V / 1.5V	1.25V
S3	0V	0V	1.8V / 1.5V	1.8V / 1.5V	0V
S5	0V	0V	0V	0V	0V

Table 10-6. Intel® Q35 and Q33 Express Chipset GMCH Voltage Rails

Host State	ME State	VCC	VCC_CL	VCC_DDR	VCC_CKDDR	VCC_EXP
S0	M0	1.25V	1.25V	1.8V	1.8V	1.25V
S1	M0	1.25V	1.25V	1.8V	1.8V	1.25V
S3	M1	0V	1.25V	1.8V	1.8V	0V
S3	Moff Wake-on-ME	0V	0V	1.8V	1.8V	0V
S3	Moff	0V	0V	1.8V	1.8V	0V
S5	M1	0V	1.25V	1.8V	1.8V	0V
S3	Moff Wake-on-ME	0V	0V	0V	0V	0V
S5	Moff	0V	0V	0V	0V	0V

The GMCH supports ACPI device power states D0, D1, D2, and D3 for the integrated graphics device.

The GMCH supports ACPI device power states D0 and D3 for the PCI Express interface

10.7.2 PCI Express Active State Power Management

- PCI Express Link States: L0, L0s, L1, L2/L3 Ready, and L3.

10.8 Thermal Sensor

There are several registers that need to be configured to support the (G)MCH thermal sensor functionality and SMI# generation. Customers must enable the Catastrophic Trip Point at 115 °C as protection for the (G)MCH. If the Catastrophic Trip Point is crossed, then the (G)MCH will instantly turn off all clocks inside the device. Customers may optionally enable the Hot Trip Point between 85 °C and 105 °C to generate SMI#. Customers will be required to then write their own SMI# handler in BIOS that will speed up the (G)MCH (or system) fan to cool the part.

10.8.1 PCI Device 0 Function 0

The SMICMD register requires that a bit be set to generate an SMI# when the Hot trip point is crossed. The ERRSTS register can be inspected for the SMI alert.

Register Address	Register Symbol	Register Name	Default Value	Access
C8–C9h	ERRSTS	Error Status	0000h	RO, RWC/S
CC–CDh	SMICMD	SMI Command	0000h	RO, RW

10.8.2 MCHBAR Thermal Sensor Registers

The Digital Thermometer Configuration Registers reside in the MCHBAR configuration space.

Address Offset	Symbol	Register Name	Default Value	Access
CD8h	TSC1	Thermal Sensor Control 1	00h	RW/L, RW, RS/WC
CD9h	TSC2	Thermal Sensor Control 2	00h	RW/L, RO
CDAh	TSS	Thermal Sensor Status	00h	RO
CDC–CDFh	TSTTP	Thermal Sensor Temperature Trip Point	00000000h	RO, RW, RW/L
CE2h	TCO	Thermal Calibration Offset	00h	RW/L/K, RW/L
CE4h	THERM1	Hardware Protection	00h	RW/L, RO, RW/L/K
CE6h	THERM3	TCO Fuses	00h	RS/WC, RO
CEA–CEBh	TIS	Thermal Interrupt Status	0000h	RO, RWC
CF1h	TSMICMD	Thermal SMI Command	00h	RO, RW

10.8.3 Programming Sequence

The following sequence must be followed in BIOS to properly set up the Hot Trip Point and ICH SMI# signal assertion:

1. In Thermal Sensor Control 1 Register (TSC1), set thermal sensor enable bit (TSE) and the hysteresis value (DHA) by writing 99h to MCHBAR CD8h
2. Program the Hot Trip Point Register (TSTTP[HTPS]) by writing the appropriate value to MCHBAR CDCh bits [15:8]
3. Program the Catastrophic Trip Point Setting Register (TSTTP[CTPS]) by writing 2Ch to MCHBAR CDCh bits [7:0]
4. In Thermal Sensor Control 2 Register (TSC2), program the Thermometer Mode Enable and Rate (TE) by writing 04h to MCHBAR CD9h bits [3:0]
5. In the Hardware Protection Register (THERM1), program the Halt on Catastrophic bit (HOC) by writing 08h to MCHBAR CE4h bits [7:0]
6. Lock the Hardware Protection by writing a 1 to the Lock bit (HTL) at MCHBAR CE4h bit [0]
7. In Thermal SMI Command Register (TSMICMD), set the SMI# on Hot bit by writing a 02h to MCHBAR CF1h
8. Program the SMI Command register (SMICMD[TSTSMI]) by writing a 1 to bit 11 to PCI CCh
9. Program the TCO Register (TCO[TSLB]) to lock down the other register settings by writing a 1 to bit 7 of MCHBAR CE2h

If the temperature rises above the Hot Trip point:
The TIS[Hot Thermal Sensor Interrupt Event] is set when SMI# interrupt is generated.

10. Clear this bit of the TIS register to allow subsequent interrupts of this type to get registered.
11. Clear the global thermal sensor event bit in the Error Status Register, bit 11.
12.
13. In thermal sensor status register (TSS), the Hot trip indicator (HTI) bit is set if this condition is still valid by the time the software gets to read the register.

10.8.4 Trip Point Temperature Programming

The Catastrophic and Hot trip points are programmed in the TSTTP Register. Bits 7:0 are for the Catastrophic Trip Point (CTPS), and bits 15:8 are for the Hot Trip Point (HTPS).

Note: The Catastrophic Trip Point is recommended to fixed at 118 C. The Hot Trip Point is recommended to be between 95 C and 105 C. Programming the Hot Trip Point above this range is not recommended.

To program both trip point settings, the following polynomial equation should be used.

Programmed temp = (0.0016 × value^2) – (1.10707 × value) + 161.05

In this case the “value” is a decimal number between 0 and 128. For the Catastrophic Trip Point, a decimal value of 41 (29h) should be used to hit 118 C.

(0.0016 × 41^2) – (1.10707 × 41) + 161.05 = 118.3 C

The CTPS should then be programmed with 29h. The Hot Trip Point is also programmed in the same manner.

10.9 Clocking

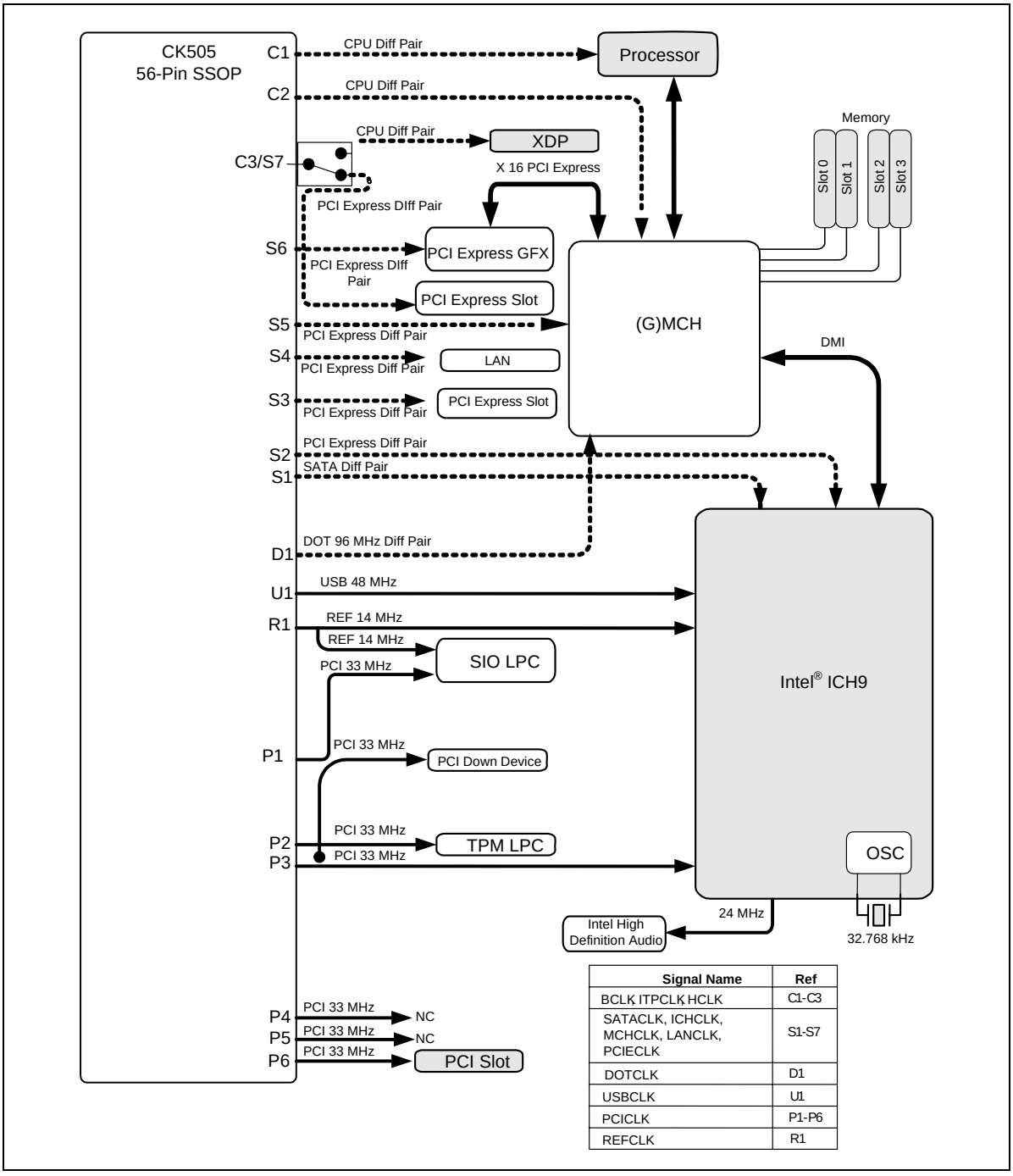
10.9.1 Overview

The (G)MCH has a total of 5 PLLs providing many times that many internal clocks. The PLLs are:

- Host PLL – Generates the main core clocks in the host clock domain. Can also be used to generate memory and internal graphics core clocks. Uses the Host clock (H_CLKIN) as a reference.
- Memory IO PLL - Optionally generates low jitter clocks for memory IO interface, as opposed to from Host PLL. Uses the Host FSB differential clock (HPL_CLKINP/HPL_CLKINN) as a reference. Low jitter clock source from Memory I/O PLL is required for DDR667 and higher frequencies.
- PCI Express PLL – Generates all PCI Express related clocks, including the Direct Media Interface that connects to the ICH. This PLL uses the 100 MHz clock (G_CLKIN) as a reference.
- Display PLL A – Generates the internal clocks for Display A. Uses D_REFCLKIN as a reference.
- Display PLL B – Generates the internal clocks for Display B. Also uses D_REFCLKIN as a reference.
- CK505 is the Clocking chip required for the Intel® 3 Series Express Chipset platform

10.9.2 Platform Clocks

Figure 10-5. Intel® 3 Series Express Chipset Clocking Diagram



Signal Name	Ref
BCLK, ITPCLK, HCLK	C1-C3
SATACLK, ICHCLK, MCHCLK, LANCLK, PCIECLK	S1-S7
DOTCLK	D1
USBCLK	U1
PCICLK	P1-P6
REFCLK	R1

§

11 Electrical Characteristics

This chapter contains the DC specifications for the (G)MCH.

Note: References to SDVO, IGD, DAC Display Interface are for the 82Q35, 82Q33, and 82G33 GMCH only.

11.1 Absolute Minimum and Maximum Ratings

The following table specifies the Intel 82Q35, 82Q33, 82G33 GMCH and 82P35 MCH absolute maximum and minimum ratings. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time its reliability will be severely degraded or not function when returned to conditions within the functional operating condition limits.

Although the (G)MCH contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 11-1. Absolute Minimum and Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{storage}$	Storage Temperature	-55	150	°C	1
(G)MCH Core					
VCC	1.25 V Core Supply Voltage with respect to VSS	-0.3	1.375	V	
Host Interface (800/1066/1333 MHz)					
VTT_FSB	System Bus Input Voltage with respect to VSS	-0.3	1.32	V	
VCCA_HPLL	1.25 V Host PLL Analog Supply Voltage with respect to VSS	-0.3	1.375	V	
System Memory Interface (DDR2 667/800 MHz, DDR3 800/1066 MHz)					
VCC_DDR	1.8 V DDR2 / 1.5 V DDR3 System Memory Supply Voltage with respect to VSS	-0.3	4.0	V	

Symbol	Parameter	Min	Max	Unit	Notes
VCC_CKDDR	1.8 V DDR2 / 1.5 V DDR3 Clock System Memory Supply Voltage with respect to VSS	-0.3	4.0	V	
VCCA_MPLL	1.25 V System Memory PLL Analog Supply Voltage with respect to VSS	-0.3	1.375	V	
PCI Express* / Intel® sDVO / DMI Interface					
VCC_EXP	1.25 V PCI Express* and DMI Supply Voltage with respect to VSS	-0.3	1.375	V	
VCCA_EXP	3.3 V PCI Express* Analog Supply Voltage with respect to VSS	-0.3	3.63	V	
VCCAPLL_EXP	1.25 V PCI Express* PLL Analog Supply Voltage with respect to VSS	-0.3	1.375	V	
R, G, B / CRT DAC Display Interface (8 bit)					
VCCA_DAC	3.3 V Display DAC Analog Supply Voltage with respect to VSS	-0.3	3.63	V	
VCCD_CRT	1.5 V Display DAC Digital Supply Voltage with respect to VSS	-0.3	1.98	V	
VCCDQ_CRT	1.5 V Display DAC Quiet Digital Supply Voltage with respect to VSS	-0.3	1.98	V	
VCCA_DPLLA	1.25 V Display PLL A Analog Supply Voltage with respect to VSS	-0.3	1.375	V	
VCCA_DPLLB	1.25 V Display PLL B Analog Supply Voltage with respect to VSS	-0.3	1.375	V	
Controller Link Interface					
VCC_CL	1.25 V Supply Voltage with respect to VSS	-0.3	1.375	V	
CMOS Interface					
VCC3_3	3.3 V CMOS Supply Voltage with respect to VSS	-0.3	3.63	V	

NOTE:
1. Possible damage to the MCH may occur if the MCH temperature exceeds 150 °C. Intel does not guarantee functionality for parts that have exceeded temperatures above 150 °C due to specification violation.

11.2 Current Consumption

The following table shows the current consumption for the (G)MCH in the Advanced Configuration and Power Interface (ACPI) S0 state. Icc max values are determined on a per-interface basis, at the highest frequencies for each interface. Sustained current values or Max current values cannot occur simultaneously on all interfaces. Sustained Values are *measured* sustained RMS maximum current consumption and includes leakage estimates. The measurements are made with fast silicon at 96 °C Tcase temperature, at the Max voltage listed in Table 11-2. The Max values are maximum theoretical pre-silicon calculated values. In some cases, the Sustained measured values have exceeded the Max theoretical values.

Table 11-2. Intel® Q35/Q33 Express Chipset – GMCH Current Consumption in S0

Symbol	Parameter	Signal Names	Sustained	Max	Unit	Notes
I_{VCC}	1.25 V Core Supply Current (using integrated graphics)	VCC (int gfx)	5.27	7.00	A	1,2
	1.25 V Core Supply Current (using external graphics)	VCC (ext gfx)	2.34	3.18		
I_{VCC_DDR2}	DDR2 System Memory Interface (1.8 V) Supply Current	VCC_DDR	2.62	3.71	A	1, 2, 3
I_{VCC_CKDDR2}	DDR2 System Memory Clock Interface (1.8 V) Supply Current	VCC_CKDDR	180	220	mA	
I_{VCC_EXP}	1.25 V PCI Express* / Intel® SDVO and DMI Supply Current (using integrated graphics)	VCC_EXP (int gfx)	0.46	1.00	A	2
	1.25 V PCI Express* / Intel® SDVO and DMI Supply Current (using external graphics)	VCC_EXP (ext gfx)	1.43	2.45		
I_{VCC_CL}	1.25 V Controller Supply Current	VCC_CL	2.45	3.88	A	2
I_{VTT_FSB}	System Bus Supply Current	VTT_FSB	0.52	1	A	1
I_{VCCA_EXP}	3.3 V PCI Express* / Intel® SDVO and DMI Analog Supply Current	VCCA_EXP	39	72	mA	
I_{VCCA_DAC}	3.3 V Display DAC Analog Supply Current	VCCA_DAC	74	78	mA	
I_{VCC3_3}	3.3 V CMOS Supply Current	VCC3_3	0.5	16	mA	
I_{VCCD_CRT}	1.5 V Display Digital Supply Current	VCCD_CRT	20	30	mA	3
I_{VCCDQ_CRT}	1.5 V Display Quiet Digital Supply Current	VCCDQ_CRT	9	11	mA	
$I_{VCCAPLL\_EXP}$	1.25 V PCI Express* / Intel® SDVO and DMI PLL Analog Supply Current	VCCAPLL_EXP	39	72	mA	
I_{VCCA_HPLL}	1.25 V Host PLL Supply Current	VCCA_HPLL	20	30	mA	
I_{VCCA_DPLLA}	1.25 V Display PLL A Supply Current	VCCA_DPLLA	49	73	mA	
I_{VCCA_DPLLB}	1.25 V Display PLL B Supply Current	VCCA_DPLLB	42	70	mA	
I_{VCCA_MPLL}	1.25 V System Memory PLL Analog Supply Current	VCCA_MPLL	115	173	mA	

NOTES:
1. Measurements are for current coming through chipset's supply pins.
2. Rail includes DLLs (and FSB sense amps on VCC).
3. Sustained Measurements are combined because one voltage regulator on the platform supplies both rails on the MCH.

Table 11-3 shows the maximum power consumption for the MCH in the ACPI S3, S4, and S5 states ***with*** Intel® Active Management Technology support. Platforms that utilize Intel Active Management Technology will keep DRAM memory powered in S4 and S5. Current consumption used by the MCH will vary between the "Idle" case and the "Max" case, depending on activity on the Intel® Management Engine. For the majority of the time, the Intel Management Engine will be in the "Idle" state. In addition, Max values are measured with fast silicon at 96° C Tcase temperature, at the Max voltage listed in the following table. The Max values are measured with a synthetic tool that forces maximum allowable bandwidth on the DRAM interface. It is unknown if commercial SW management applications will be able to generate this level of power consumption.

Table 11-3. Current Consumption in S3, S4, S5 with Intel® Active Management Technology Operation (82Q35 GMCH Only)

Symbol	Parameter	Signal Names	Idle	Max	Unit	Notes
I_{MCH_CL}	1.25 V Supply Current for MCH with Intel AMT	VCC_CL, VCCA_MPLL, VCCA_HPLL	625	1501	mA	1,2
$I_{DDR2\_PLATFORM}$	DDR2 System Memory Interface (1.8 V) Supply Current in Standby States with Intel AMT	VCC_DDR, VCC_CKDDR	143	431	mA	1,2
$I_{DDR3\_PLATFORM}$	DDR3 System Memory Interface (1.5 V) Supply Current in Standby States with Intel AMT	VCC_DDR, VCC_CKDDR	143	431	mA	1,2

NOTES:
1. Estimate is only for max current coming through chipset's supply pins, and is the I_{CC} for the MCH only.
2. Icc max values are determined on a per-interface basis. Max currents cannot occur simultaneously on all interfaces.

11.3 Signal Groups

The signal description includes the type of buffer used for the particular signal.

PCI Express* / Intel® sDVO	PCI Express interface signals. These signals are compatible with PCI Express 1.1 Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3 V tolerant. Differential voltage spec = (|D+ – D-|) * 2 = 1.2 Vmax. Single-ended maximum = 1.25 V. Single-ended minimum = 0 V.
DMI	Direct Media Interface signals. These signals are compatible with PCI Express 1.0 Signaling Environment AC Specifications, but are DC coupled. The buffers are not 3.3 V tolerant. Differential voltage spec = (|D+ - D-|) * 2 = 1.2Vmax. Single-ended maximum = 1.25 V. Single-ended minimum = 0 V.
GTL+	Open Drain GTL+ interface signal. Refer to the GTL+ I/O Specification for complete details.
HCSL	Host Clock Signal Level buffers. Current mode differential pair. Differential typical swing = (|D+ – D-|) * 2 = 1.4 V. Single ended input tolerant from -0.35 V to 1.2 V. Typical crossing voltage 0.35 V.
SSTL-1.8	Stub Series Termination Logic. These are 1.8 V output capable buffers. 1.8 V tolerant.
SSTL-1.5	Stub Series Termination Logic. These are 1.5 V output capable buffers. 1.5 V tolerant.
CMOS	CMOS buffers
Analog	Analog reference or output. May be used as a threshold voltage or for buffer compensation.

Table 11-4. Signal Groups

Signal Type	Signals	Notes
Host Interface Signal Groups		
GTL+ Input/Outputs	FSB_ADSB, FSB_BNRB, FSB_DBSYB, FSB_DINVB_3:0, FSB_DRDYB, FSB_AB_35:3, FSB_ADSTBB_1:0, FSB_DB_63:0, FSB_DSTBPB_3:0, FSB_DSTBNB_3:0, FSB_HITB, FSB_HITMB, FSB_REQB_4:0	
GTL+ Common Clock Outputs	FSB_BPRIB, FSB_BREQ0B, FSB_CPURSTB, FSB_DEFERB, FSB_TRDYB, FSB_RSB_2:0	
Analog Host I/F Ref & Comp. Signals	FSB_RCOMP, FSB_SCOMP, FSB_SCOMPB, FSB_SWING, FSB_DVREF, FSB_ACCVREF	
GTL+ Input	FSB_LOCKB, BSEL2:0	

Signal Type	Signals	Notes
PCI Express* Graphics and Intel® sDVO Interface Signal Groups		
PCI Express* / Intel® sDVO Input	**PCI Express* Interface:** PEG_RXN_15:0, PEG_RXP_15:0 **Intel® sDVO Interface:** SDVO_TVCLKIN-, SDVO_TVCLKIN, SDVOB_INT-, SDVOB_INT+, SDVOC_INT-, SDVOC_INT+, SDVO_STALL-, SDVO_STALL+	1
PCI Express* / Intel® sDVO Output	**PCI Express* Interface:** PEG_TXN_15:0, PEG_TXP_15:0 **Intel® sDVO Interface:** SDVOB_CLK-, SDVOB_CLK+, SDVOB_RED-, SDVOB_RED+, SDVOB_GREEN-, SDVOBGREEN+, SDVOB_BLUE-, SDVOB_BLUE+, SDVOC_RED-, SDVOC_RED+, SDVOC_GREEN-, SDVOC_GREEN+, SDVOC_BLUE-, SDVOC_BLUE+, SDVOC_CLK-, SDVOC_CLK+,	1
CMOS I/O OD	SDVO_CTRLCLK, SDVO_CTRLDATA	
Analog PCI Express* / Intel® sDVO I/F Compensation Signals	EXP_COMPO, EXP_COMPI	
Direct Media Interface Signal Groups		
DMI Input	DMI_RXP_3:0, DMI_RXN_3:0	
DMI Output	DMI_TXP_3:0, DMI_TXN_3:0	
System Memory Interface Signal Groups		
SSTL-1.8 / SSTL-1.5 Input/Output	DDR_A_DQ_63:0, DDR_A_DQS_7:0, DDR_A_DQSB_7:0 DDR_B_DQ_63:0, DDR_B_DQS_7:0, DDR_B_DQSB_7:0	
SSTL-1.8 / SSTL-1.5 Output	DDR_A_CK_5:0, DDR_A_CKB_5:0, DDR_A_CSB_3:0, DDR3_A_CSB_1, DDR_A_CKE_3:0, DDR_A_ODT_3:0, DDR_A_MA_14:0, DDR3_A_MA_0, DDR_A_BS_2:0, DDR_A_RASB, DDR_A_CASB, DDR_A_WEB, DDR3_A_WEB, DDR_A_DM_7:0 DDR_B_CK_5:0, DDR_B_CKB_5:0, DDR_B_CSB_3:0, DDR_B_CKE_3:0, DDR_B_ODT_3:0, DDR3_B_ODT_3, DDR_B_MA_14:0, DDR_B_BS_2:0, DDR_B_RASB, DDR_B_CASB, DDR_B_WEB, DDR_B_DM_7:0 DDR3_DRAMRST	
CMOS Input	DDR3_DRAM_PWROK	
Reference and Comp. Voltages	DDR_RCOMPXPD, DDR_RCOMPXPU, DDR_RCOMPYPD, DDR_RCOMPYPU, DDR_VREF	
Controller Link Signal Groups		
CMOS I/O OD	CL_DATA, CL_CLK	
CMOS Input	CL_RSTB, CL_PWROK	
Analog Controller Link Reference Voltage	CL_VREF	

Signal Type	Signals	Notes
R, G, B / CRT DAC Display Signal Groups		
Analog Current Outputs	CRT_RED, CRT_REDB, CRT_GREEN, CRT_GREENB, CRT_BLUE, CRT_BLUEB	
Analog/Ref DAC Miscellaneous	CRT_IREF	2
CMOS I/O OD	CRT_DDC_CLK, CRT_DDC_DATA	
HVCMOS Output	CRT_HSYNC, CRT_VSYNC	
Clocks		
HCSL	HPL_CLKINP, HPL_CLKINN, EXP_CLKINP, EXP_CLKINN, DPL_REFCLKINN, DPL_REFCLKINP	
Reset, and Miscellaneous Signal Groups		
CMOS Input	EXP_SLR, EXP_EN, PWROK, RSTINB	
CMOS Output	ICH_SYNCB	
I/O Buffer Supply Voltages		
System Bus Input Supply Voltage	VTT_FSB	
1.25 V PCI Express* / Intel® sDVO Supply Voltages	VCC_EXP	
3.3 V PCI Express* / Intel® sDVO Analog Supply Voltage	VCCA_EXP	
1.8 V DDR2 / 1.5 V DDR3 Supply Voltage	VCC_DDR	
1.8 V DDR2 / 1.5 V DDR3 Clock Supply Voltage	VCC_CKDDR	
1.25 V MCH Core Supply Voltage	VCC	
1.25 V Controller Supply Voltage	VCC_CL	
3.3 V CMOS Supply Voltage	VCC3_3	
3.3 V R, G, B / CRT DAC Display Analog Supply Voltage	VCCA_DAC	
1.5 V DAC Digital Supply Voltages	VCCD_CRT, VCCDQ_CRT	
PLL Analog Supply Voltages	VCCA_HPLL, VCCAPLL_EXP, VCCA_DPLLA, VCCA_DPLLB, VCCA_MPLL	

NOTES:

1. See Section 2.10 for Intel® sDVO & PCI Express* Pin Mapping
2. Current Mode Reference pin. DC specification not required.

11.4 DC Characteristics

11.4.1 I/O Buffer Supply Voltages

The I/O buffer supply voltage is measured at the MCH package pins. The tolerances shown in the following table are inclusive of all noise from DC up to 20 MHz. In the lab, the voltage rails should be measured with a bandwidth limited oscilloscope with a roll off of 3 dB/decade above 20 MHz under all operating conditions.

The following table indicates which supplies are connected directly to a voltage regulator or to a filtered voltage rail. For voltages that are connected to a filter, they should me measured at the *input* of the filter.

If the recommended platform decoupling guidelines cannot be met, the system designer will have to make tradeoffs between the voltage regulator output DC tolerance and the decoupling performance of the capacitor network to stay within the voltage tolerances listed below.

Table 11-5. I/O Buffer Supply Voltage

Symbol	Parameter	Min	Nom	Max	Unit	Notes
VCC_DDR	DDR2 I/O Supply Voltage	1.7	1.8	1.9	V	
	DDR3 I/O Supply Voltage	1.425	1.5	1.575	V	
VCC_CKDDR	DDR2 Clock Supply Voltage	1.7	1.8	1.9	V	2
	DDR3 Clock Supply Voltage	1.425	1.5	1.575	V	
VCC_EXP	SDVO, PCI Express* Supply Voltage	1.188	1.25	1.313	V	
VCCA_EXP	SDVO, PCI Express* Analog Supply Voltage	3.135	3.3	3.465	V	2
VTT_FSB	1.2 V System Bus Input Supply Voltage	1.14	1.2	1.26	V	4
	1.1 V System Bus Input Supply Voltage	1.045	1.1	1.155	V	
VCC	MCH Core Supply Voltage	1.188	1.25	1.313	V	
VCC_CL	Controller Supply Voltage	1.188	1.25	1.313	V	
VCC3_3	CMOS Supply Voltage	3.135	3.3	3.465	V	
VCCA_DAC	Display DAC Analog Supply Voltage	3.135	3.3	3.465	V	3
VCCD_CRT	Display Digital Supply Voltage	1.425	1.5	1.575	V	1
VCCDQ_CRT	Display Quiet Digital Supply Voltage	1.425	1.5	1.575	V	1
VCCA_HPLL, VCCAPLL_EXP, VCCA_DPLLA, VCCA_DPLLB, VCCA_MPLL	Various PLLs' Analog Supply Voltages	1.188	1.25	1.313	V	2

NOTES:

1. The VCCD_CRT and VCCDQ_CRT can also operate at a nominal 1.8 V +/- 5% input voltage. Only the 1.5 V nominal voltage setting will be validated internally.

2. These rails are filtered from other voltage rails on the platform and should be measured at the *input* of the filter. See the Platform Design Guide for proper implementation of the filter circuits.
3. VCCA_DAC voltage tolerance should only be measured when the DAC is turned ON and at a stable resolution setting. Any noise on the DAC during power on or display resolution changes do not impact the circuit.
4. MCH supports both Vtt=1.2V nominal and Vtt=1.1V nominal depending on the identified processor.

11.4.2 General DC Characteristics

Platform Reference Voltages at the top of the following table are specified at DC only. Vref measurements should be made with respect to the supply voltage. Customers should refer to the Platform Design Guide for proper decoupling of the Vref voltage dividers on the platform.

Table 11-6. DC Characteristics

Symbol	Parameter	Min	Nom	Max	Unit	Notes
Reference Voltages						
FSB_DVREF FSB_ACCVREF	Host Data, Address, and Common Clock Signal Reference Voltages	0.666 x VTT_FSB –2%	0.666 x VTT_FSB	0.666 x VTT_FSB +2%	V	
FSB_SWING	Host Compensation Reference Voltage	0.25 x VTT_FSB –2%	0.25 x VTT_FSB	0.25 x VTT_FSB +2%	V	
CL_VREF	Controller Link Reference Voltage	0.270 x VCC_CL	0.279 x VCC_CL	0.287 x VCC_CL	V	
DDR_VREF	DDR2/DDR3 Reference Voltage	0.49 x VCC_DDR	0.50 x VCC_DDR	0.51 x VCC_DDR	V	
Host Interface						
V_{IL_H}	Host GTL+ Input Low Voltage	-0.10	0	(0.666 x VTT_FSB) - 0.1	V	
V_{IH_H}	Host GTL+ Input High Voltage	(0.666 x VTT_FSB) + 0.1	VTT_FSB	VTT_FSB + 0.1	V	
V_{OL_H}	Host GTL+ Output Low Voltage	—	—	(0.25 x VTT_FSB) + 0.1	V	
V_{OH_H}	Host GTL+ Output High Voltage	VTT_FSB – 0.1	—	VTT_FSB	V	
I_{OL_H}	Host GTL+ Output Low Current	—	—	VTT_FSBmax * (1-0.25) / Rttmin	mA	Rtt_{min} = 47.5 Ω
I_{LEAK_H}	Host GTL+ Input Leakage Current	—	—	45	µA	V_{OL}< Vpad< Vtt_FSB
C_{PAD}	Host GTL+ Input Capacitance	2.0	—	2.5	pF	
C_{PCKG}	Host GTL+ Input Capacitance (common clock)	0.90	—	2.5	pF	

Symbol	Parameter	Min	Nom	Max	Unit	Notes
DDR2 System Memory Interface						
$V_{IL(DC)}$	DDR2 Input Low Voltage	—	—	DDR_VREF – 0.125	V	
$V_{IH(DC)}$	DDR2 Input High Voltage	DDR_VREF + 0.125	—		V	
$V_{IL(AC)}$	DDR2 Input Low Voltage	—	—	DDR_VREF – 0.20	V	
$V_{IH(AC)}$	DDR2 Input High Voltage	DDR_VREF + 0.20	—		V	
V_{OL}	DDR2 Output Low Voltage	—	—	0.2 * VCC_DDR	V	1
V_{OH}	DDR2 Output High Voltage	0.8 * VCC_DDR	—		V	1
I_{Leak}	Input Leakage Current	—	—	±20	µA	4
I_{Leak}	Input Leakage Current	—	—	±550	µA	5
$C_{I/O}$	DQ/DQS/DQSB DDR2 Input/Output Pin Capacitance	1.0	—	4.0	pF	
DDR3 System Memory Interface						
$V_{IL(DC)}$	DDR3 Input Low Voltage	—	—	DDR_VREF – 0.100	V	
$V_{IH(DC)}$	DDR3 Input High Voltage	DDR_VREF + 0.100	—		V	
$V_{IL(AC)}$	DDR3 Input Low Voltage	—	—	DDR_VREF – 0.175	V	
$V_{IH(AC)}$	DDR3 Input High Voltage	DDR_VREF + 0.175	—		V	
V_{OL}	DDR3 Output Low Voltage	—	—	0.2 * VCC_DDR	V	1
V_{OH}	DDR3 Output High Voltage	0.8 * VCC_DDR	—		V	1
I_{Leak}	Input Leakage Current	—	—	±20	µA	4
I_{Leak}	Input Leakage Current	—	—	±550	µA	5
$C_{I/O}$	DQ/DQS/DQSB DDR3 Input/Output Pin Capacitance	1.0	—	4.0	pF	
1.25V PCI Express* Interface 1.1 (includes PCI Express* and Intel® sDVO)						
$V_{TX\text{-}DIFF\ P\text{-}P}$	Differential Peak to Peak Output Voltage	0.800	—	1.2	V	2
$V_{TX\_CM\text{-}ACp}$	AC Peak Common Mode Output Voltage	—	—	20	mV	
$Z_{TX\text{-}DIFF\text{-}DC}$	DC Differential TX Impedance	80	100	120	Ω	
$V_{RX\text{-}DIFF\ p\text{-}p}$	Differential Peak to Peak Input Voltage	0.175	—	1.2	V	3

Symbol	Parameter	Min	Nom	Max	Unit	Notes
V_{RX_CM-ACp}	AC Peak Common Mode Input Voltage	—	—	150	mV	
Input Clocks						
V_{IL}	Input Low Voltage	-0.150	0	N/A	V	
V_{IH}	Input High Voltage	0.660	0.710	0.850	V	
$V_{CROSS(ABS)}$	Absolute Crossing Voltage	0.300	N/A	0.550	V	6,7,8
$\Delta V_{CROSS(REL)}$	Range of Crossing Points	N/A	N/A	0.140	V	
C_{IN}	Input Capacitance	1		3	pF	
SDVO_CTRLDATA, SDVO_CTRLCLK						
V_{IL}	Input Low Voltage		—	0.75	V	
V_{IH}	Input High Voltage	1.75	—		V	
I_{LEAK}	Input Leakage Current	—	—	± 10	µA	
C_{IN}	Input Capacitance	—	—	10.0	pF	
I_{OL}	Output Low Current (CMOS Outputs)	—	—	7.8	mA	@ 50% swing
I_{OH}	Output High Current (CMOS Outputs)	-1	—		mA	@ 50% swing
V_{OL}	Output Low Voltage (CMOS Outputs)		—	0.4	V	
V_{OH}	Output High Voltage (CMOS Outputs)	2.25	—		V	
CRT_DDC_DATA, CRT_DDC_CLK						
V_{IL}	Input Low Voltage		—	0.9	V	
V_{IH}	Input High Voltage	2.1	—		V	
I_{LEAK}	Input Leakage Current	—	—	± 10	µA	
C_{IN}	Input Capacitance	—	—	10.0	pF	
I_{OL}	Output Low Current (CMOS Outputs)	—	—	27.0	mA	@ 50% swing
I_{OH}	Output High Current (CMOS Outputs)	-1	—		mA	@ 50% swing
V_{OL}	Output Low Voltage (CMOS Outputs)		—	0.4	V	
V_{OH}	Output High Voltage (CMOS Outputs)	2.7	—		V	
CL_DATA, CL_CLK						
V_{IL}	Input Low Voltage		—	0.277	V	
V_{IH}	Input High Voltage	0.427	—		V	

Symbol	Parameter	Min	Nom	Max	Unit	Notes
I_{LEAK}	Input Leakage Current	—	—	± 20	µA	
C_{IN}	Input Capacitance	—	—	1.5	pF	
I_{OL}	Output Low Current (CMOS Outputs)		—	1.0	mA	@V_{OL_HI} max
I_{OH}	Output High Current (CMOS Outputs)	6.0	—		mA	@V_{OH_HI} min
V_{OL}	Output Low Voltage (CMOS Outputs)		—	0.06	V	
V_{OH}	Output High Voltage (CMOS Outputs)	0.6	—		V	
PWROK, CL_PWROK, RSTIN#						
V_{IL}	Input Low Voltage		—	0.3	V	
V_{IH}	Input High Voltage	2.7	—		V	
I_{LEAK}	Input Leakage Current	—	—	±1	mA	
C_{IN}	Input Capacitance	—	—	6.0	pF	
CL_RST#						
V_{IL}	Input Low Voltage	—	—	0.13	V	
V_{IH}	Input High Voltage	1.17	—		V	
I_{LEAK}	Input Leakage Current	—	—	±20	µA	
C_{IN}	Input Capacitance	—	—	5.0	pF	
ICH_SYNCB						
I_{OL}	Output Low Current (CMOS Outputs)	—	—	2.0	mA	@V_{OL_HI} max
I_{OH}	Output High Current (CMOS Outputs)	-2.0	—	—	mA	@V_{OH_HI} min
V_{OL}	Output Low Voltage (CMOS Outputs)	—	—	0.33	V	
V_{OH}	Output High Voltage (CMOS Outputs)	2.97	—	—	V	
EXP_SLR, EXP_EN						
V_{IL}	Input Low Voltage	-0.10	0	(0.63 x VTT) - 0.1	V	
V_{IH}	Input High Voltage	(0.63 x VTT)+0.1	VTT	VTT +0.1	V	
I_{LEAK}	Input Leakage Current	—	—	20	µA	V_{OL}< Vpad< Vtt
C_{IN}	Input Capacitance	2	—	2.5	pF	

Symbol	Parameter	Min	Nom	Max	Unit	Notes
CRT_HSYNC, CRT_VSYNC						
I_{OL}	Output Low Current (CMOS Outputs)	—	—	8.0	mA	@V_{OL_HI} max
I_{OH}	Output High Current (CMOS Outputs)	-8.0	—	—	mA	@V_{OH_HI} min
V_{OL}	Output Low Voltage (CMOS Outputs)	—	—	0.5	V	
V_{OH}	Output High Voltage (CMOS Outputs)	2.4	—	—	V	

NOTES:

1. Determined with 2x MCH Buffer Strength Settings into a 50 Ω to 0.5xVCC_DDR test load.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Transmitter compliance eye diagram of PCI Express* specification and measured over any 250 consecutive TX UIs.
3. Specified at the measurement point over any 250 consecutive UIs. The test load shown in Receiver compliance eye diagram of PCI Express* spec should be used as the RX device when taking measurements.
4. Applies to pin to VCC or VSS leakage current for the DDR_A_DQ_63:0 and DDR_B_DQ_63:0 signals.
5. Applies to pin to pin leakage current between DDR_A_DQS_7:0, DDR_A_DQSB_7:0, DDR_B_DQS_7:0, and DDR_B_DQSB_7:0 signals.
6. Crossing voltage defined as instantaneous voltage when rising edge of BCLK0 equals falling edge of BCLK1.
7. V_{Havg} is the statistical average of the V_H measured by the oscilloscope.
8. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
   Refer to the appropriate processor Electrical, Mechanical, and Thermal Specifications for further information.

11.4.3 R, G, B / CRT DAC Display DC Characteristics (Intel® 82Q35, 82Q33, 82G33 Only)

These parameters apply to the GMCH.

Table 11-7. R, G, B / CRT DAC Display DC Characteristics: Functional Operating Range (VCCA_DAC = 3.3 V ± 5%)

Parameter	Min	Typical	Max	Units	Notes
DAC Resolution	8	—	—	Bits	1
Max Luminance (full-scale)	0.665	0.700	0.770	V	1, 2, 4 (white video level voltage)
Min Luminance	—	0.000	—	V	1, 3, 4 (black video level voltage)
LSB Current	—	73.2	—	µA	4,5
Integral Linearity (INL)	-1.0	—	+1.0	LSB	1,6
Differential Linearity (DNL)	-1.0	—	+1.0	LSB	1,6
Video channel-channel voltage amplitude mismatch	—	—	6	%	7
Monotonicity	ensured			—	

NOTES:
1. Measured at each R, G, B termination according to the VESA Test Procedure – Evaluation of Analog Display Graphics Subsystems Proposal (Version 1, Draft 4, December 1, 2000).
2. Max steady-state amplitude
3. Min steady-state amplitude
4. Defined for a double 75 Ω termination.
5. Set by external reference resistor value.
6. INL and DNL measured and calculated according to VESA Video Signal Standards.
7. Max full-scale voltage difference among R, G, B outputs (percentage of steady-state full-scale voltage).

12 Ballout and Package Information

This chapter provides the ballout and package information.

12.1 Ballout

Figure 12-1, Figure 12-2, and Figure 12-3 show the (G)MCH ballout diagram as viewed from the top side of the package. The figures are divided into a left-side view and right-side view of the package.

Note: Notes for Figure 12-1, Figure 12-2, and Figure 12-3, and Table 12-1 and Table 12-2.

1. Balls that are listed as RSVD are reserved.
2. Some balls marked as reserved (RSVD) are used in XOR testing. See Chapter 14 for details.
3. Balls that are listed as NC are No Connects.
4. Analog Display Signals (CRT_RED, CRT_REDB, CRT_GREEN, CRT_GREENB, CRT_BLUE, CRT_BLUEB, CRT_IREF, CRT_HSYNC, CRT_VSYNC, CRT_DDC_CLK, CRT_DDC_DATA) and the SDVO_CTRLCLK and SDVO_CTRLDATA signals are not used on the 82P35 MCH. Contact your Intel field representative for proper termination of the corresponding balls.
5. For the 82Q35, 82Q33, 82G33 GMCH, the PCI Express and SDVO signals are multiplexed. However, only the PCI Express signal name is included in the following ballout figures and table. See Section 2.10 for the PCI Express to SDVO signal name mapping.

Figure 12-1. (G)MCH Ballout Diagram (Top View Left – Columns 43–30)

	43	42	41	40	39	38	37	36	35	34	33	32	31	30	
BC	TEST0	NC	VSS		VCC_DDR		VSS			VCC_DDR		VSS		VCC_DDR	BC
BB	NC	VCC_CKDDR	VCC_CKDDR	DDR_RCOMPYPD	VCC_DDR	DDR_A_CSB_3	VCC_DDR		DDR_A_ODT_0	DDR3_A_WEB	DDR_A_CSB_2	VCC_DDR	DDR_A_MA_10	DDR_A_MA_0	BB
BA	VCC_CKDDR	VCC_CKDDR		DDR_RCOMPYPU	DDR_A_ODT_3	DDR_A_ODT_1			DDR_A_ODT_2	DDR_A_CSB_0	DDR_A_WEB		DDR_A_BS_0	DDR_B_CSB_3	BA
AY		VCC_CKDDR	VSS	VSS		DDR_A_MA_13	DDR3_A_CSB1		DDR_A_CSB_1		DDR_A_RASB	VCC_DDR	DDR_A_BS_1		AY
AW	VSS	RSVD	VSS		DDR_B_DQS_4		DDR_B_DQ_32		DDR_A_CASB		DDR_A_CKB_2	DDR3_B_ODT3	DDR_B_CK_0		AW
AV		DDR_A_DQ_32	DDR_A_DQ_37	DDR_A_DQ_36		DDR_B_DQ_33	VSS		VSS		DDR_A_CK_2	DDR_B_CK_2	DDR_B_CKB_0		AV
AU	DDR_A_DM_4	VSS		DDR_A_DQ_33	DDR_B_DQSB_4	VSS	DDR_B_DM_4		DDR_B_DQ_36		DDR_A_CKB_5	VSS	DDR_A_CKB_0		AU
AT											DDR_A_CK_5	DDR_B_CKB_2	VSS		AT
AR		DDR_A_DQ_38	DDR_A_DQS_4	DDR_A_DQSB_4	DDR_B_DQ_44	VSS	DDR_B_DQ_39		DDR_B_DQ_37		VSS	VSS	DDR_A_CK_0		AR
AP	VSS	DDR_A_DQ_34	DDR_A_DQ_39									DDR_B_CKB_5	DDR_A_CKB_3		AP
AN		DDR_A_DQ_45	DDR_A_DQ_40	DDR_A_DQ_44	DDR_A_DQ_35	VSS	DDR_B_DQ_35	DDR_B_DQ_34	DDR_B_DQ_38		DDR_B_CK_5	RSVD	VSS		AN
AM	DDR_A_DM_5	VSS		VSS	DDR_A_DQ_41	DDR_B_DQ_41	DDR_B_DM_5	VSS	DDR_B_DQ_40	DDR_B_DQ_45	VSS		RSVD		AM
AL		DDR_A_DQ_46	DDR_A_DQS_5	DDR_A_DQSB_5	DDR_A_DQ_47	DDR_B_DQ_43	DDR_B_DQ_46	VSS	DDR_B_DQS_5	DDR_B_DQSB_5	VSS	DDR_B_DQ_47	VSS		AL
AK	VSS	DDR_A_DQ_42	DDR_A_DQ_43											VCC_CL	AK
AJ		DDR_A_DQ_52	DDR_A_DQ_53	DDR_A_DQ_48	VSS	DDR_B_DQ_49	DDR_B_DQ_52	VSS	DDR_B_DQ_53	DDR_B_DQ_42	VSS	VSS	VCC_CL	VCC_CL	AJ
AH	DDR_A_DQ_49	VSS													AH
AG		DDR_A_DQS_6	DDR_A_DQSB_6	DDR_A_DM_6	DDR_B_DM_6	DDR_B_DQ_48	VSS	DDR_B_DQSB_6	DDR_B_DQS_6	VSS	DDR_B_DQ_54	RSVD	VCC_CL	VCC_CL	AG
AF	VSS	DDR_A_DQ_55	DDR_A_DQ_54		DDR_A_DQ_50	DDR_B_DQ_61	VSS	VSS	DDR_B_DQ_50	DDR_B_DQ_55	DDR_B_DQ_51	RSVD	VCC_CL	VCC_CL	AF
AE		DDR_A_DQ_60	DDR_A_DQ_61	DDR_A_DQ_51											AE
AD	DDR_A_DQ_57	VSS		DDR_A_DQ_56	VSS	DDR_B_DM_7	VSS	DDR_B_DQ_56	VSS	DDR_B_DQ_60	VSS	VCC_CL	VCC_CL	VCC_CL	AD
AC		DDR_A_DQS_7	DDR_A_DQSB_7	DDR_A_DM_7	DDR_A_DQ_62	VSS	DDR_B_DQSB_7	DDR_B_DQS_7	VSS	DDR_B_DQ_62	DDR_B_DQ_57	VCC_CL	VCC_CL	VCC_CL	AC
AB	VSS	DDR_A_DQ_63	DDR_A_DQ_58												AB
AA		FSB_BREQ0B	FSB_RSB_1	DDR_A_DQ_59	RSVD	VSS	FSB_AB_35	DDR_B_DQ_59	VSS	DDR_B_DQ_58	DDR_B_DQ_63	VCC_CL	VCC_CL	VCC_CL	AA
Y	FSB_HITMB	VSS		FSB_TRDYB	FSB_AB_34	FSB_AB_33	VSS	FSB_AB_32	VSS	FSB_AB_29	VSS	VCC_CL	VCC_CL	VCC_CL	Y
W		FSB_BNRB	FSB_DRDYB	FSB_ADSB											W
V	VSS	FSB_AB_30	FSB_LOCKB		VSS	FSB_AB_31	VSS	FSB_AB_22	FSB_AB_28	VSS	FSB_AB_27	VSS	RSVD	VSS	V
U		FSB_HITB	FSB_RSB_0	FSB_DBSYB	FSB_RSB_2	VSS	FSB_AB_17	FSB_AB_24	VSS	FSB_ADSTBB_1	FSB_AB_25	HPL_CLKINN	RSVD	RSVD	U
T	FSB_DEFERB	VSS													T
R		FSB_DB_4	FSB_DB_2	FSB_DB_0	FSB_AB_21	FSB_AB_23	FSB_AB_19	VSS	FSB_AB_26	FSB_AB_14	VSS	HPL_CLKINP	VSS	RSVD	R
P	VSS	FSB_AB_20	FSB_DB_1											VSS	P
N		FSB_DB_7	FSB_DB_6	FSB_DB_3	FSB_AB_18	FSB_AB_16	FSB_AB_12	VSS	FSB_AB_15	FSB_AB_10	VSS	FSB_AB_9	VSS		N
M	FSB_DSTBNB_0	FSB_DSTBPB_0		FSB_DINVB_0	FSB_DB_5	FSB_AB_11	VSS	FSB_AB_13	VSS	FSB_ADSTBB_0	VSS		FSB_DB_34		M
L		FSB_DB_10	FSB_DB_8	VSS	FSB_AB_4	FSB_REQB_2	FSB_AB_6	FSB_AB_7	FSB_REQB_1		VSS	VSS	VSS		L
K	VSS	FSB_AB_8	FSB_DB_12									FSB_DB_29	FSB_DB_36		K
J		FSB_AB_3	FSB_DB_11	FSB_AB_5	FSB_DB_9	VSS	FSB_REQB_4		VSS		FSB_DINVB_1	VSS	FSB_DB_32		J
H											FSB_DSTBNB_1	FSB_DB_30	VSS		H
G	FSB_REQB_3	VSS		FSB_DB_13	FSB_BPRIB	VSS	FSB_DB_19		FSB_DSTBPB_1		FSB_DB_25	VSS	FSB_DB_37		G
F		FSB_DB_15	FSB_DB_14	FSB_REQB_0		FSB_DB_18	VSS		VSS		FSB_DB_27	FSB_DB_33	FSB_DB_39		F
E	VSS	FSB_DB_20	FSB_DB_50		FSB_DB_21		FSB_DB_22		FSB_DB_28		FSB_DINVB_3	VSS	FSB_DB_35		E
D		FSB_DB_52	FSB_DB_17	VSS		FSB_DB_56	FSB_DB_57		FSB_DB_49		FSB_DB_59	FSB_DB_63	VSS		D
C	VSS	FSB_DB_16		FSB_DB_53	FSB_DB_23	FSB_DSTBNB_3			FSB_DB_54	FSB_DB_60	FSB_DB_48		FSB_CPURSTB	VTT_FSB	C
B	NC	NC	FSB_DB_51	FSB_DB_55	FSB_DB_24	FSB_DSTBPB_3	VSS		FSB_DB_61	FSB_DB_31	FSB_DB_58	VSS	VSS	VTT_FSB	B
A	TEST2	NC	VSS		VSS		FSB_DB_26			VSS		FSB_DB_62		VTT_FSB	A
	43	42	41	40	39	38	37	36	35	34	33	32	31	30	

Figure 12-2. (G)MCH Ballout Diagram (Top View Middle– Columns 29–15)

	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	
BC		VSS		VCC_DDR		VSS		VCC_DDR		DDR_A_MA_12		VCC_DDR		DDR3_DRAMRSTB		BC
BB	DDR3_A_MA0	VCC_DDR	DDR_B_ODT_0	VCC_DDR	DDR_B_WEB	VCC_DDR	DDR_A_MA_3	DDR_A_MA_5	DDR_A_MA_7	VCC_DDR	DDR_A_CKE_2	VCC_DDR	DDR_B_BS_0	VCC_DDR	DDR_B_MA_1	BB
BA	DDR_B_CSB_1		DDR_B_ODT_2	DDR_B_CSB_2	DDR_B_CSB_0		DDR_A_MA_2	DDR_A_MA_6	DDR_A_MA_9		DDR_A_MA_14	DDR_A_CKE_3	DDR_B_MA_10		DDR_B_MA_2	BA
AY	DDR_B_ODT_3		DDR_B_MA_13		DDR_A_MA_1	DDR_B_RASB	DDR_A_MA_4		DDR_A_MA_11	DDR_A_BS_2	DDR_A_CKE_0		DDR_B_BS_1		DDR_B_MA_3	AY
AW	DDR_B_ODT_1		DDR_B_CKB_4	DDR_B_CASB		VCC_DDR	DDR_B_DQ_29		DDR_A_MA_8	VCC_DDR		DDR_A_CKE_1	DDR_B_DQ_23		DDR_B_MA_0	AW
AV	DDR_B_CK_4		VSS	VCC_DDR		DDR_B_DQ_24	VSS		VSS	DDR_A_DQ_31		VCC_DDR	VSS		DDR_B_DQ_22	AV
AU	DDR_B_CKB_3		DDR_B_CK_1	DDR_B_DQSB_3		VSS	DDR_B_DQ_28		DDR_A_DQ_26	VSS		DDR_A_DQSB_3	DDR_B_DQ_18		DDR_B_DQ_16	AU
AT	VSS		DDR_B_CKB_1	DDR_B_DQ_26		DDR_B_DQS_3	DDR_B_DQ_25		DDR_A_DQ_27	DDR_A_DQS_3		DDR_A_DQ_24	DDR_B_DQ_19		VSS	AT
AR	DDR_B_CK_3		VSS	VSS		DDR_B_DQ_30	VSS		VSS	VSS		DDR_A_DQ_25	VSS		DDR_B_DQSB_2	AR
AP	DDR_A_CK_3		DDR_A_CK_1	DDR_B_DQ_27		VSS	DDR_B_DM_3		RSVD	DDR_A_DQ_30		VSS	DDR_A_DQ_28		DDR_B_DQS_2	AP
AN	VSS		DDR_A_CKB_1	DDR_B_DQ_31		VSS	VSS		RSVD	VSS		DDR_A_DM_3	DDR_A_DQ_29		DDR3_DRAM_PWROK	AN
AM	VSS		DDR_A_CKB_4	DDR_A_CK_4		VSS	VSS		RSVD	VSS		RSTINB	PWROK		CL_PWROK	AM
AL	VCC_CL		VCC_CL	VCC_CL		VCC_CL	VCC_CL		VCC_CL	VCC_CL		VCC_CL	VCC_CL		VCC_CL	AL
AK	VCC_CL		VCC_CL	VCC_CL		VCC_CL	VCC_CL		VCC_CL	VCC_CL		VCC_CL	VCC_CL		VCC_CL	AK
AJ	VCC_CL		VCC_CL	VCC_CL		VCC_CL	VCC_CL		VCC_CL	VCC_CL		VCC_CL	VCC_CL		VCC_CL	AJ
AH																AH
AG	VCC_CL		VCC_CL	VCC_CL	VCC_CL	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		VCC	AG
AF	VCC_CL		VCC_CL	VCC	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC		VCC	AF
AE			VCC	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC			AE
AD	VCC_CL		VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC		VCC	AD
AC	VCC_CL		VCC	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC		VCC	AC
AB			VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC			AB
AA	VCC_CL		VCC	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC		VCC	AA
Y	VCC_CL		VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC		VCC	Y
W			VCC	VCC	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCC	VCC			W
V	VSS		VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		VCC	V
U	VSS		VSS	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		VCC	U
T																T
R	RSVD		VTT_FSB	VTT_FSB		VTT_FSB	VTT_FSB		VSS	RSVD		VCC	VCC		VCC	R
P	VTT_FSB		VTT_FSB	VTT_FSB		VTT_FSB	VTT_FSB		VSS	VCC		VSS	VSS		VCC	P
N	VTT_FSB		VSS	VTT_FSB		VTT_FSB	VTT_FSB		VSS	NC		RSVD	RSVD		RSVD	N
M	VTT_FSB		VSS	FSB_DB_47		VTT_FSB	VTT_FSB		VSS	VSS		RSVD	VSS		VSS	M
L	VSS		FSB_DB_42	FSB_DB_45		VTT_FSB	VTT_FSB		VSS	VSS		RSVD	RSVD		RSVD	L
K	FSB_DB_38		FSB_DB_43	VSS		VTT_FSB	VTT_FSB		VSS	ALLZTEST		VSS	RSVD		PEG_RXP_1	K
J	FSB_DB_40		VSS	FSB_DB_46		VTT_FSB	VTT_FSB		VSS	BSEL1		BSEL2	EXP_EN		PEG_RXN_1	J
H	VSS		FSB_DSTBNB_2	FSB_DB_44		VTT_FSB	VTT_FSB		VSS	VSS		RSVD	VSS		VSS	H
G	FSB_DINVB_2		FSB_DSTBPB_2	VTT_FSB		VTT_FSB	VTT_FSB		VSS	BSEL0		MTYPE	SDVO_CTRLDATA		RFU_G15	G
F	FSB_DB_41		VSS	VTT_FSB		VTT_FSB	VTT_FSB		VSS	XORTEST		VSS	RSVD		VSS	F
E	VTT_FSB		VTT_FSB	VTT_FSB		VSS	VTT_FSB		VSS	TCEN		EXP_SLR	SDVO_CTRLCLK		CRT_VSYNC	E
D	VTT_FSB	VTT_FSB	VTT_FSB		FSB_SCOMPB	FSB_DVREF	FSB_RCOMP		VSS	CRT_BLUEB	CRT_GREENB		VSS	VSS	VSS	D
C	VTT_FSB		VTT_FSB	VSS	FSB_SCOMP		VCCA_HPLL	VCCA_DPLLB	VCCD_CRT		CRT_GREEN	CRT_REDB	VCCA_DAC		CRT_HSYNC	C
B	VTT_FSB	VTT_FSB	VTT_FSB	VSS	FSB_SWING	FSB_ACCVREF	VSS	VSS	VCCDQ_CRT	CRT_BLUE	VSS	CRT_RED	VCC3_3	VCCA_DAC	VCCAPLL_EXP	B
A		VTT_FSB		VSS		VCCA_MPLL		VCCA_DPLLA		CRT_IREF		VSS		VCCA_EXP		A
	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	

Figure 12-3. (G)MCH Ballout Diagram (Top View Right – Columns 14–1)

	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
BC	VCC_DDR		DDR_B_CKE_1		VSS			DDR_A_DQ_22		VSS		VSS	NC	TEST1	BC
BB	DDR_B_MA_5	DDR_B_MA_8	VCC_DDR	DDR_B_MA_14	DDR_B_CKE_3	DDR_A_DQ_19		VSS	DDR_A_DM_2	DDR_A_DQ_16	DDR_A_DQ_21	DDR_A_DQ_11	NC	NC	BB
BA	DDR_B_MA_4	DDR_B_MA_7		DDR_B_MA_12	DDR_B_CKE_2	DDR_A_DQ_18			DDR_A_DQSB_2	DDR_A_DQ_20	DDR_A_DQ_10		RSVD	VSS	BA
AY		DDR_B_MA_9	DDR_B_MA_11	DDR_B_BS_2		DDR_A_DQ_23		DDR_A_DQS_2	DDR_A_DQ_17		VSS	DDR_A_DQ_15	DDR_A_DQ_14		AY
AW		DDR_B_DM_2	DDR_B_MA_6	DDR_B_CKE_0		DDR_B_DM_1		DDR_B_DQ_3		DDR_B_DQ_2		DDR_A_DM_1	DDR_A_DQS_1	DDR_A_DQSB_1	AW
AV		DDR_B_DQ_17	DDR_B_DQ_14	VSS		VSS		VSS	DDR_B_DQS_0		DDR_A_DQ_8	DDR_A_DQ_9	VSS		AV
AU		DDR_B_DQ_20	DDR_B_DQ_15	DDR_B_DQ_9		DDR_B_DQ_13		DDR_B_DQ_7	VSS	DDR_B_DQSB_0	VSS		DDR_A_DQ_12	DDR_A_DQ_13	AU
AT		VSS	VSS	DDR_B_DQ_8											AT
AR		DDR_B_DQ_11	DDR_B_DQS_1	DDR_B_DQ_12		VSS		DDR_B_DM_0	VSS	DDR_A_DQ_6	DDR_A_DQ_7	DDR_A_DQ_3	DDR_A_DQ_2		AR
AP		DDR_B_DQ_10	DDR_B_DQSB_1									DDR_A_DQSB_0	DDR_A_DQS_0	VSS	AP
AN		VSS	VSS	VSS		DDR_B_DQ_6	DDR_B_DQ_1	DDR_B_DQ_0	DDR_B_DQ_5	DDR_B_DQ_4	VSS	DDR_A_DQ_1	DDR_A_DM_0		AN
AM		DDR_B_DQ_21		VSS	DDR_RCOMPVOH	VSS	DDR_RCOMPVOL	VSS	DDR_VREF	CL_VREF	VSS		DDR_A_DQ_5	DDR_A_DQ_0	AM
AL		VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL	VCC_CL	DDR_RCOMPXPD	DDR_A_DQ_4	DDR_RCOMPXPU		AL
AK	VCC_CL											VCC_CL	VCC_CL	VCC_CL	AK
AJ	VCC_CL	VCC_CL	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC_CL	VCC_CL	VCC_CL		AJ
AH											VCC		VCC	VCC	AH
AG	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC		AG
AF	VCC	VCC	VCC	VCC	VSS	VSS	VSS	VSS	VSS	VSS		VCC	VCC	VCC	AF
AE											VSS	VSS	VSS		AE
AD	VCC	CL_CLK	CL_DATA	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP		VCC_EXP	VCC_EXP	AD
AC	VCC	VCC	EXP_COMPI	EXP_COMPO	VSS	DMI_TXN_2	DMI_TXP_2	VSS	VCC	VSS	VCC_EXP	VCC_EXP	VCC_EXP		AC
AB												DMI_RXP_3	VSS	VSS	AB
AA	VCC	VCC	CL_RSTB	RSVD	RSVD	RSVD	VSS	DMI_RXP_2	DMI_RXN_2	VSS	DMI_RXN_3	VCC	DMI_TXN_3		AA
Y	VCC	VCC	RSVD	VCC	VSS	DMI_RXN_1	DMI_RXP_1	VSS	VCC	VSS	DMI_TXN_1		DMI_TXP_3	VSS	Y
W											DMI_TXP_1	VSS	DMI_RXP_0		W
V	VCC	VCC	VCC	VSS	VCC	VCC	VSS	DMI_TXP_0	DMI_TXN_0	VSS		PEG_TXP_15	VSS	DMI_RXN_0	V
U	VCC	VCC	RSVD	RSVD	VCC	VCC	VSS	VSS	VCC	VSS	PEG_TXN_15	VCC	PEG_TXP_14		U
T											PEG_RXP_14		PEG_TXN_14	VSS	T
R	VCC	RSVD	RSVD	VSS	PEG_RXN_13	PEG_RXP_13	VSS	PEG_RXN_15	PEG_RXP_15	VSS	PEG_RXN_14	VSS	PEG_TXP_13		R
P	VCC											PEG_TXP_12	VSS	PEG_TXN_13	P
N		VSS	VCC	VCC	VSS	VCC	VCC	VSS	VCC	VSS	PEG_TXN_12	VCC	PEG_TXP_11		N
M		CRT_DDC_CLK		VSS	VSS	PEG_RXN_10	PEG_RXP_10	VSS	PEG_RXN_12	PEG_RXP_12	PEG_RXP_11		PEG_TXN_11	VSS	M
L		CRT_DDC_DATA	VCC	VSS		PEG_RXP_9	PEG_RXN_9	VSS	VCC	VSS	PEG_RXN_11	VSS	PEG_TXP_10		L
K		VSS	VSS									PEG_TXN_9	VSS	PEG_TXN_10	K
J		ICH_SYNCB	PEG_RXP_3	PEG_RXP_4		VSS		VSS	VCC	VSS	PEG_TXP_9	VCC	VCC		J
H		VSS	PEG_RXN_3	PEG_RXN_4											H
G		VSS	VSS	VSS		VSS		VSS	PEG_RXP_8	PEG_RXN_8	PEG_TXN_8		VCC	VSS	G
F		PEG_RXP_0	PEG_RXP_2	VCC		VCC		PEG_RXP_5	PEG_RXN_6		PEG_TXP_8	VSS	PEG_TXP_7		F
E		PEG_RXN_0	PEG_RXN_2	VSS		VSS		PEG_RXN_5		PEG_RXP_6		VSS	PEG_TXN_7	VSS	E
D		DPL_REFCLKINN	PEG_TXN_0	PEG_TXP_0		PEG_TXN_2		PEG_TXP_4	PEG_TXN_4		VCC	VSS	PEG_RXN_7		D
C	DPL_REFCLKINP	VCC		VSS	PEG_TXP_2	VCC			VSS	VSS	VSS		PEG_RXP_7	VSS	C
B	VSS	EXP_CLKINN	EXP_CLKINP	PEG_TXP_1	VSS	PEG_TXP_3		PEG_TXN_3	PEG_TXN_5	PEG_TXP_5	PEG_TXN_6	PEG_TXP_6	NC		B
A	RSVD		VSS		PEG_TXN_1			VSS		VSS		VSS			A
	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
BC43	TEST0
BC42	NC
BC41	VSS
BC40	----
BC39	VCC_DDR
BC38	----
BC37	VSS
BC36	----
BC35	----
BC34	VCC_DDR
BC33	----
BC32	VSS
BC31	----
BC30	VCC_DDR
BC29	----
BC28	VSS
BC27	----
BC26	VCC_DDR
BC25	----
BC24	VSS
BC23	----
BC22	VCC_DDR
BC21	----
BC20	DDR_A_MA_12
BC19	----
BC18	VCC_DDR
BC17	----
BC16	DDR3_DRAMRSTB
BC15	----
BC14	VCC_DDR
BC13	----

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
BC12	DDR_B_CKE_1
BC11	----
BC10	VSS
BC9	----
BC8	----
BC7	DDR_A_DQ_22
BC6	----
BC5	VSS
BC4	----
BC3	VSS
BC2	NC
BC1	TEST1
BB43	NC
BB42	VCC_CKDDR
BB41	VCC_CKDDR
BB40	DDR_RCOMPYPD
BB39	VCC_DDR
BB38	DDR_A_CSB_3
BB37	VCC_DDR
BB36	----
BB35	DDR_A_ODT_0
BB34	DDR3_A_WEB
BB33	DDR_A_CSB_2
BB32	VCC_DDR
BB31	DDR_A_MA_10
BB30	DDR_A_MA_0
BB29	DDR3_A_MA0
BB28	VCC_DDR
BB27	DDR_B_ODT_0
BB26	VCC_DDR
BB25	DDR_B_WEB

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
BB24	VCC_DDR
BB23	DDR_A_MA_3
BB22	DDR_A_MA_5
BB21	DDR_A_MA_7
BB20	VCC_DDR
BB19	DDR_A_CKE_2
BB18	VCC_DDR
BB17	DDR_B_BS_0
BB16	VCC_DDR
BB15	DDR_B_MA_1
BB14	DDR_B_MA_5
BB13	DDR_B_MA_8
BB12	VCC_DDR
BB11	DDR_B_MA_14
BB10	DDR_B_CKE_3
BB9	DDR_A_DQ_19
BB8	----
BB7	VSS
BB6	DDR_A_DM_2
BB5	DDR_A_DQ_16
BB4	DDR_A_DQ_21
BB3	DDR_A_DQ_11
BB2	NC
BB1	NC
BA43	VCC_CKDDR
BA42	VCC_CKDDR
BA41	----
BA40	DDR_RCOMPYPU
BA39	DDR_A_ODT_3
BA38	DDR_A_ODT_1
BA37	----

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
BA36	----
BA35	DDR_A_ODT_2
BA34	DDR_A_CSB_0
BA33	DDR_A_WEB
BA32	----
BA31	DDR_A_BS_0
BA30	DDR_B_CSB_3
BA29	DDR_B_CSB_1
BA28	----
BA27	DDR_B_ODT_2
BA26	DDR_B_CSB_2
BA25	DDR_B_CSB_0
BA24	----
BA23	DDR_A_MA_2
BA22	DDR_A_MA_6
BA21	DDR_A_MA_9
BA20	----
BA19	DDR_A_MA_14
BA18	DDR_A_CKE_3
BA17	DDR_B_MA_10
BA16	----
BA15	DDR_B_MA_2
BA14	DDR_B_MA_4
BA13	DDR_B_MA_7
BA12	----
BA11	DDR_B_MA_12
BA10	DDR_B_CKE_2
BA9	DDR_A_DQ_18
BA8	----
BA7	----
BA6	DDR_A_DQSB_2
BA5	DDR_A_DQ_20
BA4	DDR_A_DQ_10

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
BA3	----
BA2	RSVD
BA1	VSS
AY43	----
AY42	VCC_CKDDR
AY41	VSS
AY40	VSS
AY39	----
AY38	DDR_A_MA_13
AY37	DDR3_A_CSB1
AY36	----
AY35	DDR_A_CSB_1
AY34	----
AY33	DDR_A_RASB
AY32	VCC_DDR
AY31	DDR_A_BS_1
AY30	----
AY29	DDR_B_ODT_3
AY28	----
AY27	DDR_B_MA_13
AY26	----
AY25	DDR_A_MA_1
AY24	DDR_B_RASB
AY23	DDR_A_MA_4
AY22	----
AY21	DDR_A_MA_11
AY20	DDR_A_BS_2
AY19	DDR_A_CKE_0
AY18	----
AY17	DDR_B_BS_1
AY16	----
AY15	DDR_B_MA_3
AY14	----

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AY13	DDR_B_MA_9
AY12	DDR_B_MA_11
AY11	DDR_B_BS_2
AY10	----
AY9	DDR_A_DQ_23
AY8	----
AY7	DDR_A_DQS_2
AY6	DDR_A_DQ_17
AY5	----
AY4	VSS
AY3	DDR_A_DQ_15
AY2	DDR_A_DQ_14
AY1	----
AW43	VSS
AW42	RSVD
AW41	VSS
AW40	----
AW39	DDR_B_DQS_4
AW38	----
AW37	DDR_B_DQ_32
AW36	----
AW35	DDR_A_CASB
AW34	----
AW33	DDR_A_CKB_2
AW32	DDR3_B_ODT3
AW31	DDR_B_CK_0
AW30	----
AW29	DDR_B_ODT_1
AW28	----
AW27	DDR_B_CKB_4
AW26	DDR_B_CASB
AW25	----
AW24	VCC_DDR

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AW23	DDR_B_DQ_29
AW22	----
AW21	DDR_A_MA_8
AW20	VCC_DDR
AW19	----
AW18	DDR_A_CKE_1
AW17	DDR_B_DQ_23
AW16	----
AW15	DDR_B_MA_0
AW14	----
AW13	DDR_B_DM_2
AW12	DDR_B_MA_6
AW11	DDR_B_CKE_0
AW10	----
AW9	DDR_B_DM_1
AW8	----
AW7	DDR_B_DQ_3
AW6	----
AW5	DDR_B_DQ_2
AW4	----
AW3	DDR_A_DM_1
AW2	DDR_A_DQS_1
AW1	DDR_A_DQSB_1
AV43	----
AV42	DDR_A_DQ_32
AV41	DDR_A_DQ_37
AV40	DDR_A_DQ_36
AV39	----
AV38	DDR_B_DQ_33
AV37	VSS
AV36	----
AV35	VSS
AV34	----

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AV33	DDR_A_CK_2
AV32	DDR_B_CK_2
AV31	DDR_B_CKB_0
AV30	----
AV29	DDR_B_CK_4
AV28	----
AV27	VSS
AV26	VCC_DDR
AV25	----
AV24	DDR_B_DQ_24
AV23	VSS
AV22	----
AV21	VSS
AV20	DDR_A_DQ_31
AV19	----
AV18	VCC_DDR
AV17	VSS
AV16	----
AV15	DDR_B_DQ_22
AV14	----
AV13	DDR_B_DQ_17
AV12	DDR_B_DQ_14
AV11	VSS
AV10	----
AV9	VSS
AV8	----
AV7	VSS
AV6	DDR_B_DQS_0
AV5	----
AV4	DDR_A_DQ_8
AV3	DDR_A_DQ_9
AV2	VSS
AV1	----

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AU43	DDR_A_DM_4
AU42	VSS
AU41	----
AU40	DDR_A_DQ_33
AU39	DDR_B_DQSB_4
AU38	VSS
AU37	DDR_B_DM_4
AU36	----
AU35	DDR_B_DQ_36
AU34	----
AU33	DDR_A_CKB_5
AU32	VSS
AU31	DDR_A_CKB_0
AU30	----
AU29	DDR_B_CKB_3
AU28	----
AU27	DDR_B_CK_1
AU26	DDR_B_DQSB_3
AU25	----
AU24	VSS
AU23	DDR_B_DQ_28
AU22	----
AU21	DDR_A_DQ_26
AU20	VSS
AU19	----
AU18	DDR_A_DQSB_3
AU17	DDR_B_DQ_18
AU16	----
AU15	DDR_B_DQ_16
AU14	----
AU13	DDR_B_DQ_20
AU12	DDR_B_DQ_15
AU11	DDR_B_DQ_9

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AU10	----
AU9	DDR_B_DQ_13
AU8	----
AU7	DDR_B_DQ_7
AU6	VSS
AU5	DDR_B_DQSB_0
AU4	VSS
AU3	----
AU2	DDR_A_DQ_12
AU1	DDR_A_DQ_13
AT43	----
AT42	----
AT41	----
AT40	----
AT39	----
AT38	----
AT37	----
AT36	----
AT35	----
AT34	----
AT33	DDR_A_CK_5
AT32	DDR_B_CKB_2
AT31	VSS
AT30	----
AT29	VSS
AT28	----
AT27	DDR_B_CKB_1
AT26	DDR_B_DQ_26
AT25	----
AT24	DDR_B_DQS_3
AT23	DDR_B_DQ_25
AT22	----
AT21	DDR_A_DQ_27

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AT20	DDR_A_DQS_3
AT19	----
AT18	DDR_A_DQ_24
AT17	DDR_B_DQ_19
AT16	----
AT15	VSS
AT14	----
AT13	VSS
AT12	VSS
AT11	DDR_B_DQ_8
AT10	----
AT9	----
AT8	----
AT7	----
AT6	----
AT5	----
AT4	----
AT3	----
AT2	----
AT1	----
AR43	----
AR42	DDR_A_DQ_38
AR41	DDR_A_DQS_4
AR40	DDR_A_DQSB_4
AR39	DDR_B_DQ_44
AR38	VSS
AR37	DDR_B_DQ_39
AR36	----
AR35	DDR_B_DQ_37
AR34	----
AR33	VSS
AR32	VSS
AR31	DDR_A_CK_0

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AR30	----
AR29	DDR_B_CK_3
AR28	----
AR27	VSS
AR26	VSS
AR25	----
AR24	DDR_B_DQ_30
AR23	VSS
AR22	----
AR21	VSS
AR20	VSS
AR19	----
AR18	DDR_A_DQ_25
AR17	VSS
AR16	----
AR15	DDR_B_DQSB_2
AR14	----
AR13	DDR_B_DQ_11
AR12	DDR_B_DQS_1
AR11	DDR_B_DQ_12
AR10	----
AR9	VSS
AR8	----
AR7	DDR_B_DM_0
AR6	VSS
AR5	DDR_A_DQ_6
AR4	DDR_A_DQ_7
AR3	DDR_A_DQ_3
AR2	DDR_A_DQ_2
AR1	----
AP43	VSS
AP42	DDR_A_DQ_34
AP41	DDR_A_DQ_39

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AP40	----
AP39	----
AP38	----
AP37	----
AP36	----
AP35	----
AP34	----
AP33	----
AP32	DDR_B_CKB_5
AP31	DDR_A_CKB_3
AP30	----
AP29	DDR_A_CK_3
AP28	----
AP27	DDR_A_CK_1
AP26	DDR_B_DQ_27
AP25	----
AP24	VSS
AP23	DDR_B_DM_3
AP22	----
AP21	RSVD
AP20	DDR_A_DQ_30
AP19	----
AP18	VSS
AP17	DDR_A_DQ_28
AP16	----
AP15	DDR_B_DQS_2
AP14	----
AP13	DDR_B_DQ_10
AP12	DDR_B_DQSB_1
AP11	----
AP10	----
AP9	----
AP8	----

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AP7	----
AP6	----
AP5	----
AP4	----
AP3	DDR_A_DQSB_0
AP2	DDR_A_DQS_0
AP1	VSS
AN43	----
AN42	DDR_A_DQ_45
AN41	DDR_A_DQ_40
AN40	DDR_A_DQ_44
AN39	DDR_A_DQ_35
AN38	VSS
AN37	DDR_B_DQ_35
AN36	DDR_B_DQ_34
AN35	DDR_B_DQ_38
AN34	----
AN33	DDR_B_CK_5
AN32	RSVD
AN31	VSS
AN30	----
AN29	VSS
AN28	----
AN27	DDR_A_CKB_1
AN26	DDR_B_DQ_31
AN25	----
AN24	VSS
AN23	VSS
AN22	----
AN21	RSVD
AN20	VSS
AN19	----
AN18	DDR_A_DM_3

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AN17	DDR_A_DQ_29
AN16	----
AN15	DDR3_DRAM_PWROK
AN14	----
AN13	VSS
AN12	VSS
AN11	VSS
AN10	----
AN9	DDR_B_DQ_6
AN8	DDR_B_DQ_1
AN7	DDR_B_DQ_0
AN6	DDR_B_DQ_5
AN5	DDR_B_DQ_4
AN4	VSS
AN3	DDR_A_DQ_1
AN2	DDR_A_DM_0
AN1	----
AM43	DDR_A_DM_5
AM42	VSS
AM41	----
AM40	VSS
AM39	DDR_A_DQ_41
AM38	DDR_B_DQ_41
AM37	DDR_B_DM_5
AM36	VSS
AM35	DDR_B_DQ_40
AM34	DDR_B_DQ_45
AM33	VSS
AM32	----
AM31	RSVD
AM30	----
AM29	VSS

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AM28	----
AM27	DDR_A_CKB_4
AM26	DDR_A_CK_4
AM25	----
AM24	VSS
AM23	VSS
AM22	----
AM21	RSVD
AM20	VSS
AM19	----
AM18	RSTINB
AM17	PWROK
AM16	----
AM15	CL_PWROK
AM14	----
AM13	DDR_B_DQ_21
AM12	----
AM11	VSS
AM10	DDR_RCOMPVOH
AM9	VSS
AM8	DDR_RCOMPVOL
AM7	VSS
AM6	DDR_VREF
AM5	CL_VREF
AM4	VSS
AM3	----
AM2	DDR_A_DQ_5
AM1	DDR_A_DQ_0
AL43	----
AL42	DDR_A_DQ_46
AL41	DDR_A_DQS_5
AL40	DDR_A_DQSB_5
AL39	DDR_A_DQ_47

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AL38	DDR_B_DQ_43
AL37	DDR_B_DQ_46
AL36	VSS
AL35	DDR_B_DQS_5
AL34	DDR_B_DQSB_5
AL33	VSS
AL32	DDR_B_DQ_47
AL31	VSS
AL30	----
AL29	VCC_CL
AL28	----
AL27	VCC_CL
AL26	VCC_CL
AL25	----
AL24	VCC_CL
AL23	VCC_CL
AL22	----
AL21	VCC_CL
AL20	VCC_CL
AL19	----
AL18	VCC_CL
AL17	VCC_CL
AL16	----
AL15	VCC_CL
AL14	----
AL13	VCC_CL
AL12	VCC_CL
AL11	VCC_CL
AL10	VCC_CL
AL9	VCC_CL
AL8	VCC_CL
AL7	VCC_CL
AL6	VCC_CL

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AL5	VCC_CL
AL4	DDR_RCOMPXPD
AL3	DDR_A_DQ_4
AL2	DDR_RCOMPXPU
AL1	----
AK43	VSS
AK42	DDR_A_DQ_42
AK41	DDR_A_DQ_43
AK40	----
AK39	----
AK38	----
AK37	----
AK36	----
AK35	----
AK34	----
AK33	----
AK32	----
AK31	----
AK30	VCC_CL
AK29	VCC_CL
AK28	----
AK27	VCC_CL
AK26	VCC_CL
AK25	----
AK24	VCC_CL
AK23	VCC_CL
AK22	----
AK21	VCC_CL
AK20	VCC_CL
AK19	----
AK18	VCC_CL
AK17	VCC_CL
AK16	----

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AK15	VCC_CL
AK14	VCC_CL
AK13	----
AK12	----
AK11	----
AK10	----
AK9	----
AK8	----
AK7	----
AK6	----
AK5	----
AK4	----
AK3	VCC_CL
AK2	VCC_CL
AK1	VCC_CL
AJ43	----
AJ42	DDR_A_DQ_52
AJ41	DDR_A_DQ_53
AJ40	DDR_A_DQ_48
AJ39	VSS
AJ38	DDR_B_DQ_49
AJ37	DDR_B_DQ_52
AJ36	VSS
AJ35	DDR_B_DQ_53
AJ34	DDR_B_DQ_42
AJ33	VSS
AJ32	VSS
AJ31	VCC_CL
AJ30	VCC_CL
AJ29	VCC_CL
AJ28	----
AJ27	VCC_CL
AJ26	VCC_CL

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AJ25	----
AJ24	VCC_CL
AJ23	VCC_CL
AJ22	----
AJ21	VCC_CL
AJ20	VCC_CL
AJ19	----
AJ18	VCC_CL
AJ17	VCC_CL
AJ16	----
AJ15	VCC_CL
AJ14	VCC_CL
AJ13	VCC_CL
AJ12	VCC
AJ11	VCC
AJ10	VCC
AJ9	VCC
AJ8	VCC
AJ7	VCC
AJ6	VCC
AJ5	VCC
AJ4	VCC_CL
AJ3	VCC_CL
AJ2	VCC_CL
AJ1	----
AH43	DDR_A_DQ_49
AH42	VSS
AH41	----
AH40	----
AH39	----
AH38	----
AH37	----
AH36	----

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AH35	----
AH34	----
AH33	----
AH32	----
AH31	----
AH30	----
AH29	----
AH28	----
AH27	----
AH26	----
AH25	----
AH24	----
AH23	----
AH22	----
AH21	----
AH20	----
AH19	----
AH18	----
AH17	----
AH16	----
AH15	----
AH14	----
AH13	----
AH12	----
AH11	----
AH10	----
AH9	----
AH8	----
AH7	----
AH6	----
AH5	----
AH4	VCC
AH3	----

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AH2	VCC
AH1	VCC
AG43	----
AG42	DDR_A_DQS_6
AG41	DDR_A_DQSB_6
AG40	DDR_A_DM_6
AG39	DDR_B_DM_6
AG38	DDR_B_DQ_48
AG37	VSS
AG36	DDR_B_DQSB_6
AG35	DDR_B_DQS_6
AG34	VSS
AG33	DDR_B_DQ_54
AG32	RSVD
AG31	VCC_CL
AG30	VCC_CL
AG29	VCC_CL
AG28	----
AG27	VCC_CL
AG26	VCC_CL
AG25	VCC_CL
AG24	VCC
AG23	VCC
AG22	VCC
AG21	VCC
AG20	VCC
AG19	VCC
AG18	VCC
AG17	VCC
AG16	----
AG15	VCC
AG14	VCC
AG13	VCC

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AG12	VCC
AG11	VCC
AG10	VCC
AG9	VCC
AG8	VCC
AG7	VCC
AG6	VCC
AG5	VCC
AG4	VCC
AG3	VCC
AG2	VCC
AG1	----
AF43	VSS
AF42	DDR_A_DQ_55
AF41	DDR_A_DQ_54
AF40	----
AF39	DDR_A_DQ_50
AF38	DDR_B_DQ_61
AF37	VSS
AF36	VSS
AF35	DDR_B_DQ_50
AF34	DDR_B_DQ_55
AF33	DDR_B_DQ_51
AF32	RSVD
AF31	VCC_CL
AF30	VCC_CL
AF29	VCC_CL
AF28	----
AF27	VCC_CL
AF26	VCC
AF25	VCC
AF24	VCC
AF23	VSS

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AF22	VCC
AF21	VSS
AF20	VCC
AF19	VSS
AF18	VCC
AF17	VCC
AF16	----
AF15	VCC
AF14	VCC
AF13	VCC
AF12	VCC
AF11	VCC
AF10	VSS
AF9	VSS
AF8	VSS
AF7	VSS
AF6	VSS
AF5	VSS
AF4	----
AF3	VCC
AF2	VCC
AF1	VCC
AE43	----
AE42	DDR_A_DQ_60
AE41	DDR_A_DQ_61
AE40	DDR_A_DQ_51
AE39	----
AE38	----
AE37	----
AE36	----
AE35	----
AE34	----
AE33	----

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AE32	----
AE31	----
AE30	----
AE29	----
AE28	----
AE27	VCC
AE26	VCC
AE25	VCC
AE24	VSS
AE23	VCC
AE22	VSS
AE21	VCC
AE20	VSS
AE19	VCC
AE18	VSS
AE17	VCC
AE16	----
AE15	----
AE14	----
AE13	----
AE12	----
AE11	----
AE10	----
AE9	----
AE8	----
AE7	----
AE6	----
AE5	----
AE4	VSS
AE3	VSS
AE2	VSS
AE1	----
AD43	DDR_A_DQ_57

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AD42	VSS
AD41	----
AD40	DDR_A_DQ_56
AD39	VSS
AD38	DDR_B_DM_7
AD37	VSS
AD36	DDR_B_DQ_56
AD35	VSS
AD34	DDR_B_DQ_60
AD33	VSS
AD32	VCC_CL
AD31	VCC_CL
AD30	VCC_CL
AD29	VCC_CL
AD28	----
AD27	VCC
AD26	VCC
AD25	VSS
AD24	VCC
AD23	VSS
AD22	VCC
AD21	VSS
AD20	VCC
AD19	VSS
AD18	VCC
AD17	VCC
AD16	----
AD15	VCC
AD14	VCC
AD13	CL_CLK
AD12	CL_DATA
AD11	VCC_EXP
AD10	VCC_EXP

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AD9	VCC_EXP
AD8	VCC_EXP
AD7	VCC_EXP
AD6	VCC_EXP
AD5	VCC_EXP
AD4	VCC_EXP
AD3	----
AD2	VCC_EXP
AD1	VCC_EXP
AC43	----
AC42	DDR_A_DQS_7
AC41	DDR_A_DQSB_7
AC40	DDR_A_DM_7
AC39	DDR_A_DQ_62
AC38	VSS
AC37	DDR_B_DQSB_7
AC36	DDR_B_DQS_7
AC35	VSS
AC34	DDR_B_DQ_62
AC33	DDR_B_DQ_57
AC32	VCC_CL
AC31	VCC_CL
AC30	VCC_CL
AC29	VCC_CL
AC28	----
AC27	VCC
AC26	VCC
AC25	VCC
AC24	VSS
AC23	VCC
AC22	VSS
AC21	VCC
AC20	VSS

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AC19	VCC
AC18	VSS
AC17	VCC
AC16	----
AC15	VCC
AC14	VCC
AC13	VCC
AC12	EXP_COMPI
AC11	EXP_COMPO
AC10	VSS
AC9	DMI_TXN_2
AC8	DMI_TXP_2
AC7	VSS
AC6	VCC
AC5	VSS
AC4	VCC_EXP
AC3	VCC_EXP
AC2	VCC_EXP
AC1	----
AB43	VSS
AB42	DDR_A_DQ_63
AB41	DDR_A_DQ_58
AB40	----
AB39	----
AB38	----
AB37	----
AB36	----
AB35	----
AB34	----
AB33	----
AB32	----
AB31	----
AB30	----

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AB29	----
AB28	----
AB27	VCC
AB26	VCC
AB25	VSS
AB24	VCC
AB23	VSS
AB22	VCC
AB21	VSS
AB20	VCC
AB19	VSS
AB18	VCC
AB17	VCC
AB16	----
AB15	----
AB14	----
AB13	----
AB12	----
AB11	----
AB10	----
AB9	----
AB8	----
AB7	----
AB6	----
AB5	----
AB4	----
AB3	DMI_RXP_3
AB2	VSS
AB1	VSS
AA43	----
AA42	FSB_BREQ0B
AA41	FSB_RSB_1
AA40	DDR_A_DQ_59

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AA39	RSVD
AA38	VSS
AA37	FSB_AB_35
AA36	DDR_B_DQ_59
AA35	VSS
AA34	DDR_B_DQ_58
AA33	DDR_B_DQ_63
AA32	VCC_CL
AA31	VCC_CL
AA30	VCC_CL
AA29	VCC_CL
AA28	----
AA27	VCC
AA26	VCC
AA25	VCC
AA24	VSS
AA23	VCC
AA22	VSS
AA21	VCC
AA20	VSS
AA19	VCC
AA18	VSS
AA17	VCC
AA16	----
AA15	VCC
AA14	VCC
AA13	VCC
AA12	CL_RSTB
AA11	RSVD
AA10	RSVD
AA9	RSVD
AA8	VSS
AA7	DMI_RXP_2

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
AA6	DMI_RXN_2
AA5	VSS
AA4	DMI_RXN_3
AA3	VCC
AA2	DMI_TXN_3
AA1	----
Y43	FSB_HITMB
Y42	VSS
Y41	----
Y40	FSB_TRDYB
Y39	FSB_AB_34
Y38	FSB_AB_33
Y37	VSS
Y36	FSB_AB_32
Y35	VSS
Y34	FSB_AB_29
Y33	VSS
Y32	VCC_CL
Y31	VCC_CL
Y30	VCC_CL
Y29	VCC_CL
Y28	----
Y27	VCC
Y26	VCC
Y25	VSS
Y24	VCC
Y23	VSS
Y22	VCC
Y21	VSS
Y20	VCC
Y19	VSS
Y18	VCC
Y17	VCC

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
Y16	----
Y15	VCC
Y14	VCC
Y13	VCC
Y12	RSVD
Y11	VCC
Y10	VSS
Y9	DMI_RXN_1
Y8	DMI_RXP_1
Y7	VSS
Y6	VCC
Y5	VSS
Y4	DMI_TXN_1
Y3	----
Y2	DMI_TXP_3
Y1	VSS
W43	----
W42	FSB_BNRB
W41	FSB_DRDYB
W40	FSB_ADSB
W39	----
W38	----
W37	----
W36	----
W35	----
W34	----
W33	----
W32	----
W31	----
W30	----
W29	----
W28	----
W27	VCC

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
W26	VCC
W25	VCC
W24	VSS
W23	VCC
W22	VSS
W21	VCC
W20	VSS
W19	VCC
W18	VCC
W17	VCC
W16	----
W15	----
W14	----
W13	----
W12	----
W11	----
W10	----
W9	----
W8	----
W7	----
W6	----
W5	----
W4	DMI_TXP_1
W3	VSS
W2	DMI_RXP_0
W1	----
V43	VSS
V42	FSB_AB_30
V41	FSB_LOCKB
V40	----
V39	VSS
V38	FSB_AB_31
V37	VSS

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
V36	FSB_AB_22
V35	FSB_AB_28
V34	VSS
V33	FSB_AB_27
V32	VSS
V31	RSVD
V30	VSS
V29	VSS
V28	----
V27	VCC
V26	VCC
V25	VCC
V24	VCC
V23	VCC
V22	VCC
V21	VCC
V20	VCC
V19	VCC
V18	VCC
V17	VCC
V16	----
V15	VCC
V14	VCC
V13	VCC
V12	VCC
V11	VSS
V10	VCC
V9	VCC
V8	VSS
V7	DMI_TXP_0
V6	DMI_TXN_0
V5	VSS
V4	----

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
V3	PEG_TXP_15
V2	VSS
V1	DMI_RXN_0
U43	----
U42	FSB_HITB
U41	FSB_RSB_0
U40	FSB_DBSYB
U39	FSB_RSB_2
U38	VSS
U37	FSB_AB_17
U36	FSB_AB_24
U35	VSS
U34	FSB_ADSTBB_1
U33	FSB_AB_25
U32	HPL_CLKINN
U31	RSVD
U30	RSVD
U29	VSS
U28	----
U27	VSS
U26	VCC
U25	VCC
U24	VCC
U23	VCC
U22	VCC
U21	VCC
U20	VCC
U19	VCC
U18	VCC
U17	VCC
U16	----
U15	VCC
U14	VCC

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
U13	VCC
U12	RSVD
U11	RSVD
U10	VCC
U9	VCC
U8	VSS
U7	VSS
U6	VCC
U5	VSS
U4	PEG_TXN_15
U3	VCC
U2	PEG_TXP_14
U1	----
T43	FSB_DEFERB
T42	VSS
T41	----
T40	----
T39	----
T38	----
T37	----
T36	----
T35	----
T34	----
T33	----
T32	----
T31	----
T30	----
T29	----
T28	----
T27	----
T26	----
T25	----
T24	----

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
T23	----
T22	----
T21	----
T20	----
T19	----
T18	----
T17	----
T16	----
T15	----
T14	----
T13	----
T12	----
T11	----
T10	----
T9	----
T8	----
T7	----
T6	----
T5	----
T4	PEG_RXP_14
T3	----
T2	PEG_TXN_14
T1	VSS
R43	----
R42	FSB_DB_4
R41	FSB_DB_2
R40	FSB_DB_0
R39	FSB_AB_21
R38	FSB_AB_23
R37	FSB_AB_19
R36	VSS
R35	FSB_AB_26
R34	FSB_AB_14

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
R33	VSS
R32	HPL_CLKINP
R31	VSS
R30	RSVD
R29	RSVD
R28	----
R27	VTT_FSB
R26	VTT_FSB
R25	----
R24	VTT_FSB
R23	VTT_FSB
R22	----
R21	VSS
R20	RSVD
R19	----
R18	VCC
R17	VCC
R16	----
R15	VCC
R14	VCC
R13	RSVD
R12	RSVD
R11	VSS
R10	PEG_RXN_13
R9	PEG_RXP_13
R8	VSS
R7	PEG_RXN_15
R6	PEG_RXP_15
R5	VSS
R4	PEG_RXN_14
R3	VSS
R2	PEG_TXP_13
R1	----

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
P43	VSS
P42	FSB_AB_20
P41	FSB_DB_1
P40	----
P39	----
P38	----
P37	----
P36	----
P35	----
P34	----
P33	----
P32	----
P31	----
P30	VSS
P29	VTT_FSB
P28	----
P27	VTT_FSB
P26	VTT_FSB
P25	----
P24	VTT_FSB
P23	VTT_FSB
P22	----
P21	VSS
P20	VCC
P19	----
P18	VSS
P17	VSS
P16	----
P15	VCC
P14	VCC
P13	----
P12	----
P11	----

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
P10	----
P9	----
P8	----
P7	----
P6	----
P5	----
P4	----
P3	PEG_TXP_12
P2	VSS
P1	PEG_TXN_13
N43	----
N42	FSB_DB_7
N41	FSB_DB_6
N40	FSB_DB_3
N39	FSB_AB_18
N38	FSB_AB_16
N37	FSB_AB_12
N36	VSS
N35	FSB_AB_15
N34	FSB_AB_10
N33	VSS
N32	FSB_AB_9
N31	VSS
N30	----
N29	VTT_FSB
N28	----
N27	VSS
N26	VTT_FSB
N25	----
N24	VTT_FSB
N23	VTT_FSB
N22	----
N21	VSS

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
N20	NC
N19	----
N18	RSVD
N17	RSVD
N16	----
N15	RSVD
N14	----
N13	VSS
N12	VCC
N11	VCC
N10	VSS
N9	VCC
N8	VCC
N7	VSS
N6	VCC
N5	VSS
N4	PEG_TXN_12
N3	VCC
N2	PEG_TXP_11
N1	----
M43	FSB_DSTBNB_0
M42	FSB_DSTBPB_0
M41	----
M40	FSB_DINVB_0
M39	FSB_DB_5
M38	FSB_AB_11
M37	VSS
M36	FSB_AB_13
M35	VSS
M34	FSB_ADSTBB_0
M33	VSS
M32	----
M31	FSB_DB_34

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
M30	----
M29	VTT_FSB
M28	----
M27	VSS
M26	FSB_DB_47
M25	----
M24	VTT_FSB
M23	VTT_FSB
M22	----
M21	VSS
M20	VSS
M19	----
M18	RSVD
M17	VSS
M16	----
M15	VSS
M14	----
M13	CRT_DDC_CLK
M12	----
M11	VSS
M10	VSS
M9	PEG_RXN_10
M8	PEG_RXP_10
M7	VSS
M6	PEG_RXN_12
M5	PEG_RXP_12
M4	PEG_RXP_11
M3	----
M2	PEG_TXN_11
M1	VSS
L43	----
L42	FSB_DB_10
L41	FSB_DB_8

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
L40	VSS
L39	FSB_AB_4
L38	FSB_REQB_2
L37	FSB_AB_6
L36	FSB_AB_7
L35	FSB_REQB_1
L34	----
L33	VSS
L32	VSS
L31	VSS
L30	----
L29	VSS
L28	----
L27	FSB_DB_42
L26	FSB_DB_45
L25	----
L24	VTT_FSB
L23	VTT_FSB
L22	----
L21	VSS
L20	VSS
L19	----
L18	RSVD
L17	RSVD
L16	----
L15	RSVD
L14	----
L13	CRT_DDC_DATA
L12	VCC
L11	VSS
L10	----
L9	PEG_RXP_9
L8	PEG_RXN_9

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
L7	VSS
L6	VCC
L5	VSS
L4	PEG_RXN_11
L3	VSS
L2	PEG_TXP_10
L1	----
K43	VSS
K42	FSB_AB_8
K41	FSB_DB_12
K40	----
K39	----
K38	----
K37	----
K36	----
K35	----
K34	----
K33	----
K32	FSB_DB_29
K31	FSB_DB_36
K30	----
K29	FSB_DB_38
K28	----
K27	FSB_DB_43
K26	VSS
K25	----
K24	VTT_FSB
K23	VTT_FSB
K22	----
K21	VSS
K20	ALLZTEST
K19	----
K18	VSS

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
K17	RSVD
K16	----
K15	PEG_RXP_1
K14	----
K13	VSS
K12	VSS
K11	----
K10	----
K9	----
K8	----
K7	----
K6	----
K5	----
K4	----
K3	PEG_TXN_9
K2	VSS
K1	PEG_TXN_10
J43	----
J42	FSB_AB_3
J41	FSB_DB_11
J40	FSB_AB_5
J39	FSB_DB_9
J38	VSS
J37	FSB_REQB_4
J36	----
J35	VSS
J34	----
J33	FSB_DINVB_1
J32	VSS
J31	FSB_DB_32
J30	----
J29	FSB_DB_40
J28	----

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
J27	VSS
J26	FSB_DB_46
J25	----
J24	VTT_FSB
J23	VTT_FSB
J22	----
J21	VSS
J20	BSEL1
J19	----
J18	BSEL2
J17	EXP_EN
J16	----
J15	PEG_RXN_1
J14	----
J13	ICH_SYNCB
J12	PEG_RXP_3
J11	PEG_RXP_4
J10	----
J9	VSS
J8	----
J7	VSS
J6	VCC
J5	VSS
J4	PEG_TXP_9
J3	VCC
J2	VCC
J1	----
H43	----
H42	----
H41	----
H40	----
H39	----
H38	----

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
H37	----
H36	----
H35	----
H34	----
H33	FSB_DSTBNB_1
H32	FSB_DB_30
H31	VSS
H30	----
H29	VSS
H28	----
H27	FSB_DSTBNB_2
H26	FSB_DB_44
H25	----
H24	VTT_FSB
H23	VTT_FSB
H22	----
H21	VSS
H20	VSS
H19	----
H18	RSVD
H17	VSS
H16	----
H15	VSS
H14	----
H13	VSS
H12	PEG_RXN_3
H11	PEG_RXN_4
H10	----
H9	----
H8	----
H7	----
H6	----
H5	----

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
H4	----
H3	----
H2	----
H1	----
G43	FSB_REQB_3
G42	VSS
G41	----
G40	FSB_DB_13
G39	FSB_BPRIB
G38	VSS
G37	FSB_DB_19
G36	----
G35	FSB_DSTBPB_1
G34	----
G33	FSB_DB_25
G32	VSS
G31	FSB_DB_37
G30	----
G29	FSB_DINVB_2
G28	----
G27	FSB_DSTBPB_2
G26	VTT_FSB
G25	----
G24	VTT_FSB
G23	VTT_FSB
G22	----
G21	VSS
G20	BSEL0
G19	----
G18	MTYPE
G17	SDVO_CTRLDATA
G16	----
G15	RFU_G15

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
G14	----
G13	VSS
G12	VSS
G11	VSS
G10	----
G9	VSS
G8	----
G7	VSS
G6	PEG_RXP_8
G5	PEG_RXN_8
G4	PEG_TXN_8
G3	----
G2	VCC
G1	VSS
F43	----
F42	FSB_DB_15
F41	FSB_DB_14
F40	FSB_REQB_0
F39	----
F38	FSB_DB_18
F37	VSS
F36	----
F35	VSS
F34	----
F33	FSB_DB_27
F32	FSB_DB_33
F31	FSB_DB_39
F30	----
F29	FSB_DB_41
F28	----
F27	VSS
F26	VTT_FSB
F25	----

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
F24	VTT_FSB
F23	VTT_FSB
F22	----
F21	VSS
F20	XORTEST
F19	----
F18	VSS
F17	RSVD
F16	----
F15	VSS
F14	----
F13	PEG_RXP_0
F12	PEG_RXP_2
F11	VCC
F10	----
F9	VCC
F8	----
F7	PEG_RXP_5
F6	PEG_RXN_6
F5	----
F4	PEG_TXP_8
F3	VSS
F2	PEG_TXP_7
F1	----
E43	VSS
E42	FSB_DB_20
E41	FSB_DB_50
E40	----
E39	FSB_DB_21
E38	----
E37	FSB_DB_22
E36	----
E35	FSB_DB_28

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
E34	----
E33	FSB_DINVB_3
E32	VSS
E31	FSB_DB_35
E30	----
E29	VTT_FSB
E28	----
E27	VTT_FSB
E26	VTT_FSB
E25	----
E24	VSS
E23	VTT_FSB
E22	----
E21	VSS
E20	TCEN
E19	----
E18	EXP_SLR
E17	SDVO_CTRLCLK
E16	----
E15	CRT_VSYNC
E14	----
E13	PEG_RXN_0
E12	PEG_RXN_2
E11	VSS
E10	----
E9	VSS
E8	----
E7	PEG_RXN_5
E6	----
E5	PEG_RXP_6
E4	----
E3	VSS
E2	PEG_TXN_7

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
E1	VSS
D43	----
D42	FSB_DB_52
D41	FSB_DB_17
D40	VSS
D39	----
D38	FSB_DB_56
D37	FSB_DB_57
D36	----
D35	FSB_DB_49
D34	----
D33	FSB_DB_59
D32	FSB_DB_63
D31	VSS
D30	----
D29	VTT_FSB
D28	VTT_FSB
D27	VTT_FSB
D26	----
D25	FSB_SCOMPB
D24	FSB_DVREF
D23	FSB_RCOMP
D22	----
D21	VSS
D20	CRT_BLUEB
D19	CRT_GREENB
D18	----
D17	VSS
D16	VSS
D15	VSS
D14	----
D13	DPL_REFCLKINN
D12	PEG_TXN_0

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
D11	PEG_TXP_0
D10	----
D9	PEG_TXN_2
D8	----
D7	PEG_TXP_4
D6	PEG_TXN_4
D5	----
D4	VCC
D3	VSS
D2	PEG_RXN_7
D1	----
C43	VSS
C42	FSB_DB_16
C41	----
C40	FSB_DB_53
C39	FSB_DB_23
C38	FSB_DSTBNB_3
C37	----
C36	----
C35	FSB_DB_54
C34	FSB_DB_60
C33	FSB_DB_48
C32	----
C31	FSB_CPURSTB
C30	VTT_FSB
C29	VTT_FSB
C28	----
C27	VTT_FSB
C26	VSS
C25	FSB_SCOMP
C24	----
C23	VCCA_HPLL
C22	VCCA_DPLLB

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
C21	VCCD_CRT
C20	----
C19	CRT_GREEN
C18	CRT_REDB
C17	VCCA_DAC
C16	----
C15	CRT_HSYNC
C14	DPL_REFCLKINP
C13	VCC
C12	----
C11	VSS
C10	PEG_TXP_2
C9	VCC
C8	----
C7	----
C6	VSS
C5	VSS
C4	VSS
C3	----
C2	PEG_RXP_7
C1	VSS
B43	NC
B42	NC
B41	FSB_DB_51
B40	FSB_DB_55
B39	FSB_DB_24
B38	FSB_DSTBPB_3
B37	VSS
B36	----
B35	FSB_DB_61
B34	FSB_DB_31
B33	FSB_DB_58
B32	VSS

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
B31	VSS
B30	VTT_FSB
B29	VTT_FSB
B28	VTT_FSB
B27	VTT_FSB
B26	VSS
B25	FSB_SWING
B24	FSB_ACCVREF
B23	VSS
B22	VSS
B21	VCCDQ_CRT
B20	CRT_BLUE
B19	VSS
B18	CRT_RED
B17	VCC3_3
B16	VCCA_DAC
B15	VCCAPLL_EXP
B14	VSS
B13	EXP_CLKINN
B12	EXP_CLKINP
B11	PEG_TXP_1
B10	VSS
B9	PEG_TXP_3
B8	----
B7	PEG_TXN_3

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
B6	PEG_TXN_5
B5	PEG_TXP_5
B4	PEG_TXN_6
B3	PEG_TXP_6
B2	NC
B1	----
A43	TEST2
A42	NC
A41	VSS
A40	----
A39	VSS
A38	----
A37	FSB_DB_26
A36	----
A35	----
A34	VSS
A33	----
A32	FSB_DB_62
A31	----
A30	VTT_FSB
A29	----
A28	VTT_FSB
A27	----
A26	VSS
A25	----

Table 12-1. Ballout – Sorted by Ball

Ball	Signal Name
A24	VCCA_MPLL
A23	----
A22	VCCA_DPLLA
A21	----
A20	CRT_IREF
A19	----
A18	VSS
A17	----
A16	VCCA_EXP
A15	----
A14	RSVD
A13	----
A12	VSS
A11	----
A10	PEG_TXN_1
A9	----
A8	----
A7	VSS
A6	----
A5	VSS
A4	----
A3	VSS
A2	----
A1	----

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
ALLZTEST	K20
BSEL0	G20
BSEL1	J20
BSEL2	J18
CL_CLK	AD13
CL_DATA	AD12
CL_PWROK	AM15
CL_RSTB	AA12
CL_VREF	AM5
CRT_BLUE	B20
CRT_BLUEB	D20
CRT_DDC_CLK	M13
CRT_DDC_DATA	L13
CRT_GREEN	C19
CRT_GREENB	D19
CRT_HSYNC	C15
CRT_IREF	A20
CRT_RED	B18
CRT_REDB	C18
CRT_VSYNC	E15
DDR_A_BS_0	BA31
DDR_A_BS_1	AY31
DDR_A_BS_2	AY20
DDR_A_CASB	AW35
DDR_A_CK_0	AR31
DDR_A_CK_1	AP27
DDR_A_CK_2	AV33
DDR_A_CK_3	AP29
DDR_A_CK_4	AM26
DDR_A_CK_5	AT33
DDR_A_CKB_0	AU31

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
DDR_A_CKB_1	AN27
DDR_A_CKB_2	AW33
DDR_A_CKB_3	AP31
DDR_A_CKB_4	AM27
DDR_A_CKB_5	AU33
DDR_A_CKE_0	AY19
DDR_A_CKE_1	AW18
DDR_A_CKE_2	BB19
DDR_A_CKE_3	BA18
DDR_A_CSB_0	BA34
DDR_A_CSB_1	AY35
DDR_A_CSB_2	BB33
DDR_A_CSB_3	BB38
DDR_A_DM_0	AN2
DDR_A_DM_1	AW3
DDR_A_DM_2	BB6
DDR_A_DM_3	AN18
DDR_A_DM_4	AU43
DDR_A_DM_5	AM43
DDR_A_DM_6	AG40
DDR_A_DM_7	AC40
DDR_A_DQ_0	AM1
DDR_A_DQ_1	AN3
DDR_A_DQ_10	BA4
DDR_A_DQ_11	BB3
DDR_A_DQ_12	AU2
DDR_A_DQ_13	AU1
DDR_A_DQ_14	AY2
DDR_A_DQ_15	AY3
DDR_A_DQ_16	BB5
DDR_A_DQ_17	AY6

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
DDR_A_DQ_18	BA9
DDR_A_DQ_19	BB9
DDR_A_DQ_2	AR2
DDR_A_DQ_20	BA5
DDR_A_DQ_21	BB4
DDR_A_DQ_22	BC7
DDR_A_DQ_23	AY9
DDR_A_DQ_24	AT18
DDR_A_DQ_25	AR18
DDR_A_DQ_26	AU21
DDR_A_DQ_27	AT21
DDR_A_DQ_28	AP17
DDR_A_DQ_29	AN17
DDR_A_DQ_3	AR3
DDR_A_DQ_30	AP20
DDR_A_DQ_31	AV20
DDR_A_DQ_32	AV42
DDR_A_DQ_33	AU40
DDR_A_DQ_34	AP42
DDR_A_DQ_35	AN39
DDR_A_DQ_36	AV40
DDR_A_DQ_37	AV41
DDR_A_DQ_38	AR42
DDR_A_DQ_39	AP41
DDR_A_DQ_4	AL3
DDR_A_DQ_40	AN41
DDR_A_DQ_41	AM39
DDR_A_DQ_42	AK42
DDR_A_DQ_43	AK41
DDR_A_DQ_44	AN40
DDR_A_DQ_45	AN42

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
DDR_A_DQ_46	AL42
DDR_A_DQ_47	AL39
DDR_A_DQ_48	AJ40
DDR_A_DQ_49	AH43
DDR_A_DQ_5	AM2
DDR_A_DQ_50	AF39
DDR_A_DQ_51	AE40
DDR_A_DQ_52	AJ42
DDR_A_DQ_53	AJ41
DDR_A_DQ_54	AF41
DDR_A_DQ_55	AF42
DDR_A_DQ_56	AD40
DDR_A_DQ_57	AD43
DDR_A_DQ_58	AB41
DDR_A_DQ_59	AA40
DDR_A_DQ_6	AR5
DDR_A_DQ_60	AE42
DDR_A_DQ_61	AE41
DDR_A_DQ_62	AC39
DDR_A_DQ_63	AB42
DDR_A_DQ_7	AR4
DDR_A_DQ_8	AV4
DDR_A_DQ_9	AV3
DDR_A_DQS_0	AP2
DDR_A_DQS_1	AW2
DDR_A_DQS_2	AY7
DDR_A_DQS_3	AT20
DDR_A_DQS_4	AR41
DDR_A_DQS_5	AL41
DDR_A_DQS_6	AG42
DDR_A_DQS_7	AC42
DDR_A_DQSB_0	AP3
DDR_A_DQSB_1	AW1

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
DDR_A_DQSB_2	BA6
DDR_A_DQSB_3	AU18
DDR_A_DQSB_4	AR40
DDR_A_DQSB_5	AL40
DDR_A_DQSB_6	AG41
DDR_A_DQSB_7	AC41
DDR_A_MA_0	BB30
DDR_A_MA_1	AY25
DDR_A_MA_10	BB31
DDR_A_MA_11	AY21
DDR_A_MA_12	BC20
DDR_A_MA_13	AY38
DDR_A_MA_14	BA19
DDR_A_MA_2	BA23
DDR_A_MA_3	BB23
DDR_A_MA_4	AY23
DDR_A_MA_5	BB22
DDR_A_MA_6	BA22
DDR_A_MA_7	BB21
DDR_A_MA_8	AW21
DDR_A_MA_9	BA21
DDR_A_ODT_0	BB35
DDR_A_ODT_1	BA38
DDR_A_ODT_2	BA35
DDR_A_ODT_3	BA39
DDR_A_RASB	AY33
DDR_A_WEB	BA33
DDR_B_BS_0	BB17
DDR_B_BS_1	AY17
DDR_B_BS_2	AY11
DDR_B_CASB	AW26
DDR_B_CK_0	AW31
DDR_B_CK_1	AU27

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
DDR_B_CK_2	AV32
DDR_B_CK_3	AR29
DDR_B_CK_4	AV29
DDR_B_CK_5	AN33
DDR_B_CKB_0	AV31
DDR_B_CKB_1	AT27
DDR_B_CKB_2	AT32
DDR_B_CKB_3	AU29
DDR_B_CKB_4	AW27
DDR_B_CKB_5	AP32
DDR_B_CKE_0	AW11
DDR_B_CKE_1	BC12
DDR_B_CKE_2	BA10
DDR_B_CKE_3	BB10
DDR_B_CSB_0	BA25
DDR_B_CSB_1	BA29
DDR_B_CSB_2	BA26
DDR_B_CSB_3	BA30
DDR_B_DM_0	AR7
DDR_B_DM_1	AW9
DDR_B_DM_2	AW13
DDR_B_DM_3	AP23
DDR_B_DM_4	AU37
DDR_B_DM_5	AM37
DDR_B_DM_6	AG39
DDR_B_DM_7	AD38
DDR_B_DQ_0	AN7
DDR_B_DQ_1	AN8
DDR_B_DQ_10	AP13
DDR_B_DQ_11	AR13
DDR_B_DQ_12	AR11
DDR_B_DQ_13	AU9
DDR_B_DQ_14	AV12

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
DDR_B_DQ_15	AU12
DDR_B_DQ_16	AU15
DDR_B_DQ_17	AV13
DDR_B_DQ_18	AU17
DDR_B_DQ_19	AT17
DDR_B_DQ_2	AW5
DDR_B_DQ_20	AU13
DDR_B_DQ_21	AM13
DDR_B_DQ_22	AV15
DDR_B_DQ_23	AW17
DDR_B_DQ_24	AV24
DDR_B_DQ_25	AT23
DDR_B_DQ_26	AT26
DDR_B_DQ_27	AP26
DDR_B_DQ_28	AU23
DDR_B_DQ_29	AW23
DDR_B_DQ_3	AW7
DDR_B_DQ_30	AR24
DDR_B_DQ_31	AN26
DDR_B_DQ_32	AW37
DDR_B_DQ_33	AV38
DDR_B_DQ_34	AN36
DDR_B_DQ_35	AN37
DDR_B_DQ_36	AU35
DDR_B_DQ_37	AR35
DDR_B_DQ_38	AN35
DDR_B_DQ_39	AR37
DDR_B_DQ_4	AN5
DDR_B_DQ_40	AM35
DDR_B_DQ_41	AM38
DDR_B_DQ_42	AJ34
DDR_B_DQ_43	AL38
DDR_B_DQ_44	AR39

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
DDR_B_DQ_45	AM34
DDR_B_DQ_46	AL37
DDR_B_DQ_47	AL32
DDR_B_DQ_48	AG38
DDR_B_DQ_49	AJ38
DDR_B_DQ_5	AN6
DDR_B_DQ_50	AF35
DDR_B_DQ_51	AF33
DDR_B_DQ_52	AJ37
DDR_B_DQ_53	AJ35
DDR_B_DQ_54	AG33
DDR_B_DQ_55	AF34
DDR_B_DQ_56	AD36
DDR_B_DQ_57	AC33
DDR_B_DQ_58	AA34
DDR_B_DQ_59	AA36
DDR_B_DQ_6	AN9
DDR_B_DQ_60	AD34
DDR_B_DQ_61	AF38
DDR_B_DQ_62	AC34
DDR_B_DQ_63	AA33
DDR_B_DQ_7	AU7
DDR_B_DQ_8	AT11
DDR_B_DQ_9	AU11
DDR_B_DQS_0	AV6
DDR_B_DQS_1	AR12
DDR_B_DQS_2	AP15
DDR_B_DQS_3	AT24
DDR_B_DQS_4	AW39
DDR_B_DQS_5	AL35
DDR_B_DQS_6	AG35
DDR_B_DQS_7	AC36
DDR_B_DQSB_0	AU5

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
DDR_B_DQSB_1	AP12
DDR_B_DQSB_2	AR15
DDR_B_DQSB_3	AU26
DDR_B_DQSB_4	AU39
DDR_B_DQSB_5	AL34
DDR_B_DQSB_6	AG36
DDR_B_DQSB_7	AC37
DDR_B_MA_0	AW15
DDR_B_MA_1	BB15
DDR_B_MA_10	BA17
DDR_B_MA_11	AY12
DDR_B_MA_12	BA11
DDR_B_MA_13	AY27
DDR_B_MA_14	BB11
DDR_B_MA_2	BA15
DDR_B_MA_3	AY15
DDR_B_MA_4	BA14
DDR_B_MA_5	BB14
DDR_B_MA_6	AW12
DDR_B_MA_7	BA13
DDR_B_MA_8	BB13
DDR_B_MA_9	AY13
DDR_B_ODT_0	BB27
DDR_B_ODT_1	AW29
DDR_B_ODT_2	BA27
DDR_B_ODT_3	AY29
DDR_B_RASB	AY24
DDR_B_WEB	BB25
DDR_RCOMPVOH	AM10
DDR_RCOMPVOL	AM8
DDR_RCOMPXPD	AL4
DDR_RCOMPXPU	AL2
DDR_RCOMPYPD	BB40

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
DDR_RCOMPYPU	BA40
DDR_VREF	AM6
DDR3_A_CSB1	AY37
DDR3_A_MA0	BB29
DDR3_A_WEB	BB34
DDR3_B_ODT3	AW32
DDR3_DRAM_PWROK	AN15
DDR3_DRAMRSTB	BC16
DMI_RXN_0	V1
DMI_RXN_1	Y9
DMI_RXN_2	AA6
DMI_RXN_3	AA4
DMI_RXP_0	W2
DMI_RXP_1	Y8
DMI_RXP_2	AA7
DMI_RXP_3	AB3
DMI_TXN_0	V6
DMI_TXN_1	Y4
DMI_TXN_2	AC9
DMI_TXN_3	AA2
DMI_TXP_0	V7
DMI_TXP_1	W4
DMI_TXP_2	AC8
DMI_TXP_3	Y2
DPL_REFCLKINN	D13
DPL_REFCLKINP	C14
EXP_CLKINN	B13
EXP_CLKINP	B12
EXP_COMPI	AC12
EXP_COMPO	AC11
EXP_EN	J17

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
EXP_SLR	E18
FSB_AB_10	N34
FSB_AB_11	M38
FSB_AB_12	N37
FSB_AB_13	M36
FSB_AB_14	R34
FSB_AB_15	N35
FSB_AB_16	N38
FSB_AB_17	U37
FSB_AB_18	N39
FSB_AB_19	R37
FSB_AB_20	P42
FSB_AB_21	R39
FSB_AB_22	V36
FSB_AB_23	R38
FSB_AB_24	U36
FSB_AB_25	U33
FSB_AB_26	R35
FSB_AB_27	V33
FSB_AB_28	V35
FSB_AB_29	Y34
FSB_AB_3	J42
FSB_AB_30	V42
FSB_AB_31	V38
FSB_AB_32	Y36
FSB_AB_33	Y38
FSB_AB_34	Y39
FSB_AB_35	AA37
FSB_AB_4	L39
FSB_AB_5	J40
FSB_AB_6	L37
FSB_AB_7	L36
FSB_AB_8	K42

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
FSB_AB_9	N32
FSB_ACCVREF	B24
FSB_ADSB	W40
FSB_ADSTBB_0	M34
FSB_ADSTBB_1	U34
FSB_BNRB	W42
FSB_BPRIB	G39
FSB_BREQ0B	AA42
FSB_CPURSTB	C31
FSB_DB_0	R40
FSB_DB_1	P41
FSB_DB_10	L42
FSB_DB_11	J41
FSB_DB_12	K41
FSB_DB_13	G40
FSB_DB_14	F41
FSB_DB_15	F42
FSB_DB_16	C42
FSB_DB_17	D41
FSB_DB_18	F38
FSB_DB_19	G37
FSB_DB_2	R41
FSB_DB_20	E42
FSB_DB_21	E39
FSB_DB_22	E37
FSB_DB_23	C39
FSB_DB_24	B39
FSB_DB_25	G33
FSB_DB_26	A37
FSB_DB_27	F33
FSB_DB_28	E35
FSB_DB_29	K32
FSB_DB_3	N40

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
FSB_DB_30	H32
FSB_DB_31	B34
FSB_DB_32	J31
FSB_DB_33	F32
FSB_DB_34	M31
FSB_DB_35	E31
FSB_DB_36	K31
FSB_DB_37	G31
FSB_DB_38	K29
FSB_DB_39	F31
FSB_DB_4	R42
FSB_DB_40	J29
FSB_DB_41	F29
FSB_DB_42	L27
FSB_DB_43	K27
FSB_DB_44	H26
FSB_DB_45	L26
FSB_DB_46	J26
FSB_DB_47	M26
FSB_DB_48	C33
FSB_DB_49	D35
FSB_DB_5	M39
FSB_DB_50	E41
FSB_DB_51	B41
FSB_DB_52	D42
FSB_DB_53	C40
FSB_DB_54	C35
FSB_DB_55	B40
FSB_DB_56	D38
FSB_DB_57	D37
FSB_DB_58	B33
FSB_DB_59	D33
FSB_DB_6	N41

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
FSB_DB_60	C34
FSB_DB_61	B35
FSB_DB_62	A32
FSB_DB_63	D32
FSB_DB_7	N42
FSB_DB_8	L41
FSB_DB_9	J39
FSB_DBSYB	U40
FSB_DEFERB	T43
FSB_DINVB_0	M40
FSB_DINVB_1	J33
FSB_DINVB_2	G29
FSB_DINVB_3	E33
FSB_DRDYB	W41
FSB_DSTBNB_0	M43
FSB_DSTBNB_1	H33
FSB_DSTBNB_2	H27
FSB_DSTBNB_3	C38
FSB_DSTBPB_0	M42
FSB_DSTBPB_1	G35
FSB_DSTBPB_2	G27
FSB_DSTBPB_3	B38
FSB_DVREF	D24
FSB_HITB	U42
FSB_HITMB	Y43
FSB_LOCKB	V41
FSB_RCOMP	D23
FSB_REQB_0	F40
FSB_REQB_1	L35
FSB_REQB_2	L38
FSB_REQB_3	G43
FSB_REQB_4	J37
FSB_RSB_0	U41

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
FSB_RSB_1	AA41
FSB_RSB_2	U39
FSB_SCOMP	C25
FSB_SCOMPB	D25
FSB_SWING	B25
FSB_TRDYB	Y40
HPL_CLKINN	U32
HPL_CLKINP	R32
ICH_SYNCB	J13
MTYPE	G18
NC	BC42
NC	BC2
NC	BB43
NC	BB2
NC	BB1
NC	N20
NC	B43
NC	B42
NC	B2
NC	A42
PEG_RXN_0	E13
PEG_RXN_1	J15
PEG_RXN_10	M9
PEG_RXN_11	L4
PEG_RXN_12	M6
PEG_RXN_13	R10
PEG_RXN_14	R4
PEG_RXN_15	R7
PEG_RXN_2	E12
PEG_RXN_3	H12
PEG_RXN_4	H11
PEG_RXN_5	E7
PEG_RXN_6	F6

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
PEG_RXN_7	D2
PEG_RXN_8	G5
PEG_RXN_9	L8
PEG_RXP_0	F13
PEG_RXP_1	K15
PEG_RXP_10	M8
PEG_RXP_11	M4
PEG_RXP_12	M5
PEG_RXP_13	R9
PEG_RXP_14	T4
PEG_RXP_15	R6
PEG_RXP_2	F12
PEG_RXP_3	J12
PEG_RXP_4	J11
PEG_RXP_5	F7
PEG_RXP_6	E5
PEG_RXP_7	C2
PEG_RXP_8	G6
PEG_RXP_9	L9
PEG_TXN_0	D12
PEG_TXN_1	A10
PEG_TXN_10	K1
PEG_TXN_11	M2
PEG_TXN_12	N4
PEG_TXN_13	P1
PEG_TXN_14	T2
PEG_TXN_15	U4
PEG_TXN_2	D9
PEG_TXN_3	B7
PEG_TXN_4	D6
PEG_TXN_5	B6
PEG_TXN_6	B4
PEG_TXN_7	E2

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
PEG_TXN_8	G4
PEG_TXN_9	K3
PEG_TXP_0	D11
PEG_TXP_1	B11
PEG_TXP_10	L2
PEG_TXP_11	N2
PEG_TXP_12	P3
PEG_TXP_13	R2
PEG_TXP_14	U2
PEG_TXP_15	V3
PEG_TXP_2	C10
PEG_TXP_3	B9
PEG_TXP_4	D7
PEG_TXP_5	B5
PEG_TXP_6	B3
PEG_TXP_7	F2
PEG_TXP_8	F4
PEG_TXP_9	J4
PWROK	AM17
RFU_G15	G15
RSTINB	AM18
RSVD	BA2
RSVD	AW42
RSVD	AP21
RSVD	AN32
RSVD	AN21
RSVD	AM31
RSVD	AM21
RSVD	AG32
RSVD	AF32
RSVD	AA39
RSVD	AA11
RSVD	AA10

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
RSVD	AA9
RSVD	Y12
RSVD	V31
RSVD	U31
RSVD	U30
RSVD	U12
RSVD	U11
RSVD	R30
RSVD	R29
RSVD	R20
RSVD	R13
RSVD	R12
RSVD	N18
RSVD	N17
RSVD	N15
RSVD	M18
RSVD	L18
RSVD	L17
RSVD	L15
RSVD	K17
RSVD	H18
RSVD	F17
RSVD	A14
SDVO_CTRLCLK	E17
SDVO_CTRLDATA	G17
TCEN	E20
TEST0	BC43
TEST1	BC1
TEST2	A43
VCC	AJ12
VCC	AJ11
VCC	AJ10
VCC	AJ9

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
VCC	AJ8
VCC	AJ7
VCC	AJ6
VCC	AJ5
VCC	AH4
VCC	AH2
VCC	AH1
VCC	AG24
VCC	AG23
VCC	AG22
VCC	AG21
VCC	AG20
VCC	AG19
VCC	AG18
VCC	AG17
VCC	AG15
VCC	AG14
VCC	AG13
VCC	AG12
VCC	AG11
VCC	AG10
VCC	AG9
VCC	AG8
VCC	AG7
VCC	AG6
VCC	AG5
VCC	AG4
VCC	AG3
VCC	AG2
VCC	AF26
VCC	AF25
VCC	AF24
VCC	AF22

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
VCC	AF20
VCC	AF18
VCC	AF17
VCC	AF15
VCC	AF14
VCC	AF13
VCC	AF12
VCC	AF11
VCC	AF3
VCC	AF2
VCC	AF1
VCC	AE27
VCC	AE26
VCC	AE25
VCC	AE23
VCC	AE21
VCC	AE19
VCC	AE17
VCC	AD27
VCC	AD26
VCC	AD24
VCC	AD22
VCC	AD20
VCC	AD18
VCC	AD17
VCC	AD15
VCC	AD14
VCC	AC27
VCC	AC26
VCC	AC25
VCC	AC23
VCC	AC21
VCC	AC19

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
VCC	AC17
VCC	AC15
VCC	AC14
VCC	AC13
VCC	AC6
VCC	AB27
VCC	AB26
VCC	AB24
VCC	AB22
VCC	AB20
VCC	AB18
VCC	AB17
VCC	AA27
VCC	AA26
VCC	AA25
VCC	AA23
VCC	AA21
VCC	AA19
VCC	AA17
VCC	AA15
VCC	AA14
VCC	AA13
VCC	AA3
VCC	Y27
VCC	Y26
VCC	Y24
VCC	Y22
VCC	Y20
VCC	Y18
VCC	Y17
VCC	Y15
VCC	Y14
VCC	Y13

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
VCC	Y11
VCC	Y6
VCC	W27
VCC	W26
VCC	W25
VCC	W23
VCC	W21
VCC	W19
VCC	W18
VCC	W17
VCC	V27
VCC	V26
VCC	V25
VCC	V24
VCC	V23
VCC	V22
VCC	V21
VCC	V20
VCC	V19
VCC	V18
VCC	V17
VCC	V15
VCC	V14
VCC	V13
VCC	V12
VCC	V10
VCC	V9
VCC	U26
VCC	U25
VCC	U24
VCC	U23
VCC	U22
VCC	U21

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
VCC	U20
VCC	U19
VCC	U18
VCC	U17
VCC	U15
VCC	U14
VCC	U13
VCC	U10
VCC	U9
VCC	U6
VCC	U3
VCC	R18
VCC	R17
VCC	R15
VCC	R14
VCC	P20
VCC	P15
VCC	P14
VCC	N12
VCC	N11
VCC	N9
VCC	N8
VCC	N6
VCC	N3
VCC	L12
VCC	L6
VCC	J6
VCC	J3
VCC	J2
VCC	G2
VCC	F11
VCC	F9
VCC	D4

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
VCC	C13
VCC	C9
VCC_CKDDR	BB42
VCC_CKDDR	BB41
VCC_CKDDR	BA43
VCC_CKDDR	BA42
VCC_CKDDR	AY42
VCC_CL	AL29
VCC_CL	AL27
VCC_CL	AL26
VCC_CL	AL24
VCC_CL	AL23
VCC_CL	AL21
VCC_CL	AL20
VCC_CL	AL18
VCC_CL	AL17
VCC_CL	AL15
VCC_CL	AL13
VCC_CL	AL12
VCC_CL	AL11
VCC_CL	AL10
VCC_CL	AL9
VCC_CL	AL8
VCC_CL	AL7
VCC_CL	AL6
VCC_CL	AL5
VCC_CL	AK30
VCC_CL	AK29
VCC_CL	AK27
VCC_CL	AK26
VCC_CL	AK24
VCC_CL	AK23
VCC_CL	AK21

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
VCC_CL	AK20
VCC_CL	AK18
VCC_CL	AK17
VCC_CL	AK15
VCC_CL	AK14
VCC_CL	AK3
VCC_CL	AK2
VCC_CL	AK1
VCC_CL	AJ31
VCC_CL	AJ30
VCC_CL	AJ29
VCC_CL	AJ27
VCC_CL	AJ26
VCC_CL	AJ24
VCC_CL	AJ23
VCC_CL	AJ21
VCC_CL	AJ20
VCC_CL	AJ18
VCC_CL	AJ17
VCC_CL	AJ15
VCC_CL	AJ14
VCC_CL	AJ13
VCC_CL	AJ4
VCC_CL	AJ3
VCC_CL	AJ2
VCC_CL	AG31
VCC_CL	AG30
VCC_CL	AG29
VCC_CL	AG27
VCC_CL	AG26
VCC_CL	AG25
VCC_CL	AF31
VCC_CL	AF30

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
VCC_CL	AF29
VCC_CL	AF27
VCC_CL	AD32
VCC_CL	AD31
VCC_CL	AD30
VCC_CL	AD29
VCC_CL	AC32
VCC_CL	AC31
VCC_CL	AC30
VCC_CL	AC29
VCC_CL	AA32
VCC_CL	AA31
VCC_CL	AA30
VCC_CL	AA29
VCC_CL	Y32
VCC_CL	Y31
VCC_CL	Y30
VCC_CL	Y29
VCC_DDR	BC39
VCC_DDR	BC34
VCC_DDR	BC30
VCC_DDR	BC26
VCC_DDR	BC22
VCC_DDR	BC18
VCC_DDR	BC14
VCC_DDR	BB39
VCC_DDR	BB37
VCC_DDR	BB32
VCC_DDR	BB28
VCC_DDR	BB26
VCC_DDR	BB24
VCC_DDR	BB20
VCC_DDR	BB18

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
VCC_DDR	BB16
VCC_DDR	BB12
VCC_DDR	AY32
VCC_DDR	AW24
VCC_DDR	AW20
VCC_DDR	AV26
VCC_DDR	AV18
VCC_EXP	AD11
VCC_EXP	AD10
VCC_EXP	AD9
VCC_EXP	AD8
VCC_EXP	AD7
VCC_EXP	AD6
VCC_EXP	AD5
VCC_EXP	AD4
VCC_EXP	AD2
VCC_EXP	AD1
VCC_EXP	AC4
VCC_EXP	AC3
VCC_EXP	AC2
VCC3_3	B17
VCCA_DAC	C17
VCCA_DAC	B16
VCCA_DPLLA	A22
VCCA_DPLLB	C22
VCCA_EXP	A16
VCCA_HPLL	C23
VCCA_MPLL	A24
VCCAPLL_EXP	B15
VCCD_CRT	C21
VCCDQ_CRT	B21
VSS	BC41
VSS	BC37

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
VSS	BC32
VSS	BC28
VSS	BC24
VSS	BC10
VSS	BC5
VSS	BC3
VSS	BB7
VSS	BA1
VSS	AY41
VSS	AY40
VSS	AY4
VSS	AW43
VSS	AW41
VSS	AV37
VSS	AV35
VSS	AV27
VSS	AV23
VSS	AV21
VSS	AV17
VSS	AV11
VSS	AV9
VSS	AV7
VSS	AV2
VSS	AU42
VSS	AU38
VSS	AU32
VSS	AU24
VSS	AU20
VSS	AU6
VSS	AU4
VSS	AT31
VSS	AT29
VSS	AT15

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
VSS	AT13
VSS	AT12
VSS	AR38
VSS	AR33
VSS	AR32
VSS	AR27
VSS	AR26
VSS	AR23
VSS	AR21
VSS	AR20
VSS	AR17
VSS	AR9
VSS	AR6
VSS	AP43
VSS	AP24
VSS	AP18
VSS	AP1
VSS	AN38
VSS	AN31
VSS	AN29
VSS	AN24
VSS	AN23
VSS	AN20
VSS	AN13
VSS	AN12
VSS	AN11
VSS	AN4
VSS	AM42
VSS	AM40
VSS	AM36
VSS	AM33
VSS	AM29
VSS	AM24

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
VSS	AM23
VSS	AM20
VSS	AM11
VSS	AM9
VSS	AM7
VSS	AM4
VSS	AL36
VSS	AL33
VSS	AL31
VSS	AK43
VSS	AJ39
VSS	AJ36
VSS	AJ33
VSS	AJ32
VSS	AH42
VSS	AG37
VSS	AG34
VSS	AF43
VSS	AF37
VSS	AF36
VSS	AF23
VSS	AF21
VSS	AF19
VSS	AF10
VSS	AF9
VSS	AF8
VSS	AF7
VSS	AF6
VSS	AF5
VSS	AE24
VSS	AE22
VSS	AE20
VSS	AE18

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
VSS	AE4
VSS	AE3
VSS	AE2
VSS	AD42
VSS	AD39
VSS	AD37
VSS	AD35
VSS	AD33
VSS	AD25
VSS	AD23
VSS	AD21
VSS	AD19
VSS	AC38
VSS	AC35
VSS	AC24
VSS	AC22
VSS	AC20
VSS	AC18
VSS	AC10
VSS	AC7
VSS	AC5
VSS	AB43
VSS	AB25
VSS	AB23
VSS	AB21
VSS	AB19
VSS	AB2
VSS	AB1
VSS	AA38
VSS	AA35
VSS	AA24
VSS	AA22
VSS	AA20

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
VSS	AA18
VSS	AA8
VSS	AA5
VSS	Y42
VSS	Y37
VSS	Y35
VSS	Y33
VSS	Y25
VSS	Y23
VSS	Y21
VSS	Y19
VSS	Y10
VSS	Y7
VSS	Y5
VSS	Y1
VSS	W24
VSS	W22
VSS	W20
VSS	W3
VSS	V43
VSS	V39
VSS	V37
VSS	V34
VSS	V32
VSS	V30
VSS	V29
VSS	V11
VSS	V8
VSS	V5
VSS	V2
VSS	U38
VSS	U35
VSS	U29

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
VSS	U27
VSS	U8
VSS	U7
VSS	U5
VSS	T42
VSS	T1
VSS	R36
VSS	R33
VSS	R31
VSS	R21
VSS	R11
VSS	R8
VSS	R5
VSS	R3
VSS	P43
VSS	P30
VSS	P21
VSS	P18
VSS	P17
VSS	P2
VSS	N36
VSS	N33
VSS	N31
VSS	N27
VSS	N21
VSS	N13
VSS	N10
VSS	N7
VSS	N5
VSS	M37
VSS	M35
VSS	M33
VSS	M27

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
VSS	M21
VSS	M20
VSS	M17
VSS	M15
VSS	M11
VSS	M10
VSS	M7
VSS	M1
VSS	L40
VSS	L33
VSS	L32
VSS	L31
VSS	L29
VSS	L21
VSS	L20
VSS	L11
VSS	L7
VSS	L5
VSS	L3
VSS	K43
VSS	K26
VSS	K21
VSS	K18
VSS	K13
VSS	K12
VSS	K2
VSS	J38
VSS	J35
VSS	J32
VSS	J27
VSS	J21
VSS	J9
VSS	J7

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
VSS	J5
VSS	H31
VSS	H29
VSS	H21
VSS	H20
VSS	H17
VSS	H15
VSS	H13
VSS	G42
VSS	G38
VSS	G32
VSS	G21
VSS	G13
VSS	G12
VSS	G11
VSS	G9
VSS	G7
VSS	G1
VSS	F37
VSS	F35
VSS	F27
VSS	F21
VSS	F18
VSS	F15
VSS	F3
VSS	E43
VSS	E32
VSS	E24
VSS	E21
VSS	E11
VSS	E9
VSS	E3
VSS	E1

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
VSS	D40
VSS	D31
VSS	D21
VSS	D17
VSS	D16
VSS	D15
VSS	D3
VSS	C43
VSS	C26
VSS	C11
VSS	C6
VSS	C5
VSS	C4
VSS	C1
VSS	B37
VSS	B32
VSS	B31
VSS	B26
VSS	B23
VSS	B22
VSS	B19
VSS	B14
VSS	B10
VSS	A41
VSS	A39
VSS	A34
VSS	A26
VSS	A18
VSS	A12
VSS	A7
VSS	A5
VSS	A3
VTT_FSB	R27

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
VTT_FSB	R26
VTT_FSB	R24
VTT_FSB	R23
VTT_FSB	P29
VTT_FSB	P27
VTT_FSB	P26
VTT_FSB	P24
VTT_FSB	P23
VTT_FSB	N29
VTT_FSB	N26
VTT_FSB	N24
VTT_FSB	N23
VTT_FSB	M29
VTT_FSB	M24
VTT_FSB	M23
VTT_FSB	L24
VTT_FSB	L23

Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
VTT_FSB	K24
VTT_FSB	K23
VTT_FSB	J24
VTT_FSB	J23
VTT_FSB	H24
VTT_FSB	H23
VTT_FSB	G26
VTT_FSB	G24
VTT_FSB	G23
VTT_FSB	F26
VTT_FSB	F24
VTT_FSB	F23
VTT_FSB	E29
VTT_FSB	E27
VTT_FSB	E26
VTT_FSB	E23
VTT_FSB	D29

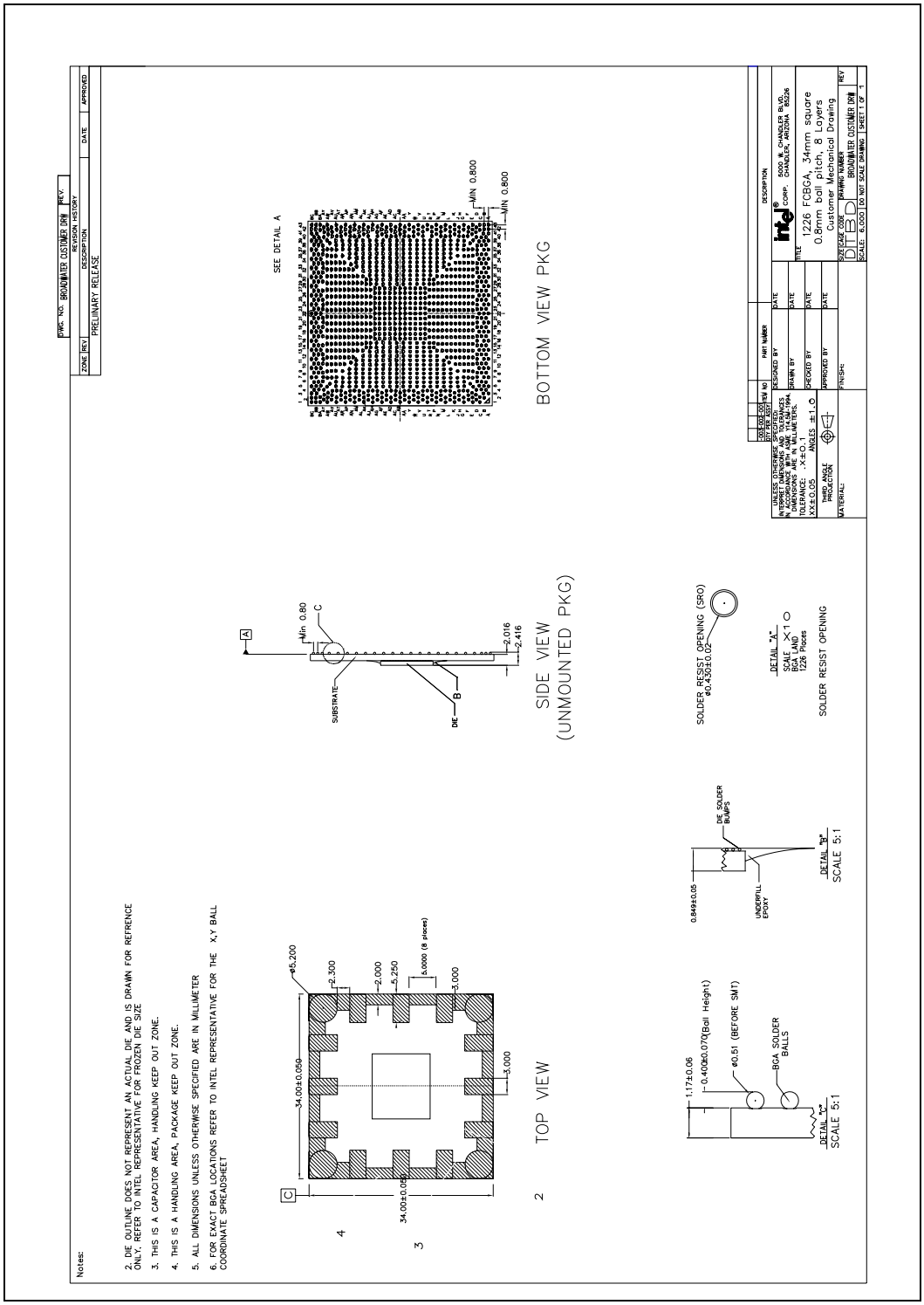
Table 12-2. Ballout – Sorted by Signal

Signal Name	Ball
VTT_FSB	D28
VTT_FSB	D27
VTT_FSB	C30
VTT_FSB	C29
VTT_FSB	C27
VTT_FSB	B30
VTT_FSB	B29
VTT_FSB	B28
VTT_FSB	B27
VTT_FSB	A30
VTT_FSB	A28
XORTEST	F20

13 Package Specifications

The (G)MCH is available in a 34 mm [1.34 in] x 34 mm [1.34 in] Flip Chip Ball Grid Array (FC-BGA) package with 1226 solder balls. The (G)MCH package uses a “balls anywhere” concept. Minimum ball pitch is 0.8 mm [0.031 in], but ball ordering does not follow a 0.8 mm grid. Figure 13-1 shows the package dimensions.

Figure 13-1. (G)MCH Package Drawing



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14 Testability

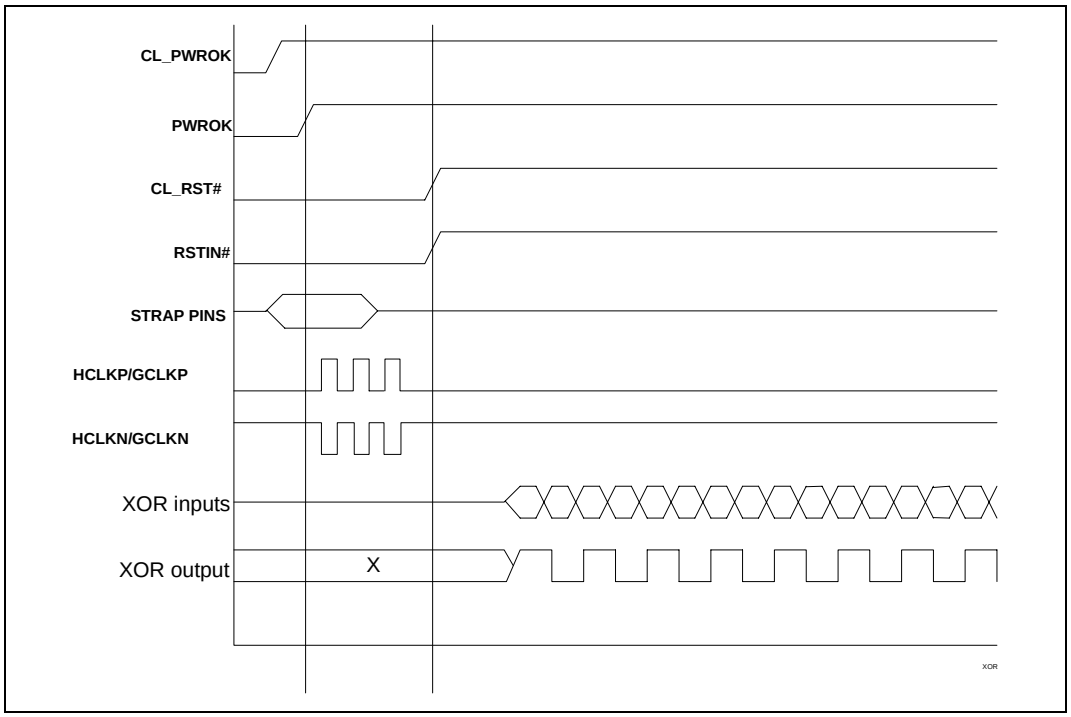
In the (G)MCH, testability for Automated Test Equipment (ATE) board level testing has been implemented as an XOR chain. An XOR-tree is a chain of XOR gates each with one input pin connected to it which allows for pad to ball to trace connection testing.

The XOR testing methodology is to boot the part using straps to enter XOR mode (A description of the boot process follows). Once in XOR mode, all of the pins of an XOR chain are driven to logic 1. This action will force the output of that XOR chain to either a 1 if the number of the pins making up the chain is even or a 0 if the number of the pins making up the chain is odd.

Once a valid output is detected on the XOR chain output, a walking 0 pattern is moved from one end of the chain to the other. Every time the walking 0 is applied to a pin on the chain, the output will toggle. If the output does not toggle, there is a disconnect somewhere between die, package, and board and the system can be considered a failure.

14.1 XOR Test Mode Initialization

Figure 14-1. XOR Test Mode Initialization Cycles



The above figure shows the wave forms to be able to boot the part into XOR mode. The straps that need to be controlled during this boot process are BSEL[2:0], SDVO_CTRLDATA, EXP_EM, EXP_SLR, and XORTEST.

On Broadwater platforms, all strap values must be driven before PWROK asserts. BSEL0 must be a 1. BSEL[2:1] need to be defined values, but logic value in any order will do. XORTEST must be driven to 0.

If SDVO is present in the design, SDVO_CTRLDATA must be pulled to logic 1. Depending on if Static Lane Reversal is used and if the SDVO/PCI Express Coexistence is selected, EXP_SLR and EXP_EN must be pulled in a valid manner.

Because of the different functionalities of the SDVO/PCI Express interface, not all of the pins will be used in all implementations. Due to the need to minimize test points and unnecessary routing, the XOR Chain 14 is dynamic depending on the values of SDVO_CTRLDATA, EXP_SLR, and EXP_EN. See Table 14-1 for what parts of XOR Chain 14 become valid XOR inputs depending on the use of SDVO_CTRLDATA, EXP_SLR, and EXP_EN.

Table 14-1. XOR Chain 14 functionality

SDVO_CTRLDATA	EXP_EN	EXP_SLR	XOR Chain 14
0	1	0	EXP_RXP[15:0] EXP_RXN[15:0] EXP_TXP[15:0] EXP_TXN[15:0]
0	1	1	EXP_RXP[15:0] EXP_RXN[15:0] EXP_TXP[15:0] EXP_TXN[15:0]
1	0	0	EXP_RXP[15:8] EXP_RXN[15:8] EXP_TXP[15:8] EXP_TXN[15:8]
1	0	1	EXP_RXP[7:0] EXP_RXN[7:0] EXP_TXP[7:0] EXP_TXN[7:0]
1	1	0	EXP_RXP[15:0] EXP_RXN[15:0] EXP_TXP[15:0] EXP_TXN[15:0]
1	1	1	EXP_RXP[15:0] EXP_RXN[15:0] EXP_TXP[15:0] EXP_TXN[15:0]

14.2 XOR Chain Definition

The (G)MCH chipset has 15 XOR chains. The XOR chain outputs are driven out on the following output pins. During full-width testing, XOR chain outputs will be visible on both pins.

Table 14-2. XOR Chain Outputs

XOR Chain	Output Pins	Coordinate Location
xor_out0	ALLZTEST	K20
xor_out1	XORTEST	F20
xor_out2	ICH_SYNC#	J13
xor_out3	RSVD	F17
xor_out4	RSVD	AA9
xor_out5	RSVD	AA10
xor_out6	BSEL1	J20
xor_out7	BSEL2	J18
xor_out8	RSVD	AA11
xor_out9	RSVD	Y12
xor_out10	EXP_SLR	E18
xor_out11	EXP_EN	J17
xor_out12	MTYPE	G18
xor_out13	RSVD	K17
xor_out14	BSEL0	G20

14.3 XOR Chains

The following tables lists the XOR chains.

Table 14-3. XOR Chain 0		
Pin Count	**Ball**	**Signal Name**
1	B33	FSB_DB_58
2	D35	FSB_DB_49
3	B40	FSB_DB_55
4	E41	FSB_DB_50
5	C40	FSB_DB_53
6	B41	FSB_DB_51
7	A32	FSB_DB_62
8	B35	FSB_DB_61
9	C33	FSB_DB_48
10	C35	FSB_DB_54
11	D38	FSB_DB_56
12	D37	FSB_DB_57
13	D42	FSB_DB_52
14	C34	FSB_DB_60
15	D32	FSB_DB_63
16	D33	FSB_DB_59
17	B34	FSB_DB_31
18	A37	FSB_DB_26
19	B39	FSB_DB_24
20	D41	FSB_DB_17
21	C42	FSB_DB_16
22	C39	FSB_DB_23
23	E37	FSB_DB_22
24	E35	FSB_DB_28
25	E42	FSB_DB_20
26	F38	FSB_DB_18
27	E39	FSB_DB_21
28	G33	FSB_DB_25
29	F33	FSB_DB_27

Table 14-3. XOR Chain 0		
Pin Count	**Ball**	**Signal Name**
30	G37	FSB_DB_19
31	H32	FSB_DB_30
32	K32	FSB_DB_29
33	F29	FSB_DB_41
34	H26	FSB_DB_44
35	J26	FSB_DB_46
36	G31	FSB_DB_37
37	F32	FSB_DB_33
38	F31	FSB_DB_39
39	E31	FSB_DB_35
40	J29	FSB_DB_40
41	M26	FSB_DB_47
42	L26	FSB_DB_45
43	J31	FSB_DB_32
44	K27	FSB_DB_43
45	L27	FSB_DB_42
46	K29	FSB_DB_38
47	K31	FSB_DB_36
48	M31	FSB_DB_34
49	J41	FSB_DB_11
50	R42	FSB_DB_4
51	F42	FSB_DB_15
52	M39	FSB_DB_5
53	F41	FSB_DB_14
54	G40	FSB_DB_13
55	J39	FSB_DB_9
56	K41	FSB_DB_12
57	N40	FSB_DB_3
58	N41	FSB_DB_6

Table 14-3. XOR Chain 0		
Pin Count	**Ball**	**Signal Name**
59	R41	FSB_DB_2
60	L42	FSB_DB_10
61	L41	FSB_DB_8
62	P41	FSB_DB_1
63	N42	FSB_DB_7
64	R40	FSB_DB_0

Table 14-4. XOR Chain 1

Pin Count	Ball #	Signal Name
1	L37	FSB_AB_6
2	N35	FSB_AB_15
3	L36	FSB_AB_7
4	L39	FSB_AB_4
5	M38	FSB_AB_11
6	L38	FSB_REQB_2
7	J37	FSB_REQB_4
8	N34	FSB_AB_10
9	L35	FSB_REQB_1
10	F40	FSB_REQB_0
11	M34	FSB_ADSTBB_0
12	M36	FSB_AB_13
13	N37	FSB_AB_12
14	J40	FSB_AB_5
15	K42	FSB_AB_8
16	R34	FSB_AB_14
17	N32	FSB_AB_9
18	N38	FSB_AB_16
19	G43	FSB_REQB_3
20	J42	FSB_AB_3
21	Y38	FSB_AB_33
22	Y34	FSB_AB_29

Table 14-4. XOR Chain 1

Pin Count	Ball #	Signal Name
23	V42	FSB_AB_30
24	R35	FSB_AB_26
25	U36	FSB_AB_24
26	U33	FSB_AB_25
27	Y39	FSB_AB_34
28	V33	FSB_AB_27
29	V36	FSB_AB_22
30	R38	FSB_AB_23
31	U34	FSB_ADSTBB_1
32	R37	FSB_AB_19
33	AA37	FSB_AB_35
34	U37	FSB_AB_17
35	N39	FSB_AB_18
36	V38	FSB_AB_31
37	R39	FSB_AB_21
38	Y36	FSB_AB_32
39	V35	FSB_AB_28
40	P42	FSB_AB_20

Table 14-5. XOR Chain 2

Pin Count	Ball #	Signal Name
1	G35	FSB_DSTBPB_1
2	H33	FSB_DSTBNB_1
3	U42	FSB_HITB
4	Y40	FSB_TRDYB
5	AA41	FSB_RSB_1
6	Y43	FSB_HITMB
7	G27	FSB_DSTBPB_2
8	H27	FSB_DSTBNB_2
9	M42	FSB_DSTBPB_0
10	M43	FSB_DSTBNB_0

Table 14-5. XOR Chain 2

Pin Count	Ball #	Signal Name
11	V41	FSB_LOCKB
12	W42	FSB_BNRB
13	C31	FSB_CPURSTB
14	G39	FSB_BPRIB

Table 14-6. XOR Chain 3

Pin Count	Ball #	Signal Name
1	B38	FSB_DSTBPB_3
2	C38	FSB_DSTBNB_3
3	E33	FSB_DINVB_3
4	J33	FSB_DINVB_1
5	U40	FSB_DBSYB
6	U39	FSB_RSB_2
7	W41	FSB_DRDYB
8	U41	FSB_RSB_0
9	T43	FSB_DEFERB
10	G29	FSB_DINVB_2
11	M40	FSB_DINVB_0
12	W40	FSB_ADSB
13	AA42	FSB_BREQ0B

Table 14-7. XOR Chain 4

Pin Count	Ball #	Signal Name
1	BB35	DDR_A_ODT_0
2	AY35	DDR_A_CSB_1
3	AY37	DDR3_A_CSB1
4	BA38	DDR_A_ODT_1
5	BB31	DDR_A_MA_10
6	BA34	DDR_A_CSB_0
7	BB29	DDR3_A_MA0

Table 14-7. XOR Chain 4

Pin Count	Ball #	Signal Name
8	BB30	DDR_A_MA_0
9	AW33	DDR_A_CKB_2
10	AV33	DDR_A_CK_2
11	AR31	DDR_A_CK_0
12	AU31	DDR_A_CKB_0
13	AN27	DDR_A_CKB_1
14	AP27	DDR_A_CK_1
15	BA21	DDR_A_MA_9
16	BA23	DDR_A_MA_2
17	BB23	DDR_A_MA_3
18	AY23	DDR_A_MA_4
19	BB21	DDR_A_MA_7
20	AW18	DDR_A_CKE_1
21	BB22	DDR_A_MA_5
22	AY25	DDR_A_MA_1
23	AW21	DDR_A_MA_8
24	BA22	DDR_A_MA_6
25	AY19	DDR_A_CKE_0
26	AU18	DDR_A_DQSB_3
27	AN18	DDR_A_DM_3
28	BA6	DDR_A_DQSB_2
29	BB6	DDR_A_DM_2
30	AW1	DDR_A_DQSB_1
31	AW3	DDR_A_DM_1
32	AP3	DDR_A_DQSB_0
33	AN2	DDR_A_DM_0

Table 14-8. XOR Chain 5

Pin Count	Ball #	Signal Name
1	AC41	DDR_A_DQSB_7
2	AC40	DDR_A_DM_7
3	AG41	DDR_A_DQSB_6
4	AG40	DDR_A_DM_6
5	AL40	DDR_A_DQSB_5
6	AM43	DDR_A_DM_5
7	AR40	DDR_A_DQSB_4
8	AU43	DDR_A_DM_4
9	AY38	DDR_A_MA_13
10	AW35	DDR_A_CASB
11	AY31	DDR_A_BS_1
12	BA31	DDR_A_BS_0
13	BB34	DDR3_A_WEB
14	AY33	DDR_A_RASB
15	BA33	DDR_A_WEB
16	AY20	DDR_A_BS_2
17	AY21	DDR_A_MA_11
18	BA19	DDR_A_MA_14
19	BC20	DDR_A_MA_12

Table 14-9. XOR Chain 6

Pin Count	Ball #	Signal Name
1	AC42	DDR_A_DQS_7
2	AB41	DDR_A_DQ_58
3	AE42	DDR_A_DQ_60
4	AD43	DDR_A_DQ_57
5	AB42	DDR_A_DQ_63
6	AA40	DDR_A_DQ_59
7	AC39	DDR_A_DQ_62
8	AE41	DDR_A_DQ_61

Table 14-9. XOR Chain 6

Pin Count	Ball #	Signal Name
9	AD40	DDR_A_DQ_56
10	AG42	DDR_A_DQS_6
11	AH43	DDR_A_DQ_49
12	AE40	DDR_A_DQ_51
13	AJ41	DDR_A_DQ_53
14	AF42	DDR_A_DQ_55
15	AF41	DDR_A_DQ_54
16	AJ42	DDR_A_DQ_52
17	AJ40	DDR_A_DQ_48
18	AF39	DDR_A_DQ_50
19	AL41	DDR_A_DQS_5
20	AL39	DDR_A_DQ_47
21	AN40	DDR_A_DQ_44
22	AM39	DDR_A_DQ_41
23	AL42	DDR_A_DQ_46
24	AN41	DDR_A_DQ_40
25	AK42	DDR_A_DQ_42
26	AN42	DDR_A_DQ_45
27	AK41	DDR_A_DQ_43
28	AR41	DDR_A_DQS_4
29	AV40	DDR_A_DQ_36
30	AV42	DDR_A_DQ_32
31	AP41	DDR_A_DQ_39
32	AN39	DDR_A_DQ_35
33	AU40	DDR_A_DQ_33
34	AV41	DDR_A_DQ_37
35	AP42	DDR_A_DQ_34
36	AR42	DDR_A_DQ_38
37	AT20	DDR_A_DQS_3
38	AR18	DDR_A_DQ_25
39	AU21	DDR_A_DQ_26
40	AV20	DDR_A_DQ_31
41	AP20	DDR_A_DQ_30

Table 14-9. XOR Chain 6

Pin Count	Ball #	Signal Name
42	AT18	DDR_A_DQ_24
43	AN17	DDR_A_DQ_29
44	AT21	DDR_A_DQ_27
45	AP17	DDR_A_DQ_28
46	AY7	DDR_A_DQS_2
47	BB9	DDR_A_DQ_19
48	BC7	DDR_A_DQ_22
49	BA9	DDR_A_DQ_18
50	AY6	DDR_A_DQ_17
51	BB4	DDR_A_DQ_21
52	AY9	DDR_A_DQ_23
53	BB5	DDR_A_DQ_16
54	BA5	DDR_A_DQ_20
55	AW2	DDR_A_DQS_1
56	AY3	DDR_A_DQ_15
57	BA4	DDR_A_DQ_10
58	BB3	DDR_A_DQ_11
59	AY2	DDR_A_DQ_14
60	AV4	DDR_A_DQ_8
61	AV3	DDR_A_DQ_9
62	AU1	DDR_A_DQ_13
63	AU2	DDR_A_DQ_12
64	AP2	DDR_A_DQS_0
65	AR2	DDR_A_DQ_2
66	AN3	DDR_A_DQ_1
67	AM1	DDR_A_DQ_0
68	AM2	DDR_A_DQ_5
69	AR4	DDR_A_DQ_7
70	AR5	DDR_A_DQ_6
71	AL3	DDR_A_DQ_4
72	AR3	DDR_A_DQ_3

Table 14-10. XOR Chain 7

Pin Count	Ball #	Signal Name
1	BA5	DDR_A_CSB_2
2	BC25	DDR_A_ODT_3
3	BA9	DDR_A_CSB_3
4	BC21	DDR_A_ODT_2
5	AR29	DDR_A_CK_3
6	AR31	DDR_A_CKB_3
7	AU42	DDR_A_CK_5
8	AW6	DDR_A_CKB_5
9	AN11	DDR_A_CK_4
10	AN12	DDR_A_CKB_4
11	BC3	DDR_A_CKE_3
12	AM2	DDR_A_CKE_2
13	AR41	DDR3_DRAMRST

Table 14-11. XOR Chain 8

Pin Count	Ball #	Signal Name
1	AV31	DDR_B_CKB_0
2	AW31	DDR_B_CK_0
3	AT32	DDR_B_CKB_2
4	AU27	DDR_B_CK_1
5	AT27	DDR_B_CKB_1
6	AV32	DDR_B_CK_2
7	BA29	DDR_B_CSB_1
8	AW29	DDR_B_ODT_1
9	BB27	DDR_B_ODT_0
10	BA25	DDR_B_CSB_0
11	BA14	DDR_B_MA_4
12	BB15	DDR_B_MA_1
13	BB13	DDR_B_MA_8
14	BB14	DDR_B_MA_5
15	BA17	DDR_B_MA_10

Table 14-11. XOR Chain 8

Pin Count	Ball #	Signal Name
16	BC12	DDR_B_CKE_1
17	BA13	DDR_B_MA_7
18	BA15	DDR_B_MA_2
19	AW11	DDR_B_CKE_0
20	AY13	DDR_B_MA_9
21	AW15	DDR_B_MA_0
22	AW12	DDR_B_MA_6
23	AY15	DDR_B_MA_3
24	AU26	DDR_B_DQSB_3
25	AP23	DDR_B_DM_3
26	AR15	DDR_B_DQSB_2
27	AW13	DDR_B_DM_2
28	AP12	DDR_B_DQSB_1
29	AW9	DDR_B_DM_1
30	AU5	DDR_B_DQSB_0
31	AR7	DDR_B_DM_0

Table 14-12. XOR Chain 9

Pin Count	Ball #	Signal Name
1	AC37	DDR_B_DQSB_7
2	AD38	DDR_B_DM_7
3	AG36	DDR_B_DQSB_6
4	AG39	DDR_B_DM_6
5	AL34	DDR_B_DQSB_5
6	AM37	DDR_B_DM_5
7	AU39	DDR_B_DQSB_4
8	AU37	DDR_B_DM_4
9	AY27	DDR_B_MA_13
10	AY24	DDR_B_RASB
11	AW26	DDR_B_CASB
12	BB25	DDR_B_WEB

Table 14-12. XOR Chain 9

Pin Count	Ball #	Signal Name
13	AY17	DDR_B_BS_1
14	BB17	DDR_B_BS_0
15	BB11	DDR_B_MA_14
16	AY11	DDR_B_BS_2
17	BA11	DDR_B_MA_12
18	AY12	DDR_B_MA_11

Table 14-13. XOR Chain 10

Pin Count	Ball #	Signal Name
1	AC36	DDR_B_DQS_7
2	AF38	DDR_B_DQ_61
3	AC34	DDR_B_DQ_62
4	AA34	DDR_B_DQ_58
5	AA33	DDR_B_DQ_63
6	AA36	DDR_B_DQ_59
7	AD36	DDR_B_DQ_56
8	AC33	DDR_B_DQ_57
9	AD34	DDR_B_DQ_60
10	AG35	DDR_B_DQS_6
11	AF34	DDR_B_DQ_55
12	AJ38	DDR_B_DQ_49
13	AF33	DDR_B_DQ_51
14	AJ35	DDR_B_DQ_53
15	AG33	DDR_B_DQ_54
16	AG38	DDR_B_DQ_48
17	AJ37	DDR_B_DQ_52
18	AF35	DDR_B_DQ_50
19	AL35	DDR_B_DQS_5
20	AL38	DDR_B_DQ_43
21	AJ34	DDR_B_DQ_42
22	AM34	DDR_B_DQ_45

Table 14-13. XOR Chain 10

Pin Count	Ball #	Signal Name
23	AL32	DDR_B_DQ_47
24	AM38	DDR_B_DQ_41
25	AM35	DDR_B_DQ_40
26	AL37	DDR_B_DQ_46
27	AR39	DDR_B_DQ_44
28	AW39	DDR_B_DQS_4
29	AV38	DDR_B_DQ_33
30	AN35	DDR_B_DQ_38
31	AN36	DDR_B_DQ_34
32	AR37	DDR_B_DQ_39
33	AW37	DDR_B_DQ_32
34	AU35	DDR_B_DQ_36
35	AN37	DDR_B_DQ_35
36	AR35	DDR_B_DQ_37
37	AT24	DDR_B_DQS_3
38	AP26	DDR_B_DQ_27
39	AU23	DDR_B_DQ_28
40	AT23	DDR_B_DQ_25
41	AV24	DDR_B_DQ_24
42	AR24	DDR_B_DQ_30
43	AW23	DDR_B_DQ_29
44	AT26	DDR_B_DQ_26
45	AN26	DDR_B_DQ_31
46	AP15	DDR_B_DQS_2
47	AM13	DDR_B_DQ_21
48	AU15	DDR_B_DQ_16
49	AT17	DDR_B_DQ_19
50	AU17	DDR_B_DQ_18
51	AW17	DDR_B_DQ_23
52	AV13	DDR_B_DQ_17
53	AV15	DDR_B_DQ_22
54	AU13	DDR_B_DQ_20
55	AR12	DDR_B_DQS_1

Table 14-13. XOR Chain 10

Pin Count	Ball #	Signal Name
56	AR11	DDR_B_DQ_12
57	AV12	DDR_B_DQ_14
58	AU11	DDR_B_DQ_9
59	AU12	DDR_B_DQ_15
60	AR13	DDR_B_DQ_11
61	AU9	DDR_B_DQ_13
62	AP13	DDR_B_DQ_10
63	AT11	DDR_B_DQ_8
64	AV6	DDR_B_DQS_0
65	AU7	DDR_B_DQ_7
66	AW7	DDR_B_DQ_3
67	AN6	DDR_B_DQ_5
68	AW5	DDR_B_DQ_2
69	AN9	DDR_B_DQ_6
70	AN5	DDR_B_DQ_4
71	AN7	DDR_B_DQ_0
72	AN8	DDR_B_DQ_1

Table 14-14. XOR Chain 11

Pin Count	Ball #	Signal Name
1	BA30	DDR_B_CSB_3
2	AP32	DDR_B_CKB_5
3	AN33	DDR_B_CK_5
4	AW27	DDR_B_CKB_4
5	AV29	DDR_B_CK_4
6	AR29	DDR_B_CK_3
7	AU29	DDR_B_CKB_3
8	AY29	DDR_B_ODT_3
9	BA27	DDR_B_ODT_2
10	BA26	DDR_B_CSB_2
11	AW32	DDR3_B_ODT3

Table 14-14. XOR Chain 11

Pin Count	Ball #	Signal Name
12	BB10	DDR_B_CKE_3
13	BA10	DDR_B_CKE_2

Table 14-15. XOR Chain 12

Pin Count	Ball #	Signal Name
1	G17	SDVO_CTRLDATA
2	E17	SDVO_CTRLCLK
3	L13	CRT_DDC_DATA
4	M13	CRT_DDC_CLK

Table 14-16. XOR Chain 13

Pin Count	Ball #	Signal Name
1	AA2	DMI_TXN_3
2	Y2	DMI_TXP_3
3	AA4	DMI_RXN_3
4	AB3	DMI_RXP_3
5	AC9	DMI_TXN_2
6	AC8	DMI_TXP_2
7	AA6	DMI_RXN_2
8	AA7	DMI_RXP_2
9	Y4	DMI_TXN_1
10	W4	DMI_TXP_1
11	Y9	DMI_RXN_1
12	Y8	DMI_RXP_1
13	V6	DMI_TXN_0
14	V7	DMI_TXP_0
15	V1	DMI_RXN_0
16	W2	DMI_RXP_0

Table 14-17. XOR Chain 14

Pin Count	Ball #	Signal Name
1	U4	PEG_TXN_15
2	V3	PEG_TXP_15
3	R7	PEG_RXN_15
4	R6	PEG_RXP_15
5	T2	PEG_TXN_14
6	U2	PEG_TXP_14
7	R4	PEG_RXN_14
8	T4	PEG_RXP_14
9	P1	PEG_TXN_13
10	R2	PEG_TXP_13
11	R10	PEG_RXN_13
12	R9	PEG_RXP_13
13	N4	PEG_TXN_12
14	P3	PEG_TXP_12
15	M6	PEG_RXN_12
16	M5	PEG_RXP_12
17	M2	PEG_TXN_11
18	N2	PEG_TXP_11
19	L4	PEG_RXN_11
20	M4	PEG_RXP_11
21	K1	PEG_TXN_10
22	L2	PEG_TXP_10
23	M9	PEG_RXN_10
24	M8	PEG_RXP_10
25	K3	PEG_TXN_9
26	J4	PEG_TXP_9
27	L8	PEG_RXN_9
28	L9	PEG_RXP_9
29	G4	PEG_TXN_8
30	F4	PEG_TXP_8
31	G5	PEG_RXN_8
32	G6	PEG_RXP_8
33	E2	PEG_TXN_7

Table 14-17. XOR Chain 14

Pin Count	Ball #	Signal Name
34	F2	PEG_TXP_7
35	D2	PEG_RXN_7
36	C2	PEG_RXP_7
37	B4	PEG_TXN_6
38	B3	PEG_TXP_6
39	F6	PEG_RXN_6
40	E5	PEG_RXP_6
41	B6	PEG_TXN_5
42	B5	PEG_TXP_5
43	E7	PEG_RXN_5
44	F7	PEG_RXP_5
45	D6	PEG_TXN_4
46	D7	PEG_TXP_4
47	H11	PEG_RXN_4
48	J11	PEG_RXP_4
49	B7	PEG_TXN_3

Table 14-17. XOR Chain 14

Pin Count	Ball #	Signal Name
50	B9	PEG_TXP_3
51	H12	PEG_RXN_3
52	J12	PEG_RXP_3
53	D9	PEG_TXN_2
54	C10	PEG_TXP_2
55	E12	PEG_RXN_2
56	F12	PEG_RXP_2
57	A10	PEG_TXN_1
58	B11	PEG_TXP_1
59	J15	PEG_RXN_1
60	K15	PEG_RXP_1
61	D12	PEG_TXN_0
62	D11	PEG_TXP_0
63	E13	PEG_RXN_0
64	F13	PEG_RXP_0

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