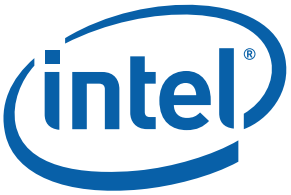

Intel® I/O Controller Hub 6 (ICH6) Family

Specification Update

May 2012

The ICH6 Family product may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Order Number: 301474-030

Contents

Revision History

Revision	Description	Date
1.0	Initial Release.	June 2004
2.0	Modified: Erratum 3-SATA Swap Bay Device Detection, 7-Intel ICH6 Completion Delays Documentation Changes 1-PCI Device Register ID Table updated for B2 stepping. Added: Erratum: 9-Intel ICH6 PCI Express* Completion Timer Not Halting in L1, 10-Intel ICH6 Does Not Send Minimum Number TS2 on PCI Express*, 11-Intel ICH6 PCI Express* Recovery, 12-Intel ICH6 PCI Express* Extended Tag Capability Bit Specification Changes: 1-AHCI SALP Bit Change, 2-V_{IL14} Change Specification Clarifications: 1-IDE Controller Interrupt Status Note Documentation Changes: 2-Input Signal Association Table Correction	August 2004
3.0	Added: Erratum: 13-ICH6 Does Not Ignore a PCI Express* Null Packet, 14-ICH6 PCI Express DLLPs With Unknown Encoding Type, 15-SATA SRST During Link Low Power States Specification Changes: 3-XOR Test Change Specification Clarifications: 2-Table 22-20 Note Corrections, 3-Standard ATA Emulation Clarification, 4-Secondary PCI Bus Reset, 5-EHCI Test Mode Documentation Changes: 3-DC Current Characteristics Table Update	September 2004
4.0	Added: Errata: 16-PCI Express* Replay, 17-ICHR/RW SATA FIS Posting Cycle, 18-USB Output Voltage Specification Changes: SIR28 Change Specification Clarifications: 6-IRQ14/IRQ15 and SERIRQ, 7-t302 Clarification	October 2004
5.0	Added: New Component Marks Errata: 19-ICH6 AHCI Command FIS SYNC Escape, 20-ICH6 ACHI PxCMD.CR Bit, 21-ICH6 High Definition Audio Payload Capabilities Registers, 22-ICH6 PIO Setup FIS Error, 23-ICH6 PCI Express Surprise Removal Specification Changes: 5-Intel Wireless Connect Technology/ICH6W/ICH6RW Defeature, 6-EE_SHCLK Change, 7-INIT3_3V VOL Change Specification Clarifications: 8-EDD (Execute Device Diagnostics) Command Completion Clarification, 9-SMBus Reset Clarification Documentation Changes: 4-AHCI CAP Default Correction, 5-LCTL Corrections Modified: Removed Intel Wireless Connect Technology references	November 2004
6.0	Added: Specification Changes: 8-t214 Change, 9-Peer Cycle Change Documentation Changes: 6-PxSSTS.IPM Correction	December 2004

Revision	Description	Date
7.0	Moved all Specification Changes, Specification Clarifications and Documentation Changes into parent Datasheet (301473-002). Modified: Errata: 11-PCI Express* Recovery Documentation Changes: 1-PCI Device Revision ID Added: ICH6/ICH6-M Marks Errata: 24-PCI Express Scrambling, 25-AHCI PxSERR:[M] Bit, 24-L0s With Extended Sync, 25-ICH6-M DPRSLPVR.	January 2005
8.0	Added: Errata: 28-PATA V-Threshold, 29-PCI Express SKP/InitFCx Contention, 30-DMI L0s Latency Bit Attribute, 31-PCI Express Two DWord Malformed TLP	February 2005
9.0	Moved the following to the parent ICH6 Family Datasheet (301473-002): Errata: 28-PATA V-Threshold, 29-PCI Express SKP/InitFCx Contention, 30-DMI L0s Latency Bit Attribute, 31-PCI Express* Two DWord Malformed TLP Added: Errata: 32-Full-speed USB ISOC End of Packet, 33-ICH6R/ICH6-M AHCI SATA Interlock Switch. Specification Clarifications: 1-t216 Clarification, 2-C2 Support, 3-LPC Cycle Clarification. Document Changes: 2-CAP.SALP, 3-Memory Address Range Addition, 4-D30:F0.PSTS Correction.	March 2005
10.0	Modified: Errata: #11-PCI Express Recovery, #14-Intel(R) ICH6 PCI Express* DLLPs with Unknown Encoding Type Documentation Changes: #1-PCI Device Revision ID. Added: Specification Clarifications: 4-GPIO25 Pull-up, 5-HPET TIMERn_32MODE_CNF, 6-PCI Clock, 7-Reserved Clarification.	April 2005
11.0	Modified: Specification Clarifications: 5-HPET TIMERn_32MODE_CNF Added: Errata: 34-SATA AHCI Recovery From Task File Error Specification Clarifications: 8-PATA Secondary Command/Control BAR Documentation Changes: 5-IDE MSE Bit, 6-PxCMD.ST Bit Description Correction	May 2005
12.0	Modified: Specification Clarification: 8-PATA Secondary Command/Control BAR. Added: Specification Clarifications: 9-F0h Read Behavior Clarifications and 10-Indeterminate State Before Power Stable. Documentation Changes: 7-PCI Functional Description Correction and 8-VRMPWRGD Timing Diagram Corrections.	September 2005
13.0	Added: Specification Clarifications: 11-LPC SERR Generation Behavior Clarification and 12-PCI Downstream Device Disable Clarification. Documentation Changes: 9-THRMTRIP# Timing Correction and 10-LSTS Note Correction.	October 2005
14.0	Added: Document Changes: 11-Interrupt Pin Register Reserved Bits Correction and 12-USB Port Number Documentation Corrections.	November 2005

Revision	Description	Date
15.0	Added: Document Change: 13-LPC Cycle Change	December 2005
16.0	Added: Errata: 35-ASF Decode Erratum	February 2006
17.0	Added: Specification Changes: 1-t200 Change	March 2006
18.0	Added: Errata: 36-MW DMA Mode-1 Tdh Erratum	April 2006
19.0	Added: Specification Clarification: 13-t232 Clarification	May 2006
20.0	Added: Errata: 37-Reset Command Received Through SMBus During Suspend Specification Changes: 2-RSMRST# Timing Addition Specification Clarifications: 14-SMBus Slave Write Cycle Clarification Miscellaneous formatting corrections	July 2006
21.0	Added: Errata: 38-SATA Early SYNC, 39-PCI Express Root Port Power State Value	August 2006
22.0	Added: Errata: 40-PCI Express Upstream Link Base Address Register Bit 0 Documentation Changes: 14-BIOSWE Bit Clarification	September 2006
23.0	Added: Documentation changes:15-APIC Enable (AEN) Bit Clarification, 16-Reset Control Register (CF9h) Clarification	February 2007
24.0	Added: Errata: 41-High Speed (HS) USB 2.0 D+ and D- maximum Driven Signal Level.	September 2007
25.0	Added: Specification Change: 3-Removing Support for USB Wake from S5	November 2007
26.0	Added Identification Information: Added additional ICH6M top marking 82801FPM SLG8L	November 2008
27.0	Added: Errata: 42-Intel® I/O Controller Hub 6 (ICH6) Family PCI Express Function Disable Document Change: 17-Correct Section 5.14.7.5 Sx-G3-Sx, Handling Power Failures regarding possible wake events following a power failure	October 2009
28.0	Added Items: Document Changes: 18- Correct A20M#Signal Description Errata: 43-Intel® ICH6 SATA GEN3 Device Detection	November 2010
29.0	Removed: Errata: 43-Intel® ICH6 SATA GEN3 Device Detection	March 2011
30.0	Added Item: - Errata: 43- Incorrect IRQ(x) Vector Returned for 8259 Interrupts With RAEOI Enabled - Specification Change: 4- ROAEI options removal for OCW2.	May 2012

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Document Number
Intel® I/O Controller Hub 6 (ICH6) Family Datasheet	301473-002

Nomenclature

Errata are design defects or errors. Errata may cause the ICH6's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the Intel® I/O Controller Hub 6 (ICH6) family. Intel intends to fix some of the errata in a future stepping of the component(s), and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X: Specification Change, Erratum, Specification Clarification or Documentation Change that applies to a stepping or to this product line.

(No mark) or (Blank Box):This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc: Document change or update that will be implemented.

PlanFix: This erratum may be fixed in a future stepping of the product.

Fixed: This erratum has been previously fixed.

No Fix: There are no plans to fix this erratum.

Bar: This item is either new or modified from the previous version of the document.

Errata

Erratum Number	Stepping			Status	ERRATA
	B1	B2	C0		
1.	X	X	X	No Fix	SATA COMINIT/COMWAKE Detection
2.	X	X	X	No Fix	PCI Express* Common Mode Voltage Noise Immediately Following Receiver Detect Sequence
3.	X			Fixed	SATA Swap Bay Device Detection
4.	X	X	X	No Fix	Intel® ICH6 SATA Sending Less Than Minimum Number of PMACK
5.	X	X	X	No Fix	Intel® ICH6 Improper Length Register Device-to-Host FIS
6.	X	X	X	No Fix	Intel® ICH6 Split Lock LPC Cycle
7.	X			Fixed	Intel® ICH6 Completion Delays
8.	X	X	X	No Fix	Intel® ICH6 SATA Signal Voltage Level

Errata

Erratum Number	Stepping			Status	ERRATA
	B1	B2	C0		
9.	X	X	X	No Fix	Intel® ICH6 PCI Express* Completion Timer Not Halting in L1
10.	X	X		Fixed	IIntel® ICH6 Does Not Send Minimum Number TS2 on PCI Express*
11.	X	X		Fixed (DT)	PCI Express* Recovery
12.	X	X	X	No Fix	Intel® ICH6 PCI Express* Extended Tag Capability Bit
13.	X	X	X	No Fix	Intel® ICH6 Does Not Ignore a PCI Express* Null Packet
14.	X	X	X	No Fix	Intel® ICH6 PCI Express* DLLPs with Unknown Type Encoding
15.	X	X	X	No Fix	SATA SRST during Link Low Power States
16.	X	X	X	No Fix	PCI Express* Replay
17.	X	X	X	No Fix	Intel® ICH6R SATA FIS Posting Cycle
18.	X	X	X	No Fix	USB Output Voltage
19.	X	X	X	No Fix	Intel® ICH6 AHCI Command FIS SYNC Escape
20.	X	X	X	No Fix	Intel® ICH6 AHCI PxCMD.CR Bit
21.	X	X	X	No Fix	Intel® ICH6 High Definition Audio Payload Capabilities Registers
22.	X	X	X	No Fix	Intel® ICH6 PIO Setup FIS Error
23.	X	X	X	No Fix	Intel® ICH6 PCI Express* Surprise Removal
24.	X	X	X	No Fix	PCI Express* Scrambling
25.	X	X	X	No Fix	AHCI PxSERR:[M] Bit
26.	X	X	X	No Fix	L0s With Extended Sync
27.	X	X	X	No Fix	Intel® ICH6-M DPRSLPVR
28.	X	X	X	No Fix	PATA V- Threshold
29.	X	X	X	No Fix	PCI Express* SKP/InitFCx Contention
30.	X	X	X	No Fix	DMI L0s Latency Bit Attribute
31.	X	X	X	No Fix	PCI Express* Two DWord Malformed TLP
32.	X	X	X	No Fix	Full speed USB ISOC End of Packet
33.	X	X	X	No Fix	AHCI SATA Interlock Switch
34.	X	X	X	No Fix	SATA AHCI Recovery From Task File Error
35.	X	X	X	No Fix	ASF Decode Erratum
36.	X	X	X	No Fix	MW DMA Mode-1 Tdh Erratum
37.	X	X	X	No Fix	Reset Command Received Through SMBus During Suspend
38.	X	X	X	No Fix	SATA Early SYNC
39.	X	X	X	No Fix	PCI Express* Root Port Power State Value
40.	X	X	X	No Fix	PCI Express* Upstream Link Base Address Register Bit 0

Errata

Erratum Number	Stepping			Status	ERRATA
	B1	B2	C0		
41.	X	X	X	No Fix	High Speed (HS) USB2.0 D+ and D- Maximum Driven Signal Level
42.	X	X	X	No Fix	Intel® I/O Controller Hub 6 (ICH6) Family PCI Express Function Disable
43.	X	X	X	No Fix	Incorrect IRQ(x) Vector Returned for 8259 Interrupts With RAEOI Enabled

Specification Changes

Spec Change Number	Stepping			SPECIFICATION CHANGES
	B1	B2	C0	
1	X	X	X	t200 change
2	X	X	X	RSMRST# Timing Addition
3	X	X	X	Removing Support for USB Wake from S5
4	X	X	X	ROAEI options removal for OCW2

Specification Clarifications

No.	SPECIFICATION CLARIFICATIONS
1	t216 Clarification
2	C2 Support
3	LPC Cycle Clarification
4	GPIO25 Pull-up
5	HPET TIMERn_32MODE_CNF
6	PCI Clock
7	Reserved Clarification
8	PATA Secondary Command/Control BAR
9	F0h Read Behavior Clarifications
10	Indeterminate State Before Power Stable
11	LPC SERR Generation Behavior Clarification
12	PCI Downstream Device Disable Clarification
13	t232 Clarification
14	SMBus Slave Write Cycle Clarification

Documentation Changes

No.	DOCUMENTATION CHANGES
1	PCI Device Revision ID
2	CAP.SALP
3	Memory Address Range Addition
4	D30:F0 PSTS Correction
5	IDE MSE Bit
6	PxCMD.ST Bit Description Correction
7	PCI Functional Description Correction
8	VRMPWRGD Timing Diagram Corrections
9	THRMTRIP# Timing Correction
10	LSTS Note Correction
11	Interrupt Pin Register Reserved Bits Correction
12	USB Port Number Documentation Corrections.
13	LPC Cycle Change
14	BIOSWE Bit Clarification
15	APIC Enable (AEN) Bit Clarification
16	Reset Control Register (CF9h) Clarification
17	Correct Section 5.14.7.5 Sx-G3-Sx Handling Power Failures regarding possible wake events following a power failure
18	Correct A20M#Signal Description

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Identification Information

Markings

ICH6 Stepping	S-Spec	Top Marking	Notes
B1	N/A	82801FB QF88ES	Engineering Sample ICH6
B1	SL7AG	82801FB SL7AG	Production ICH6
B1	N/A	82801FB QG36ES	Engineering Sample ICH6 (Lead-free)
B1	N/A	82801FR QF89ES	Engineering Sample ICH6R
B1	SL79N	82801FR SL79N	Production ICH6R
B1	N/A	82801FRW QF91ES	Not Supported
B1	SL7LT	82801FRW SL7LT	Not Supported
B1	N/A	82801FW QF92ES	Not Supported
B1	SL7LM	82801FW SL7LM	Not Supported
B2	N/A	82801FB QH16ES	Engineering Sample ICH6
B2	SL7Y5	82801FB SL7Y5	Production ICH6
B2	N/A	82801FB QI29ES	Engineering Sample ICH6 (Lead-free)
B2	SL89L	82801FB SL89L	Production ICH6 (Lead-free)
B2	N/A	82801FR QH17ES	Engineering Sample ICH6R
B2	SL7W7	82801FR SL7W7	Production ICH6R
B2	N/A	82801FR QI46ES	Engineering Sample ICH6R (Lead-free)
B2	SL89J	82801FR SL89J	Production ICH6R (Lead-free)
B2	N/A	82801FBM QG87ES	Engineering Sample ICH6-M
B2	SL7W6	82801FBM SL7W6	Production ICH6-M
B2	N/A	82801FBM QH58ES	Engineering Sample ICH6-M (Lead-free)
B2	SL89K	82801FBM SL89K	Production ICH6-M (Lead-free)
B2	SLG8L	82801FPM SLG8L	Production ICH6-M (Lead-free)
C0	N/A	82801FB QI08ES	Engineering Sample ICH6
C0	SL8BZ	82801FB SL8BZ	Production ICH6
C0	N/A	82801FR QH82ES	Engineering Sample ICH6R
C0	SL8C2	82801FR SL8C2	Production ICH6R

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Errata

1. SATA COMINIT/COMWAKE Detection

Problem: During Out-Of-Band (OOB) sequencing, the Intel® ICH6 may detect COMINIT/COMWAKE when only 2 or 3 bursts of ALIGNs are received from the SATA device instead of the required 4 bursts as per the SATA 1.0a Specification.

Implication: None Known - The Intel® ICH6 appropriately handles subsequent ALIGNs.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

2. PCI Express* Common Mode Voltage Noise Immediately Following Receiver Detect Sequence

Problem: The PCI Express common mode voltage is not stable immediately after Receiver Detect Sequence when entering Polling.Active from Detect.Active states.

Implication: Common mode voltage noise may result in bit errors early in Polling.Active state. This may result in additional training time before transitioning on to Polling.Configuration.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

3. SATA Swap Bay Device Detection

Problem: During non-AHCI SATA swap bay operation with slave device while master is present, slave device task file may stay at 00h if slave device not ready.

Implication: Slave SATA device swapped may not be detected.

Workaround: None.

Status: Fixed in B-2 stepping. For steppings affected, see the *Summary Tables of Changes*.

4. Intel® ICH6 SATA Sending Less Than Minimum Number of PMACK

Problem: The SATA Spec requires the Intel® ICH6 to send at least four PMACKs (Power Management Acknowledgments) to the SATA device. Intel® ICH6 sends only three PMACKs before entering a lower power state after the device requests partial or slumber state on the SATA bus.

Implication: None known. The SATA Specification intent is to provide four PMACK messages to provide redundancy thru repetition. the device is required to operate after receiving only one PMACK.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

5. Intel® ICH6 Improper Length Register Device-to-Host FIS

Problem: If a SATA device sends less than a 5 DWord Register Device-to-Host FIS, the Intel® ICH6 will correctly respond with RERR but may not be able to accept any further FISes from the device.

Implication: SATA bus will hang.

Note: This only applies while operating in AHCI mode.

Note: No known devices use Register Device-to-Host FIS sizes less than 5 DWords, as these are not allowed by the Serial ATA Specification, rev 1.0a.

Workaround: The AHCI driver shall reset the bus by sending COMRESET, per the AHCI spec.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

6. Intel® ICH6 Split Lock LPC Cycle

Problem: ICH6 may not properly complete non-DWord aligned locked cycles to LPC.

Implication: System Hang.

This issue has only been replicated using a synthetic test environment and has not been reported using commercially available hardware/software.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

7. Intel® ICH6 Completion Delays

Problem: Intel® ICH6 internal devices or devices connected to the ICH6 may experience additional completion delays of up to 40 usec.

Implication: No end user functional impact expected.

Most ICH6 devices are buffered adequately to withstand an additional 40 usec delay.

The UHCI (Full-speed only) may experience underruns and PCI may experience downstream request delays. Both implications are allowable their respective industry specifications.

Workaround: None.

Status: Fixed in B-2 stepping. For steppings affected, see the *Summary Tables of Changes*.

8. Intel® ICH6 SATA Signal Voltage Level

Problem: The Intel® ICH6 SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, the Intel® ICH6 Serial ATA (SATA) transmit signaling voltage levels may exceed the maximum motherboard TX connector and device RX connector voltage specifications (section 6.6.2 of SATA Specification, rev 1.0a).

Implication: None known.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

9. Intel® ICH6 PCI Express* Completion Timer Not Halting in L1

Problem: The Intel® ICH6 PCI Express Completion Timer does not halt when the link enters the L1 state.

Implication: The Intel® ICH6 will flag a completion error:

Note: This requires a device that is not fully compliant with the PCI Express* specification and has only been replicated in a synthetic test environment.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

10. Intel® ICH6 Does Not Send Minimum Number TS2 on PCI Express*

Problem: On PCI Express*, the ICH6 transitions to Recovery.Idle after sending 9 TS2s (Training Order Sets) after receiving the first TS2 from the endpoint. The PCI Express specification requires that the Intel® ICH6 send a minimum of 16 TS2s after detecting the first TS2.

Implication: If the endpoint is unable to consecutively receive 8 of the 9 transmitted TS2s within 48 ms, the endpoint will transition to the Detect state and reattempt training. All known production devices have been able to properly train after receiving 9 TS2s.

Workaround: None.

Status: Fixed in C0. For steppings affected, see the *Summary Tables of Changes*.

11. PCI Express* Recovery

Problem: On PCI Express* L0s and L1 Exit, the Intel® ICH6 may fail to train to L0 and initiate Recovery.

Implication: ICH6 PCI Express interface times out during the Recovery state, which results in PCI Express link down conditions, sporadic recovery transitions, and possible system hangs.

Workaround: (Desktop) None necessary: L0s/L1 states are not enabled by the current desktop BIOS recommendations.

Workaround: (Mobile) BIOS Workaround. BIOS should do the following:

1. Ensure that bits [1:0] of Link Control register (D28:F0/F1/F2/F3:Offset 50h:[1:0] are 00b (power on default value) for all Intel® ICH6-M PCI Express root ports in the system.
2. In the ACPI_OSC control method, return the capabilities dword with bit-6 = 0 indicating that ASPM control should not be transferred to the OS with native PCI Express support.

Status: Fixed in C0 (Desktop). For steppings affected, see the *Summary Tables of Changes*.

12. Intel® ICH6 PCI Express* Extended Tag Capability Bit

Problem: The Intel® ICH6 incorrectly has the PCI Express* Extended Tags Supported capability bit (D28:F0/F1/F2/F3:Offset 44h bit-5) set to '1', though the ICH6 does not support Extended Tags.

Implication: Software will not be able to implement Extended Tags support.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

13. Intel® ICH6 Does Not Ignore a PCI Express* Null Packet

Problem: If the Intel® ICH6 receives a PCI Express* Null packet, it should drop the packet and not perform sequence number checking or respond with any ACK or NAK DLLP. The Intel® ICH6 still performs sequence number checks for Null packets and may respond with an ACK or NAK depending on the result of the check.

Implication: ICH6 may send ACK or NAK DLLPs in response to a Null packet. This may degrade link performance due to unnecessary retries.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

14. Intel® ICH6 PCI Express* DLLPs with Unknown Type Encoding

Problem: If the Intel® ICH6 receives a DLLP on PCI Express* with an unknown type encoding, the ICH6 may interpret the packet as an ACK or NAK.

Implication: The Intel® ICH6 may interpret the ACK as being from an outstanding TLP sent to the device, indicating that the device received the TLP. Or, the Intel® ICH6 may flag a DLLP protocol error if the sequence number is not appropriate. If the Intel® ICH6 interprets the packet as a NAK, needless replay may occur.

Note: This requires PCI Express* rev 1.0a and rev 1.1 noncompliant devices or require a future revision of the PCI Express spec to expand into currently undefined type encodings.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

15. SATA SRST during Link Low Power States

Problem: When exiting SATA link partial or slumber states, the Intel®ICH6 may not send a SRST when instructed by software.

Implication: The device will not appear available to software until SRST is re-tried.

Workaround: BIOS workaround available.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

16. PCI Express* Replay

Problem: The Intel® ICH6 PCI Express* port's receiver does not properly recognize a ACK packet from a device when the ICH6 is replaying a packet.

Implication: PCI Express link may halt, resulting in a system hang.

This issue has only been replicated using a synthetic test environment using targeted error injection testing.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

17. Intel® ICH6R SATA FIS Posting Cycle

Problem: In only AHCI mode (ICH6R), the SATA controller may post a FIS incorrectly if either an unsolicited COMINIT arrives or if software performs a port reset, while FIS posting is pending internally.

Implication: Both a malformed TLP is delivered and inappropriate data is delivered on the next upstream cycle.

Note: This has only been replicated in a synthetic test environment and has not been reproduced in a real world environment.

Workaround: None. The system can be configured to detect this anomalous condition and reset the system to prevent this data migration. Refer to the ICH6 BIOS Specification for implementation details.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

18. USB Output Voltage

Problem: Intel® ICH6 High Speed USB 2.0 V_{HSOL} and V_{HSOH} may not meet the USB 2.0 specification.

The maximum expected V_{HSOL} is 60 mV and the maximum expected V_{HSOH} is 470 mV.

Implication: None known.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

19. Intel® ICH6 AHCI Command FIS SYNC Escape

Problem: If the Intel® ICH6 SATA controller is operating in AHCI mode and a device sends a SYNC escape, the Intel® ICH6 retries the Command FIS (CFIS) sent to the device. The SATA spec requires that the Intel® ICH6 not resend the CFIS.

Implication: The ICH6 may continuously retry until reset by software.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

20. Intel® ICH6 AHCI PxCMD.CR Bit

Problem: If a Task File fatal error occurs during a SATA AHCI transfer, the Intel® ICH6 will not automatically clear the PxCMD.CR bit, as required by the AHCI 1.0 spec, until the AHCI driver software follows the spec-defined recovery mechanism.

Implication: None known, as AHCI compliant driver software will cause the ICH6 to clear the CR bit during error recovery.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

21. Intel® ICH6 High Definition Audio Payload Capabilities Registers

Problem: The Intel® ICH6 Intel® High Definition Audio controller does not implement the OUTSTRMPAY and INSTRMPAY registers, per Intel® HD Audio spec rev 1.0.

Implication: None - the Intel® ICH6 supports all standard audio useage models. Additionally, Intel® HD Audio codecs do not support configurations that exceed the stream BW of the Intel® ICH6. However, if software programs the audio stream to a non-standard audio format that exceeds the bandwidth capabilities of the Intel® ICH6, then the stream's DMA engine may halt.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

22. Intel® ICH6 PIO Setup FIS Error

Problem: The Intel® ICH6 SATA AHCI controller may set the ERR.T and PxIS.IFS bits when a link error (such as a CRC error) or Intel® ICH6 SATA receiver error occurs on a PIO Setup FIS, instead of setting the PxIS.INFS bit, as defined by the AHCI 1.0 specification.

Implication: A spurious interrupt is generated and the AHCI driver software will detect the error and retry.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

23. Intel® ICH6 PCI Express* Surprise Removal

Problem: After eight surprise removal or non-software initiated link down events on a PCI Express* port without a platform reset, the ICH6 may not be able to receive completions from the device on the PCI Express* link.

Implication: System may hang.

Note: Issue requires multiple PCI Express devices to be populated in the system with simultaneous upstream requests. Software must also deprogram the PCI Express port number that experienced the event before hardware is able to fully respond to the link down condition. Known software does not deprogram surprise removal port before hardware responds. This issue has only been observed in a simulation environment.

Workaround: Perform platform reset.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

24. PCI Express* Scrambling

Problem: While entering the Recovery state, the Intel® ICH6 stops scrambling two symbols before the first TS (training sequence).

Implication: When these non-scrambled symbols are received by the endpoint, the de-scrambler of the endpoint will observe two symbols of random data. The first symbol of TS1 will reset the endpoint's de-scrambler so that the endpoint should recognize the TS1 and TS2 ordered-sets being transmitted and move into the Recovery state as planned.

There is no system level impact if the endpoint is PCI Express* Specification 1.0a compliant in ignoring the random data.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

25. AHCI PxSERR:[M] Bit

Problem: The SATA AHCI controller incorrectly sets the PxSERR:[M] (Recovered Communications Error) bit if PhyRDY is established and either an internal overflow occurs or a miss-align (when SATA primitives are not detected on the correct primitive boundaries) occurs during resume from Partial/Slumber power management states.

Implication: The controller will set the PxIS:[INFS] bit which is informative only and is recoverable by software. There is no impact to system operation.

Workaround: None needed.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

26. L0s With Extended Sync

Problem: If Extended Sync and L0s are both enabled, the Intel® ICH6 may lose proper sequence of ACK messages when the link is resuming from L0s.

Implication: System may hang.

Extended Synch mode only intended for debug and test environment.

Note: This impacts both DMI and PCI Express.

Workaround: None

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

27. Intel® ICH6-M DPRSLPVR

Problem: The DPRSLPVR signal may not be properly initialized until Intel® ICH6-M's core well power rails (Vcc1_5, Vcc3_3) become stable and Intel® ICH6-M receives PCI clock.

Implication: The system may fail to boot depending on the power sequencing logic implementation and CPU VR solution used on the platform.

Workaround: An external weak pull-down resistor of 100K ohms will ensure DPRSLPVR does not float on affected systems.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

28. PATA V- Threshold

Problem: The Intel® ICH6 may violate the V_{-min} spec, per the AT Attachment with Packet Interface - 7 specification.

Implication: None known. Intel has performed extensive, targeted validation without any detected functional issues.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes.*

29. PCI Express* SKP / InitFCx Contention

Problem: During Intel® ICH6 PCI Express* initialization, if a SKP is being transmitted immediately before a InitFCx DLLP, then a partial InitFCx may be transmitted.

Implication: A slight delay (less than 100 ns) may occur during link initialization. Device may report correctable errors. InitFCx will automatically be repeated.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes.*

30. DMI L0s Latency Bit Attribute

Problem: Intel® ICH6 DMI L0s exit latency bits (RCRB+1A4h, bits 14:12) are Read/Write, not Read Only.

Implication: None known. Software should not write to this register.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes.*

31. PCI Express* Two DWord Malformed TLP

Problem: If the Intel® ICH6 receives a two DWord TLP (which is not legal per PCI Express* Spec), the ICH6 may flag the immediately following TLP as malformed.

Implication: Incorrectable error flagged and system may hang.

This issue has only been replicated using a synthetic test environment with an illegal two DWord TLP injected onto the PCI Express bus and has not been reported using commercially available hardware/software.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes.*

32. Full speed USB ISOC End of Packet

Problem: If a Full-speed USB ISOC OUT transaction occurs very late in the USB frame such that the payload cannot be contained in that frame, then a bit stuff error is created as defined in the USB 2.0 specification and flagged to both host software and device. When this occurs, and a specific data pattern is present, then the End of Packet (EOP) will not be sent. In this event, devices attached to that UHCI controller may not detect the subsequent Start of Frame (SOF) due to lack of EOP.

Implication: None, the resulting bit stuff error and device not detecting SOF are recoverable events by USB 2.0 system design.

Note: USB ISOC traffic and SOF packets are not necessarily data coherent by definition of the protocol. This issue has only been replicated in a synthetic test environment and has not been reproduced in known system configurations.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

33. AHCI SATA Interlock Switch

Problem: In AHCI enabled systems using the native interlock switch for Hot Plug, the PxIS:[DIS] bit in D31:F2 may not reflect the change in connection of a SATA device on a port via the SATA[n]GP§ pin.

Implication: The SATA controller may not properly detect a device insertion or removal event possibly resulting in loss of unsaved data (for removals), or failure to detect device presence (for insertions).

Workaround: This applies only to platforms implementing Hot Plug via an interlock switch using SATA[n]GP signals. For systems that do not have Hot Plug capability, or that do not use SATA[n]GP, no workaround is needed.

- Either completely disable all Hot Plug support by
  - — Clearing CAP:[SIS (bit-28)], PxCMD:[HPCP (bit-18)] and PxCMD:[ISP (bit-19)]

OR

- Use a GPI instead of the SATA[n]GP signal following these steps:
  - — Completely disable all Hot Plug support as indicated above and
  - — Use an SCI/SMI capable GPI(15:0) routed to the HDD interlock switch.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

34. SATA AHCI Recovery From Task File Error

Problem: During an AHCI fatal error condition, if the device signals a Task File Error (TFES), the ICH6 may not be able to recover correctly after software performs the AHCI spec-defined fatal error recovery mechanism.

Implication: SATA port will appear bus resulting in the device being inaccessible.

Note: IAA/IAMT 4.0 and later implements a reset mechanism that does not allow this issue to be exposed.

Workaround: AHCI driver should toggle the ST bit to '1' and back to '0' upon detecting TFES bit set after ST bit is cleared.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

35. ASF Decode Erratum

Problem: After receiving an ACK from a remote management console, the Intel® ICH6 ASF controller may, under certain circumstances, incorrectly decode the Remote Management and Control Protocol (RMCP) header. The incorrect decode may result in the ICH6 inappropriately sending an ACK to the management console.

Implication: None known.

The redundant ACK generated by the Intel® ICH6 will be ignored and dropped by the management console via the Intel management console software development kit available to developers.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

36. MW DMA Mode-1 Tdh Erratum

Problem: Data hold time of MW DMA Mode-1 writes may not meet ATA specification.

Implication: None known.

Workaround: Program the controller to PIO Mode-4 instead.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*

37. Reset Command Received Through SMBus During Suspend

Problem: If the Intel® ICH6 is sent a 'Hard Reset Without Cycling' command on SMBus while the system is in S3, the reset command will not be executed until the next wake event. The ASF Spec, rev 1.03, requires the ICH6 to execute the Hard Reset Without Cycling command immediately.

Implication: SMBus write commands sent after the Hard Reset Without Cycling command and before the wake event will be NAKed by the ICH6. This also applies to any SMBus wake

commands sent after a Hard Reset Without Cycling command, such that the SMBus wake command will not cause the system to wake.

Note: Any SMBus read that is accepted by the ICH6 will complete normally.

Workaround: Do not send a Hard Reset Without Cycling command while the system is in S3.

Note: Exposure to this issue can be reduced by issuing a wake command prior to issuing the Hard Reset Without Cycling command.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

38. SATA Early SYNC

Problem: After an AHCI Port Reset, the Intel® ICH6 SATA host controller may send SYNC primitives to the SATA device earlier than allowed by the SATA spec. This may cause the host to be out of sync with the device, resulting in communication not being correctly established between the host and the device.

Implication: System implication may vary depending on AHCI driver and/or SATA device.

- If software driver issues a command to the device after the problem has occurred, the command may not be sent to the device correctly. The AHCI spec allows for the driver to time-out and perform another Port Reset as error recovery.
- If the host and device are able to re-establish the link and get in-sync through software error recovery actions, no end-user implications are visible.

Workaround: Software must program the port to be reset into AHCI 'Offline mode' by writing 4h to AHCI PxSCTL.DET register field (ABAR + 12Ch + (x*80h)) before doing a 'Port Reset' to the port; where x = any port number from 0 to 3.

Note: Workaround implemented in Intel® Matrix Storage Manager driver version 6.0.0.1022 and later.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes.*

39. PCI Express* Root Port Power State Value

Problem: The Intel® ICH6 PCI Express* root ports support the D3 and D0 states, but also accept writes of values corresponding to the D2 and D1 states in the Power State bit field of the Power Management Control and Status registers (D28:F0/F1/F2/F3:A4h). The Intel® ICH6 PCI Express root port PCI Power Management Capabilities Registers (D28:F0/F1/F2/F3:A2h) do not claim support of D2 and D1 power states.

Implication: No functional implications known. Writes of values corresponding to the D2 and D1 states (i.e., 10b or 01b) do not cause behavioral changes within the ICH6, but the value is displayed in the Power State bit field.

Workaround: Software should not write unsupported power state values (i.e., 10b or 01b) to the Power State bit field of the Power Management Control and Status register

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*

40. PCI Express* Upstream Link Base Address Register Bit 0

Problem: The ICH6 PCI Express* root ports' Upstream Link Base Address (ULBA) Register (D28:F0/F1/F2/F3:198h) bit 0 mirrors the value of bit 0 in the ICH6 RCBA register (D31:F0:F0h). During normal system operation, bit 0 of the RCBA register is set to 1. This results in bit 0 of the ULBA also being set to 1. The PCI Express specification, rev 1.0a, requires that bit 0 of the ULBA be 0.

Implication: No functional implications known.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*

41. High Speed (HS) USB2.0 D+ and D- Maximum Driven Signal Level

Problem: During Start-of-Packet (SOP)/End-of-Packet (EOP), the Intel® ICH6 may drive D+ and D- lines to a level greater than USB 2.0 spec +/-200mV max.

Implication: May cause High Speed (HS) USB 2.0 devices to be unrecognized by OS or may not be readable/writable if the following two conditions are met:

- The receiver is pseudo differential design
- The receiver is not able to ignore SE1 (single-ended) state

Note: Intel has only observed this issue with a motherboard down HS USB 2.0 device using pseudo differential design. This issue will not affect HS USB 2.0 devices with complementary differential design or Low Speed (LS) and Full Speed (FS) devices

Workaround: None.

Status: No Fix.For steppings affected, see the *Summary Tables of Changes.*§

42. Intel® I/O Controller Hub 6 (ICH6) Family PCI Express Function Disable

Problem: Intel® ICH6 Family PCI Express [1:6] Disable bit in Function Disable Register may not put the PCI Express port into a link down state if a PCI Express device is attached.

Implication: Intel® ICH6, ICH6R, and ICH6-M:

PCI Express port [1:6] with a PCI Express device attached may remain in L0 state.

Workaround: A BIOS code change update has been identified.

Status: No Fix. For steppings affected, see the *Summary Table of Changes.*

43. Incorrect IRQ(x) Vector Returned for 8259 Interrupts With RAEOI Enabled

Problem: If multiple interrupts are active prior to an interrupt acknowledge cycle with Rotating Automatic End of Interrupt (RAEOI) mode of operation enabled for 8259 interrupts (0-7), an incorrect IRQ(x) vector may be returned to the CPU.

Implication: Implications of an incorrect IRQ(x) vector being returned to the CPU are SW implementation dependent.

Note: This issue has only been observed in a synthetic test environment.

Workaround: None.

Status: No Plan to Fix.

Specification Changes

1. t200 change

The minimum value of t200 in Table 22-21 is changed to 18ms as indicated below:

Sym	Parameter	Min	Max	Units	Fig	Notes
t200	VccRTC active to RTCRST# inactive	18		ms	22-18 22-19	

2. RSMRST# Timing Addition

The following timing and note are added to Table 22-22. The new timing reflects the requirements that are already part of the platform design.

Sym	Parameter	Min	Max	Units	Notes	Fig
t311	RSMRST# rising edge transition from 20% to 80%		50	us		
t312	RSMRST# falling edge transition				15	

NOTES:

15. RSMRST# falling edge must transition to 0.8V or less before VccSus3_3 drops to 2.1V

3. Removing Support for USB Wake from S5

Support for USB wake from S5 is removed from Datasheet as indicated below.

a. Update Intel® ICH6 Features page of the Datasheet as follows:

USB 2.0

- ..... Includes four UHCI Host Controllers, supporting eight external ports
- Includes one EHCI Host Controllers that support all eight ports
- Includes one USB 2.0 High-speed Debug Ports
- Supports wake-up from sleeping states S1–S4
- Supports legacy Keyboard/Mouse software

b. Update Table 5-31 as follows:

Table 5-30. Causes of Wake Events

Table 1.

Cause	States Can Wake From	How Enabled
Classic USB	S1–S4	Set USB1_EN, USB 2_EN, USB3_EN, and USB4_EN bits in GPE0_EN register

4. ROAEI options removal for OCW2

Remove bit setting “000” and “100” for Operational Control Word 2 Register bits [7:5] in section 10.4.8.

10.4.8 OCW2—Operational Control Word 2 Register (LPC I/F-D31:F0)

Offset Address:	Master Controller – 020h	Attribute:	WO
	Slave Controller – 0A0h	Size:	8 bits
Default Value:	Bit[4:0]=undefined, Bit[7:5]=001		

Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Bit	Description
7:5	**Rotate and EOI Codes** (R, SL, EOI) —WO. These three bits control the Rotate and End of Interrupt modes and combinations of the two. 000 = ~~Rotate in Auto EOI Mode (Clear)~~ Reserved 001 = Non-specific EOI command 010 = No Operation 011 = *Specific EOI Command 100 = ~~Rotate in Auto EOI Mode (Set)~~ Reserved 101 = Rotate on Non-Specific EOI Command 110 = *Set Priority Command 111 = *Rotate on Specific EOI Command *L0 – L2 Are Used

Specification Clarifications

1. t216 Clarification

Note 10 is added to parameter t216 (Table 22-21 (Power Sequencing and Reset Signal Timings)

Note 10: Vcc3_3 should be used for DPRSLPVR, STP_PCI#, STP_CPU# and V_CPU_IO should be used for STPCLK#, CPUSLP#, DPSLP#, DPRSTP#.

2. C2 Support

C2 support is provided for only in the ICH6-M. The title of section 10.8.3.6 is changed to “LV2 - Level 2 Register (Mobile Only)”

The first two rows of Table 5-25 State Transition Rules for Intel® ICH6 are changed as indicated below:

Present State	Transition Trigger	Next State
G0/S0/C0	• Processor halt instruction • Level 2 Read (Mobile Only) • Level 3 Read (Mobile Only) • Level 4 Read (Mobile Only) • SLP_EN bit set • Power Button Override • Mechanical Off/Power Failure	• G0/S0/C1 • G0/S0/C2 • G0/S0/C2, G0/S0/C3 or G0/S0/C4 - depending on C4onC3_EN bit (D31:F0;Offset A0h:bit-7 and BM_STS_ZERO_EN bit (D31:F0;Offset A9h:bit-2) (Mobile Only) • G1/Sx or G3/S5 state • G2/S5 • G3
G0/S0/C1	• Any Enabled Break Event • STPCLK# goes active • Power Button Override • Power Failure	• G0/S0/C0 • G0/S0 / C2 (Mobile Only) • G2/S5 • G3

3. LPC Cycle Clarification

The following changes are made to Table 5-4 LPC Cycle Types Supported in section 5.5.1.1:

- “See Note 1” is removed from the comment column for both I/O Read and I/O Write cycle types.§
- “See Note 1 is added to the comment column for both Memory Read and Memory Write cycle types.
- Note 1 is replaced with the following text:

“For memory cycles below 16 MB that do not target enabled firmware hub ranges, the ICH6 performs standard LPC memory cycles. It only attempts 8-bit transfers. For larger transfers, ICH6 performs multiple 8-bit transfers. If the cycle is not claimed by any

peripherals, it is subsequently aborted, and the Intel® ICH6 returns a value of all 1s to the processor. This is done to maintain compatibility with ISA memory cycles where pull-up resistors would keep the bus high if no device responds."

1. GPIO25 Pull-up

Table 3-1 incorrectly applies Note 11 to the GPIO[25] signal. This reference to Note 11 is removed for GPIO[25].

2. HPET TIMERn_32MODE_CNF

The description of TIMERn_32MODE_CNF (section 20.1.5) is replaced as follows:

Bit	Description
8	Timer n 32-bit Mode (TIMERn_32MODE_CNF) - R/W or RO. Software can set this bit to force a 64-bit timer to behave as a 32-bit timer. This is typically needed if software is not willing to halt the main counter to read or write a particular timer, and the software is not capable of atomic 64-bit operations to the timer. This bit is only relevant if the timer is operating in 64-bit mode in which case that timer can be forced to 32-bit mode by setting this bit. When Timer 0 is switched to 32-bit mode, the upper 32 bits are loaded with all 0's which will remain when the timer is switched back to 64-bit mode. If the timer is not in 64-bit mode, then this bit will always be read as 0 and writes will have no effect. Timer 0: Read/Write (default 0). 0 = 64-bit, 1=32-bit. Timers 1/2: Hardwired to 0. Writes have no effect since these timers are 32-bit only.

3. PCI Clock

The Intel® ICH6 PCI was designed to meet the requirements for the PCI 2.3 specification. As a result, Table 22-9 is updated to match that specification using the below table.

Sym	Parameter	Min.	Max	Unit	Figure	Notes
PCI Clock (PCICLK)						
t1	Period	30	33.3	ns	22-1	
t2	High Time	11		ns	22-1	
t3	Low Time	11		ns	22-1	
t4	Rise Time	1	4	V/ns	22-1	
t5	Fall Time	1	4	V/ns	22-1	

4. Reserved Clarification

The following text is added to the bottom of Chapter 6 (before section 6.1):

"All bit(s) or bit-fields listed as Reserved must be correctly dealt with by software. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit locations are preserved. Any ICH6 configuration register or I/O or memory mapped location not explicitly indicated in this document must be considered reserved."

5. PATA Secondary Command/Control BAR

The following sentence is added to the descriptions of the Base Address field for both SCMD_BAR and SCNL_BAR (sections 11.1.13 and 11.1.14):

"If register is programmed, the programmed value must not be less than 100h."

6. F0h Read Behavior Clarifications

The ICH6's behavior when reads are made to I/O address F0h is clarified below.

Table 6-2 is updated as follows:

I/O Address	Read Target	Write Target	Internal Unit
F0h	FERR# / IGNNE# / Interrupt Controller	FERR# / IGNNE# / Interrupt Controller	Processor I/F

Note 1 from table 6-2 is removed.

Section 10.7.4 is replaced as follows:

10.7.4 COPROC_ERR—Coprocessor Error Register (LPC I/F—D31:F0)

I/O Address:	F0h	Attribute:	R/W
Default Value:	00h	Size:	8-bits
Lockable:	No	Power Well:	Core

Bits	Description
7:0	**Coprocessor Error (COPROC_ERR)** — R/W. Any value written to this register will cause IGNNE# to go active, if FERR# had generated an internal IRQ13. For FERR# to generate an internal IRQ13, the COPROC_ERR_EN bit (Device 31:Function 0, Offset D0, Bit 13) must be 1. Reads to this register always return 00h.

7. Indeterminate State Before Power Stable

The following notes are added to the table notes of Tables 3-3 (Power Plane and States for Output and I/O Signals for Desktop Configurations), 3-4 (Power Plane and States for Output and I/O Signals for Mobile Configurations), 3-5 (Power Plane for Input Signals for Desktop Configurations) and 3-6 (Power Plane for Input Signals for Mobile Configurations):

Intel® ICH6 suspend well signal states are indeterminate and undefined and may glitch prior to RSMRST# deassertion. This note does not apply to LAN_RST#, SLP_S3#, SLP_S4#, and SLP_S5#. These signals are determinate and defined prior to RSMRST# deassertion.

Intel® ICH6 core well signal states are indeterminate and undefined and may glitch prior to PWROK assertion. This note does not apply to FERR# and THRMTRIP#. These signals are determinate and defined prior to PWROK assertion.

8. LPC SERR Generation Behavior Clarification

The following is added as section 5.5.2:

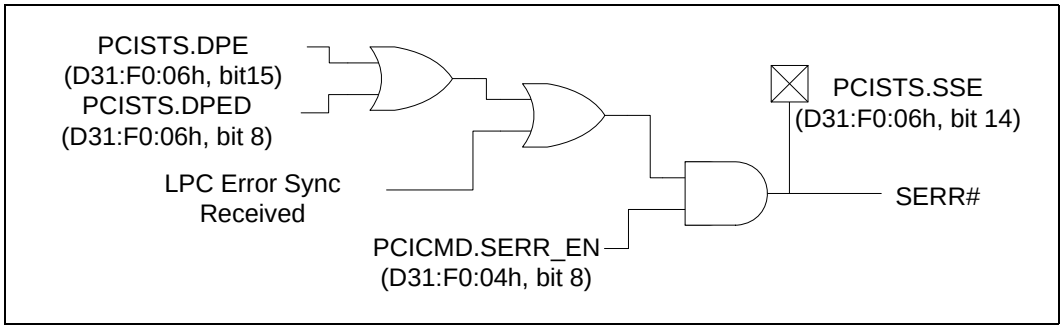
5.5.2 SERR# Generation

Several internal and external sources of the LPC Bridge can cause SERR#, as described below.

The first class of errors is parity errors related to the backbone. The LPC Bridge captures generic data parity errors (errors it finds on the backbone) as well as errors returned on the backbone cycles where the bridge was the master and parity error response is enabled. If either of these two conditions is met, and with SERR# enable (PCICMD.SERR_EN) set, SERR# will be captured.

Additionally, if the LPC Bridge receives an error SYNC on LPC bus, an SERR# will also be generated.

Figure 1. LPC Bridge SERR# Generation



9. PCI Downstream Device Disable Clarification

In section 5.1.6, the following note is added:

Note: All downstream devices should be disabled before reconfiguring the PCI Bridge. Failure to do so may cause undefined results.

10. t232 Clarification

Note 14 has been added to table 22-22 Power Management Timings to describe the relationship between AFTERG3_EN and timing t232 as indicated below.

t231 t232	RSMRST# inactive to SUSCLK running, SLP_S5# inactive		110	ms	1, 14	22-20 22-21

Note: 14. If the AFTERG3_EN bit (GEN_PMCON_3 Configuration Register Bit 1) is set to a 1, SLP_S5# will not be de-asserted until a wake event is detected. If the AFTERG3_EN bit is set to 0, SLP_S5# will deassert within the specification listed in the table.

11. SMBus Slave Write Clarification

The following Note is added to Section 5.21.7.1.

Note: If the Intel® ICH6 is sent a 'Hard Reset Without Cycling' command on SMBus while the system is in S4 or S5, the reset command will not be executed until the next wake event. SMBus write commands sent after the Hard Reset Without Cycling command and before the wake event will be NAKed by the Intel® ICH6. This also applies to any SMBus wake commands sent after a Hard Reset Without Cycling command, such that the SMBus wake command will not cause the system to wake. Any SMBus read that is accepted by the Intel® ICH6 will complete normally.

§

Document Changes

1. PCI Device Revision ID

PCI Revision ID Register values (PCI Offset 08h) for all Intel® ICH6 functions are shown below. This information is not found in the datasheet. This is the standard reference document.

Device Function	Description	Intel® ICH6 Dev ID	ICH6 B1 Rev ID	ICH6 B2 Rev ID	ICH6 C0 Rev ID	Comments
D31, F0	LPC	2640h	03h	04h	05h	ICH6/ICH6R
		2641h	03h	04h	N/A	ICH6-M
D31, F1	IDE	266Fh	03h	04h	05h	
D31, F2 SATA		2651h	03h	04h	05h	ICH6
		2652h	03h	04h	05h	ICH6R
		2653h	03h	04h	N/A	ICH6-M
D31, F3	SMBus	266Ah	03h	04h	05h	
D30, F0	DMI to PCI Bridge	244Eh	D3h	D4h	D5h	
		2448h	D3h	D4h	N/A	ICH6-M
D30, F2	AC '97 Audio	266Eh	03h	04h	05h	
D30, F3	AC '97 Modem	266Dh	03h	04h	05h	
D29, F0	USB UHC #1	2658h	03h	04h	05h	
D29, F1	USB UHC #2	2659h	03h	04h	05h	
D29, F2	USB UHC #3	265Ah	03h	04h	05h	
D29, F3	USB UHC #4	265Bh	03h	04h	05h	
D29, F7	USB EHCI	265Ch	03h	04h	05h	
D28:F0	PCI Express* Port 1	2660h	03h	04h	05h	
D28:F1	PCI Express Port 2	2662h	03h	04h	05h	
D28:F2	PCI Express Port 3	2664h	03h	04h	05h	
D28:F3	PCI Express Port 4	2666h	03h	04h	05h	
D27:F0	Intel® High Definition Audio	2668h	03h	04h	05h	
D8:F0	LAN	1065h[1]	03h	04h	05h	

Notes:

1. Loaded from EEPROM. If EEPROM contains either 0000h or FFFFh in the device ID location, then 266Ch is used. Refer to the ICH6 EEPROM Map and Programming Guide for LAN Device IDs.
2. VccRTC at 3.0 V while the system is in G3 state at room temperature and only the G3 state for this power well is shown to provide an estimate of battery life.

2. CAP.SALP

Section 12.3.1.1 (CAP - Host Capabilities Register) incorrectly identifies the attribute for its SALP (bit-26) bit. It is changed to R/WO.

3. Memory Address Range Addition

Section 6.4, the following row is added to Table 6-4:

Memory Range	Target	Dependency/Comments
FED4 0000h - FED4 0FFFh	TPM on LPC	

4. D30:F0 PSTS Correction

In section 9.1.4, D30:F0;PSTS, the description for bit-0 is change to Reserved.

5. IDE MSE Bit

In section 11.1.3 (PCI Command Register) the description for bit-1 is incorrect and is changed to the following:

Bit	Description
1	**Memory Space Enable (MSE)** - RO

6. PxCMD.ST Bit Description Correction

The description for the Start bit in PxCMD (section 12.3.2.7) incorrectly refers to section 12.2.1 of the Serial ATA AHCI Specification. This is corrected to section 10.3.1.

7. PCI Functional Description Correction

The Memory Reads and Writes subsection of the PCI functional description (section 5.1.2.1) has an incorrect register reference. The second sentence of the paragraph is removed.

8. VRMPWRGD Timing Diagram Corrections

“VRMPWRGD” is deleted from Figures 22-23 and 22-25. In Figures 22-24 and 22-26 VRMPWRGD is changed to PWROK.

9. THRMTRIP# Timing Correction

The THRMTRIP# active to SLP_S3#, SLP_S4#, SLP_S5# active time (t310MAX) is corrected from 2 PCICLK periods to 3 PCICLK periods.

10. LSTS Note Correction

The note in LSTS.NLW (section 23.1.29) is corrected to the following:

Note: 000001b = x1 link width, 0000100 = x4 link width (Enterprise applications only)

11. Interrupt Pin Register Reserved Bits Correction

For sections 7.1.42 thru 7.1.45, interrupt pin register values of 8h-Fh are Reserved in addition to 5h-7h (that is, the reserved interrupt pin values are 5h-Fh).

12. USB Port Number Documentation Corrections

In section 5.20.10.1.3, the description of bits 20:23 of the EHCI Host Controller Structural Parameters register indicates an incorrect value for these bits. The sentence is changed to:

"This 4-bit field represents the numeric value assigned to the debug port (i.e., 0001 = port 0)."

The PWAKE_CAP.Port Wake Up Capability Mask (section 14.1.25) bit description is changed to the following:

Bit	Description
8:1	**Port Wake Up Capability Mask** — R/W. Bit positions 1 through 8 correspond to a physical port implemented on this host controller. For example, bit position 1 corresponds to port 0, bit position 2 corresponds to port 1, etc.

13. LPC Cycle Change

LPC Memory cycles are not supported by the ICH6. Section 5.5.1.1 and 5.5.1.3 are changed to:

0.0.0.1 LPC Cycle Types

The Intel® ICH6 implements the following cycle types as described in Table 5-4.

Cycle Type	Comment
I/O Read	1 byte only. Intel® ICH6 breaks up 16- and 32-bit processor cycles into multiple 8-bit transfers.
I/O Write	1 byte only. ICH6 breaks up 16- and 32-bit processor cycles into multiple 8-bit transfers.
DMA Read	Can be 1, or 2 bytes
DMA Write	Can be 1, or 2 bytes
Bus Master Read	Can be 1, 2, or 4 bytes. (See Note 1 below)
Bus Master Write	Can be 1, 2, or 4 bytes. (See Note 1 below)

Notes:

1. Bus Master Read or Write cycles must be naturally aligned. For example, a 1-byte transfer can be to any address. However, the 2-byte transfer must be word-aligned (i.e., with an address where A0=0). A dword transfer must be dword-aligned (i.e., with an address where A1 and A0 are both 0)

0.0.0.2 Cycle Type / Direction (CYCTYPE + DIR)

The Intel® ICH6 always drives bit 0 of this field to 0. Peripherals running bus master cycles must also drive bit 0 to 0. Table 5-6 shows the valid bit encodings.

Bits[3:2]	Bit1	Definition
00	0	I/O Read
00	1	I/O Write
10	0	DMA Read
10	1	DMA Write
11	x	Reserved. If a peripheral performing a bus master cycle generates this value, the Intel® ICH6 aborts the cycle.

All other encodings are RESERVED.

14. BIOSWE Bit Clarification

In Section 10.1.26, D31:F0 BIOS_CTRL register, the description of bit 0 (BIOWE) is clarified with a note as indicated below:

Bits	Description
0	**BIOS Write Enable (BIOSWE)** — R/W. 0 = Only read cycles result in Firmware Hub I/F cycles. 1 = Access to the BIOS space is enabled for both read and write cycles. When this bit is written from a 0 to a 1 and BIOS Lock Enable (BLE) is also set, an SMI# is generated. This ensures that only SMI code can update BIOS Note: Writes to the Firmware Hub's Feature Space are not blocked when the BIOSWE is cleared in order to allow access to registers. The Feature Space is the second range that is located 4MB below the BIOS range for each Firmware Hub.

15. APIC Enable (AEN) Bit Clarification

The following change applies to Section 7.1.51 to clarify the description of APIC Enable bit.

0	**APIC Enable (AEN)** — R/W 0 = The internal IOxAPIC is disabled. 1 = Enables the internal IOxAPIC and its address decode. **Note**: SW should read this register after modifying APIC Enable bit, prior to access to the IOxAPIC address range.

16. Reset Control Register (CF9h) Clarification

The following clarification applies to Section 10.7.5.

1	**System Reset (SYS_RST)** — R/W. This bit is used to determine a hard or soft reset to the processor. 0 = When RST_CPU bit goes from 0 to 1, the ICH6 performs a soft reset by activating INIT# for 16 PCI clocks. 1 = When RST_CPU bit goes from 0 to 1, the ICH6 performs a hard reset by activating PLTRST# and SUS_STAT# active for about 5-6 milliseconds. In this case, SLP_S#3, SLP_S4#, and SLP_S5# state (assertion or de-assertion) depends on FULL_RST bit setting. The ICH6 main power well is reset when this bit is 1. It also resets the resume well bits (except for those noted throughout the datasheet).

17. Correct section 5.14.7.5 Sx-G3-Sx, Handling Power Failures regarding possible wake events following a power failure

Correct section 5.14.7.5 Sx-G3-Sx, Handling Power Failures in the Datasheet.

Section 5.14.7.5 Sx-G3-Sx, Handling Power Failures§

Depending on when the power failure occurs and how the system is designed, different transitions could occur due to a power failure.

The AFTER_G3 bit provides the ability to program whether or not the system should boot once power returns after a power loss event. If the policy is to not boot, the system remains in an S5 state (unless previously in S4). ~~There are only three possible~~

~~events that will wake the system after a power failure.~~ The following wake events can wake the system following a power loss by either RSMRST# going low and enabling by default, the enable bits reside in the RCT well or the wake event is always enabled.

1. **PWRBTN#:** PWRBTN# is always enabled as a wake event. When RSMRST# is low (G3 state), the PWRBTN_STS bit is reset. When the ICH6 exits G3 after power returns (RSMRST# goes high), the PWRBTN# signal is already high (because VCC-standby goes high before RSMRST# goes high) and the PWRBTN_STS bit is 0.

2. **RI#:** RI# does not have an internal pull-up. Therefore, if this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit is set and the system interprets that as a wake event.

3. **RTC Alarm:** The RTC_EN bit is in the RTC well and is preserved after a power loss. Like PWRBTN_STS the RTC_STS bit is cleared when RSMRST# goes low.

4. **PME_B0:** PME_B0_EN is in the RTC Well and is preserved after a power loss. The PME_B0_STS bit is also cleared when RSMRST# goes low.

5. **PME: PME_EN:** is in the RTC Well and is preserved after a power loss. The PME_STS bit is also cleared when RSMRST# goes low.

6. **Host SMBUS:** SMBALERT# or Slave Wake message is always enabled as Wake Event

The ICH6 monitors both PWROK and RSMRST# to detect for power failures. If PWROK goes low, the PWROK_FLR bit is set. If RSMRST# goes low, PWR_FLR is set.

~~***Note:*** Although PME_EN is in the RTC well, this signal cannot wake the system after a power loss. PME_EN is cleared by RTCRST#, and PME_STS is cleared by RSMRST#.~~

18. Correct A20M# Signal Description

Correct A20M# signal description in Table 2-12: Processor Interface Signals in the ICH6 Datasheet.

Name	Type	Description
A20M#	O	**Mask A20:** A20M# will go ~~active~~ inactive based on either setting the appropriate bit in the Port 92h register, or based on the A20GATE input being active.