Design For EMI

Application Note AP-589

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1.0 Introduction

As microprocessor speeds increase, reducing Electromagnetic Interference (EMI) becomes an essential part of design considerations. This application note provides guidelines to aid the PC desktop system and motherboard designer with low cost solutions on reducing EMI.

The document focuses on the efforts made by Intel to prevent systems utilizing Intel processors and components from interfering with other electronic products.

There are generally two methods by which interference is measured:

- below 30 MHz EMI RF, noise is measured as *conducted* emissions
- above 30 MHz RF, noise is measured as *radiated* emissions.

As all of the frequencies generated for and by the P6 class of microprocessor (e.g., Pentium® III processor, Pentium® II processor, Intel® Celeron™ processor, and Pentium® Pro processor) exceed 66 MHz, this document concerns itself only with radiated emissions above 66 MHz.

Topics discussed are:

- Board/System EMI Design Considerations (e.g., spread spectrum clocking, differential clocking, heatsink effects, SDRAM clock buffers, and SC242 EMI pins)
- Board EMI Design Considerations (e.g., grounding, component placement, trace routing, power decoupling, and minimizing board conducted emissions)
- System EMI Design Recommendations (e.g., chassis construction and cabling)

Note: This application note is not intended to be a guaranteed, fool-proof method on passing FCC regulations.

1.1 Terminology

- **Electromagnetic Interference (EMI)**. Electromagnetic radiation from an electrical source interrupting the normal operation of an electronic device.
- **Electromagnetic Compatibility (EMC)**. The successful operation of electronic equipment in its intended electromagnetic environment. Encompasses energy generated within or external to the system.
- **Emissions**. Energy emanating from an external source that may pose a threat to other equipment. This energy may be conducted or radiated.
- **SC242**. The 242-contact slot connector that the Pentium® III processor, Pentium® II processor, and Intel® Celeron™ processor (S.E.P. Package) plugs into.

1.2 References

- *ABC's of EMI and RFI*, Daryl Gerke and Bill Kimmel, Kimmel Gerke Associates, Ltd., St. Paul, June 1994.
- EDN's *Designer's Guide to Electromagnetic Compatibility*, Daryl Gerke and Bill Kimmel, Cahners Publishing Co., January 1994.
- *An Introduction to Electromagnetic Compatibility*, Clayton R. Paul, John Wiley and Sons, New York, 1992.

1.3 Brief EMI Theory

The simplest component of EMI is an electromagnetic wave, which consists of both electric (E-field) and magnetic (H-field) waves running perpendicular to each other. Reducing either the E-field or H-field can lower emissions and is the basis of suppression techniques.

Another key source of emissions is current flow. As processor speeds increase, the processor's current requirements increase. Current flowing through a loop generates a magnetic field, which is proportional to the area of the loop. Loop area is defined as trace length times the distance to the ground plane. As signals change logic states, an electric field is generated from the voltage transition. Thus, radiation occurs as a result of this current loop. The following equation shows the relationship of current, its loop area, and the frequency to EMI:

$$EMI\ (^{V}/_{m}) = kIAf^{2}$$

Where:

k	=	constant of proportionality
I	=	current (A)
A	=	loop area (m^2)
f	=	frequency (MHz)

Since the distance to the ground plane is usually fixed due to board stackup requirements, minimizing trace length on the board layout is key to decreasing emissions.

1.4 EMI Regulations and Certifications

Personal Computer Original Equipment Manufacturers (PC OEMs) ensure Electromagnetic Compatibility (EMC) by meeting EMI regulatory requirements. PC OEMs must ensure that their computer systems do not exceed the emission limit standards set by applicable regulatory agencies. The two standards that this document references are:

- United States Federal Communication Commission's (FCC) Part 15
- International Electrotechnical Commission's International Special Committee on Radio Interference (CISPR) Publication 22 class B limits.

Table 1 and Table 2 list the frequency and associated radiation limits. The FCC requires any PC OEM who sells an "on-the-shelf" motherboard to pass an open-chassis requirement. This regulation ensures that system boards, which are key contributors to EMI, have reasonable emission levels. The open-chassis requirement relaxes the FCC Part 15 class B limits by 6 dB, but requires that the test be administered with the chassis cover off.

Table 1. FCC Part 15 Class B Limits

Frequency (MHz)	Radiation (dB uV/m)
30 – 88	40.0
88 – 216	43.5
216 – 960	46.0
Above 960	54.0

NOTES:
1. Quasi-peak measured at 3 meters.
2. The upper test frequency is determined by the highest clock frequency utilized in the product. Clocks below 108 MHz require testing to 1 GHz. Clocks from 108 MHz to 500 MHz require testing to 2 GHz. Clocks from 500 MHz to 1 GHz require testing to 5 GHz. Clocks above 1 GHz require testing to the 5^{th} harmonic or 40 GHz, whichever is lower.

Table 2. CISPR 22 Class B Limits

Frequency (MHz)	Radiation (dB uV/m)
30 – 230 MHz	30.0
230 – 1000 MHz	37.0

NOTES:
1. Quasi-peak measured at 10 meters.
2. Limits above 1 GHz are under consideration.

2.0 Board/System EMI Design Considerations

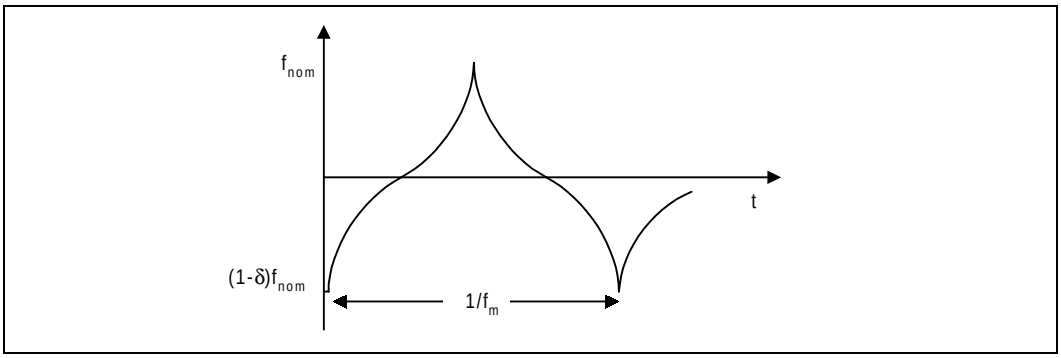
The following sections discuss guidelines which may be applied to minimize EMI.

2.1 Spread Spectrum Clocking

Spread Spectrum Clocking (SSC) has been demonstrated to reduce peak radiation by approximately 8 dB. The spread spectrum clock generator reduces radiated emissions by spreading the emissions over a wider frequency band (Figure 2). This band can be broadened, with subsequent reductions in the measured radiation levels, by slowly frequency modulating the processor clock over a few hundred kHz. Thus, instead of maintaining a constant system frequency, SSC modulates the clock frequency/period along a predetermined path (i.e., modulation profile) with a predetermined modulation frequency. The modulation frequency is usually selected to be larger than 30 KHz (above the audio band) while small enough not to upset the PC system's timings.

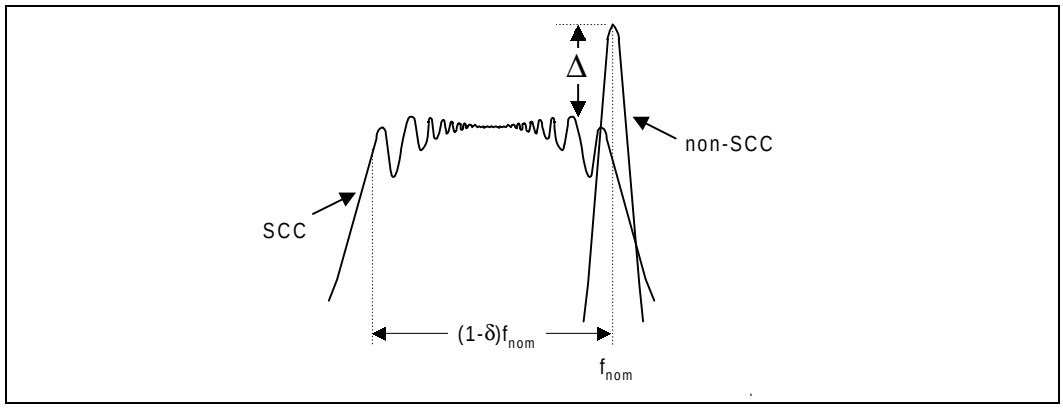
To conserve the minimum period requirement for bus timing, the SSC clock is modulated between f_{nom} and $(1-\delta)f_{nom}$ where f_{nom} is the nominal frequency for a constant-frequency clock (Figure 1); δ specifies the total amount of spreading as a relative percentage of f_{nom}.

Figure 1. Typical Modulation Profile for SSC Clocks



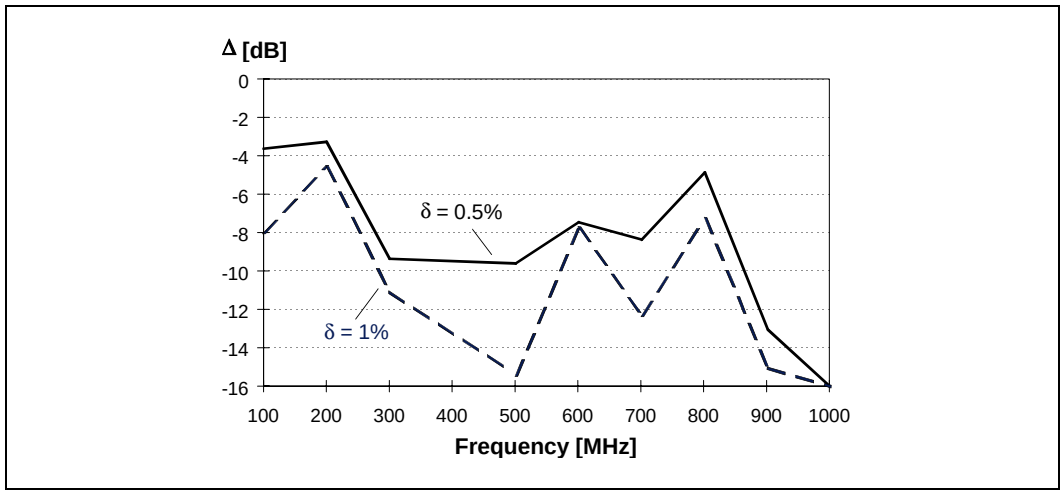
The frequency modulation in the time-domain results in a frequency-domain energy redistribution of the constant-frequency clock harmonics. The shape of the spectral energy distribution of the SSC is determined by the time-domain modulation profile, while the energy distribution width is determined be the modulation amount (δ). The two combined determine the amount of EMI reduction (Δ).

Figure 2. Spread Spectrum Clocking (SSC)



Radiated emissions are typically confined in a narrow band centered around clock frequency harmonics. By uniformly distributing the radiation over a band of a few MHz, regulatory measurement levels (in a 120 kHz bandwidth at frequencies below 1 GHz and in a 1 MHz bandwidth at frequencies above 1 GHz) will be reduced. Figure 3 shows that as the modulation amount (δ) increases, so does the amount of EMI reduction (Δ).

Figure 3. Impact of a Spread Spectrum Clock



2.2 Differential Clocking

Experiments have shown that a differential clocking scheme can potentially reduce emissions in the order of 6 dB. Differential clocking requires that the clock generator supply both clock and clock bar traces, where the board designer would route the two traces together in parallel. A clock bar has equal and opposite current with the primary clock and is also 180° out of phase.

The EMI reduction due to differential clocking is caused by H-field cancellation (Figure 4). Since H-fields travel with current flow according to the right-hand rule, two currents flowing in opposite directions and 180° out of phase will have their H-fields cancelled. Reducing H-fields results in lower emissions.

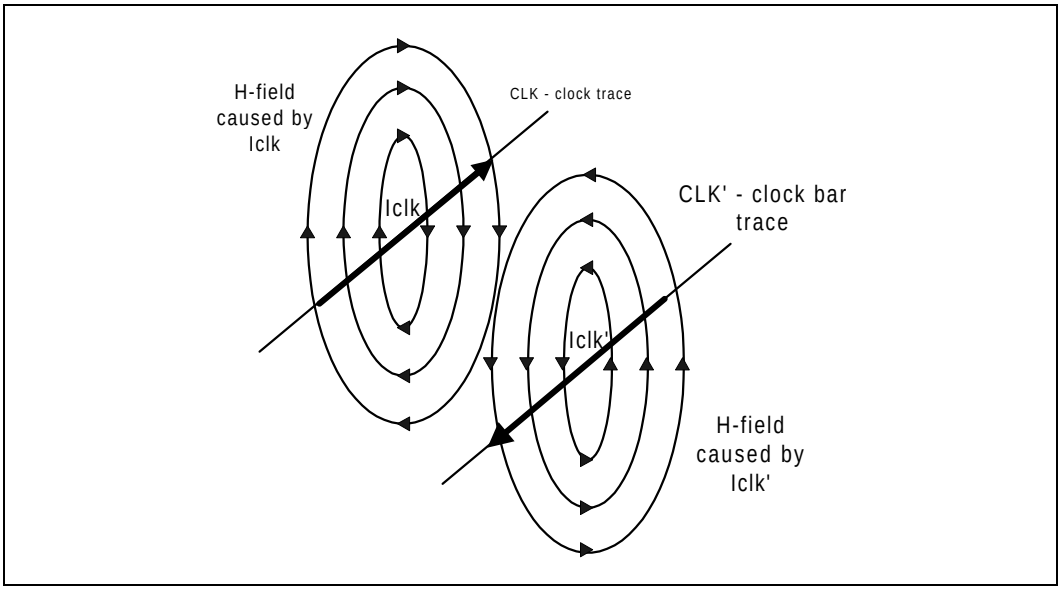
Differential clocking can also reduce the amount of noise coupled to I/O traces, which are EMI-generating paths because they leave the system. A single-ended clock's return path is usually a reference plane, which is shared by other signals/traces. When noise is created on a single-ended clock, the noise will appear on the reference plane and may be coupled to I/O traces. A differential clock's return path is the clock bar signal/trace, which is more isolated than the reference plane and reduces I/O trace coupling.

For best results,

- The trace lengths and the 180° phase difference between the two clocks needs to be closely matched.
- The real and parasitic terminations of each differential pair line should be the same.

The spacing between the two traces should be as small as possible. Placing ground traces on the outside of the differential pair may further reduce emissions. Intermediate vias to ground may be needed to reduce the opportunity for re-radiation from the ground traces themselves. Distance between vias is related to the clock trace's frequency. Since this is specific to the type of clock, see specific design guidelines for implementation.

Figure 4. H-Field Cancellation



2.3 Heatsink Effects

As the processor's core frequency increases, so does the opportunity for its heatsink to act as a radiating antenna. Studies have shown that its size, geometry, and orientation have an effect on the amount of emissions generated. While Intel cannot recommend which heatsink to use and what orientation is best, as it is system dependent, the designer should consider heatsink effects and determine the best solution for their particular system.

Experiments have also suggested that grounding the processor's heatsink may reduce emissions. Creating a ground path from the heatsink to either the motherboard or chassis ground will return some stray current to its source and reduce EMI. While this may have both positive and negative effects on various frequencies, the decision is again left to the system designer on the implementation and whether it has a positive effect on passing regulations.

Other items of note are the thermal interface material (between the processor and heatsink) and the distance of the heatsink to the processor core. Experiments have shown that the distance of the processor heatsink to its core can greatly have an effect on emissions. Since the heatsink acts as an antenna, the amount of processor noise coupled to the heatsink is relative to the distance between the two. A thermal interface material can reduce EMI by helping to prevent the heatsink from getting too close to the processor.

2.4 SDRAM Clock Buffer

Intel has observed an increase in emission levels with system boards that use an individual 100 MHz SDRAM clock buffer. The affected frequencies are the 100 MHz harmonics (n x 100 MHz, where n is the integral harmonic number).

Experiments have shown that an integrated clock generator (one that integrates the 100 MHz SDRAM clock buffer) has lower emissions than having a separate clock generator and clock buffer. Also, isolating the clock buffer through dedicated power and ground planes also reduces emissions. For more information on clock buffer isolation, a document is available on Intel's developer website at:

http://developer.intel.com/ial/sdt/

2.5 SC242 EMI Pins

There are five EMI pins on SC242-compatible processors which connect to the processor substrate's V_{SS} (ground) plane. This allows the designer to determine whether grounding or disconnecting these pins have any effect on emission levels. The recommendation is to ground the EMI pins through 0 Ω resistors. A designer can, therefore, conduct EMI testing with the resistors stuffed (grounding the pins) or unstuffed (leaving the pins disconnected). The approach with the better results can be implemented without a motherboard layout change.

3.0 Board EMI Design Recommendations

3.1 Grounding Considerations

Good grounding requires taking precautions to minimize inductance levels in the interconnection. To minimize the radiation levels, keep the ground return paths short, signal loop areas small, and provide bypass at the power inputs. For the high-speed signal returns, the DC power and ground planes may be considered equivalent. This is due to the capacitive coupling between the two planes.

The following guidelines may help to reduce circuit inductance on the motherboard:

- Locate grounds to minimize the loop area between a signal path and its return path.
- Avoid splitting ground and power planes or creating cutouts and voids.
- To reduce ground noise coupling, separate noisy logic grounds from analog signal grounds to reduce coupling.
- If the power planes are separated into high-speed, low-speed, analog, or digital for isolation, do not route traces over these boundaries. If there are vacant areas on a ground or power plane, do not allow signal conductors to cross the vacant area. These interruptions in the power plane generally increase the return current path and emissions.
- Avoid changing layers with signal traces. Return current flows on the adjacent ground/power plane and must find a path to the new plane when the signal trace changes layers, resulting in increased loop area and emissions.
- Connect all ground vias to every ground plane, and similarly, connect every power via to all power planes at equal potential.
- Connect all the high-speed and sensitive signal returns closest to the chassis ground.
- Provide multiple direct metal-to-metal contacts for circuit board grounds to the chassis connections, unless the circuit ground must float. Unintended insulation formed by paint over-spray, washers, or non-conductive coatings degrade the ground connection and increase radiation levels.
- Between the connector pins, equally disperse the DC power and ground traces among the digital signals. It is best to have every signal pin surrounded by ground pins in all four directions. If this is not possible: 1) Use at least one ground for every signal, or, 2) Do not allow for more than a $^{1}/_{4}$" of space from the signal to its return pin. The spacing may need to be less for high density connectors.
- Keep the power plane shorter than the ground plane by at least 5X the spacing between the power and ground planes. This allows any AC difference in potential to be absorbed by the ground plane.

3.2 Component Placement

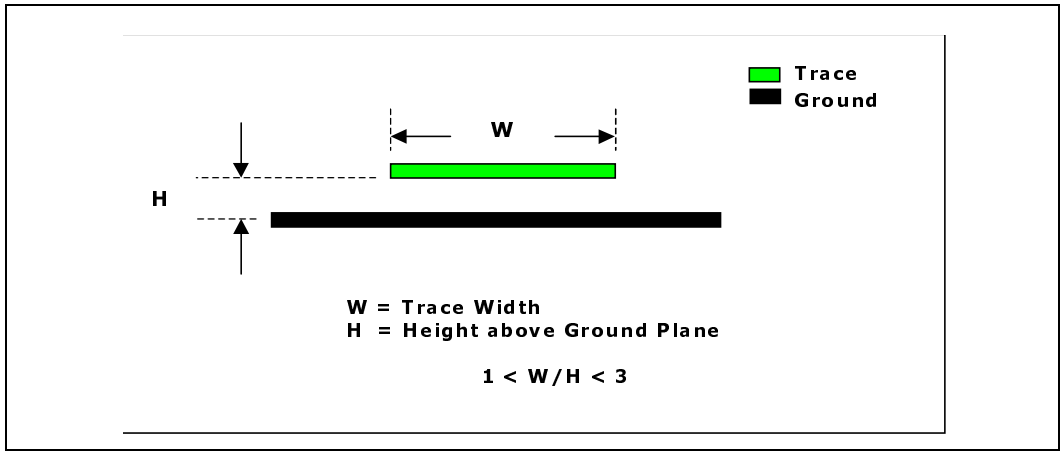
Component placement can influence the amount of EMI generated. The guidelines below are general approaches to minimize EMI.

- Keep leads on through hole components short. Mount the components as close to the PCB as possible and trim leads if necessary.
- Place all components associated with one clock trace closely together. This reduces the trace length and reduces radiation.
- Place high-current devices as closely as possible to the power sources.
- Minimize the use of sockets in high frequency portions of the board. Sockets introduce higher inductance and mis-matched impedance.
- Keep crystal, oscillators, and clock generators away from I/O ports and board edges. EMI from these devices can be coupled onto the I/O ports.
- Position crystals so that they lie flat against the PC board. This minimizes the distance to the ground plane and provides better coupling of electromagnetic fields to the board.
- Connect the crystal retaining straps to the ground plane. These straps, if ungrounded, can behave as an antenna and radiate.
- Provide a ground pad equal or larger than footprint under crystals and oscillators on the component side of the board. This ground pad should be tied to the ground planes with multiple vias.

3.3 Trace Routing

It is very critical to properly route traces for EMC testing, especially traces carrying high-speed signals. It is recommended to manually route all the high-speed traces and not rely on the auto-routers. The key factors in controlling the trace radiation are the trace length and the ratio of trace width to trace height above the ground plane. To minimize trace inductance, keep clock and other high-speed traces short, as wide as possible, and on signal layers that are adjacent to either ground or power plane. As shown in Figure 5, this ratio is ideally somewhere between 1:1 and 3:1. The radiation level or impedance is not appreciably reduced for ratios above 3:1. Above this length, traces begin to act like antennas and increase radiation.

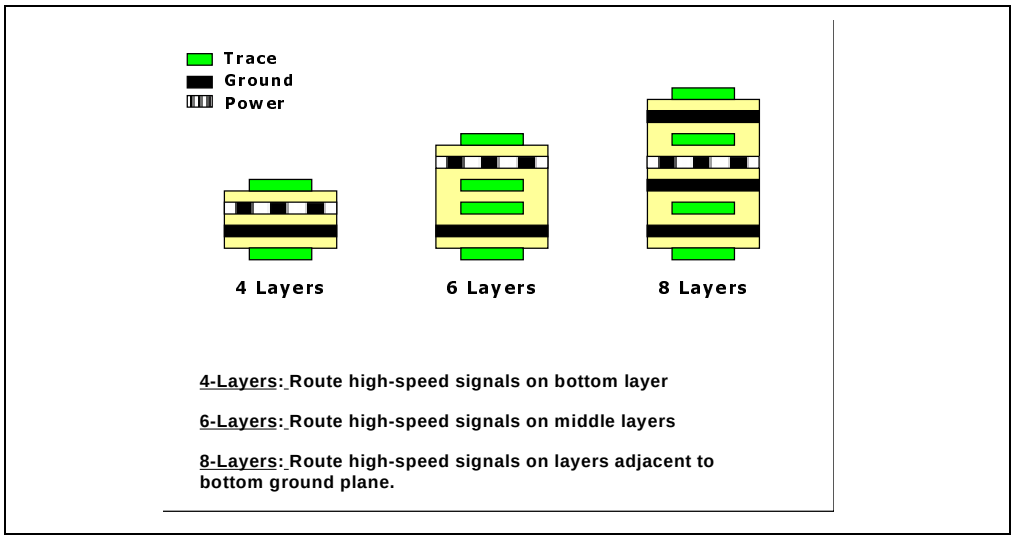
Figure 5. Trace Geometry



The following guidelines will also help improve the radiation:

- For multi-layer boards, the power and ground planes can be distributed between various signal layers to improve coupling between the signal and ground planes. The power and ground planes may be considered equivalent, since they are both capacitively coupled together. For platform specific board stackup and geometry, please refer to the Intel Design Guide Recommendation Documents.

Figure 6. Power/Ground Layer Stacking



For inner traces on multi-layer boards greater than 4, it is recommended to limit the trace length on external layers. For traces that are not treated as transmission lines (i.e., clocks and strobes), keep the length of the trace conductor to $^{1}/_{20}$th of a wavelength of the highest harmonic of interest. For example, if EMI is a concern on the 10th harmonic of a 32 MHz signal, the maximum ground trace length is:

Max external trace length = [30000 (or 20000) cm/sec] ÷ [20 X 320 MHz]*
= 4.69 cm

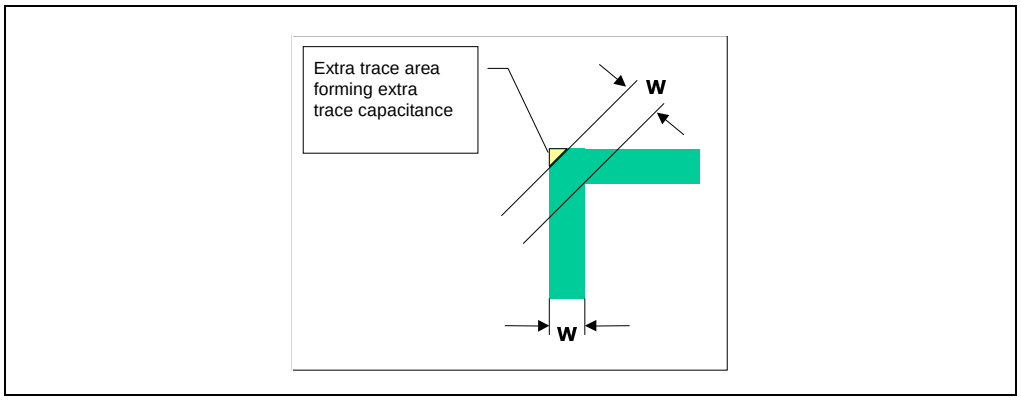
* 20000 cm/sec assumes typical PCB material.

This applies to the external routing of clock and strobes.

Note that the above equation assumes a wave traveling through free space. In the PCB, the wave velocity over a dielectric will differ from above and depends on PCB material (typically in the range of 66% of the speed of light in free space). However, the above calculation still applies with a high degree of confidence.

- For high-speed signals, keep the number of corners and vias to a minimum. When necessary to turn 90 degree corners, use two 45 degree bends or arcs. A 90 degree corner causes a mismatch in impedance by changing the trace capacitance coupling.

Figure 7. Trace Corners



- To improve isolation between traces, increase the spacing between adjacent traces or add guard traces on either side of critical traces. Adding shield planes between adjacent trace layers also helps.
- Do not route any traces or vias under crystals, oscillators or clock generators. Breaking into this region reduces the coupling area, and provides a path for RF to couple from clock device to the trace.
- To contain the field around traces near the edges of the board, keep traces away from the board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or other boards.
- Keep traces from clocks and drivers away from apertures by a distance greater than the largest aperture dimension.
- When changing from one layer to another layer, if the two layers are not equidistant from a power/ground plane, it is necessary to change trace width and spacing to maintain the impedance of the trace. Changing layers should be avoided if at all possible as the effect on loop area invariably results in higher emissions.

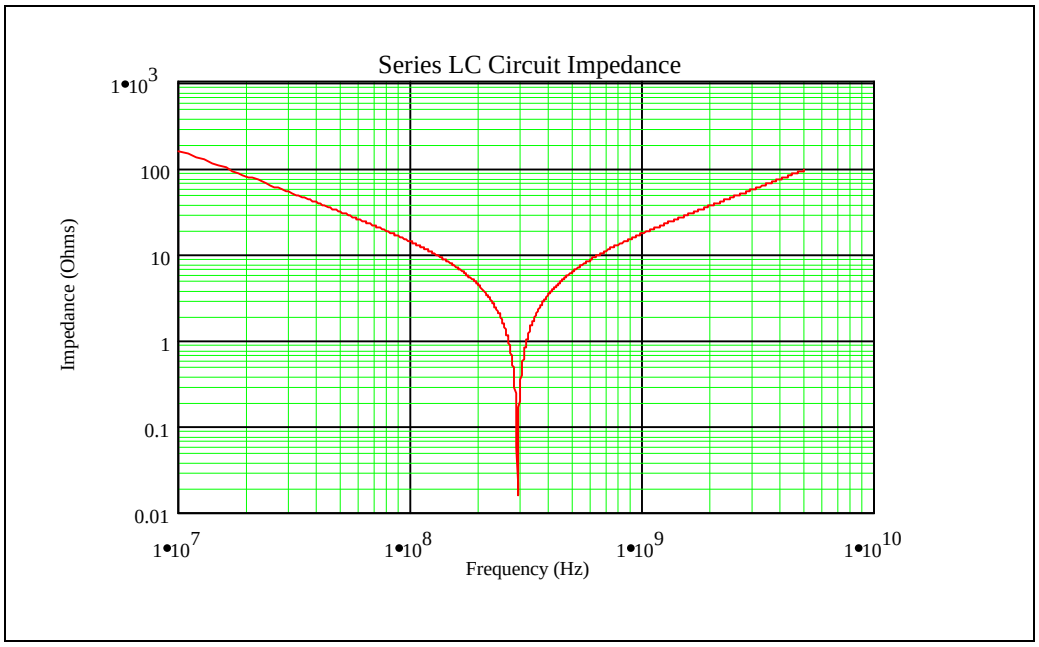
3.4 Power Decoupling

Decoupling capacitors serve two purposes:

- First, they are sources of charge to devices that are sinking or sourcing high frequency currents. The capacitors act like charge buckets, quickly supplying or accepting current, as required by the devices located in the immediate vicinity. Decoupling capacitors reduce the voltage sags and ground shifts.
- Secondly, the capacitors provide a path for the high frequency return currents on the power plane to reach ground. If the capacitors are not available, these currents return to ground through I/O signals or power connectors, creating large loops and increasing radiation.

Bypass capacitors self-resonate at a specific frequency and this phenomenon must be considered. For noise signals a few decades above the self-resonant frequency, the bypass capacitor becomes inductive and ineffective in filtering these signals. More capacitance is not always better. Leads on components and in IC packages typically add about 8 nH of inductance per inch. This forms a series LC circuit with the capacitor, causing it to appear as an inductor above the resonant frequency. A typical SMT capacitor installation has about 3 nH of series inductance from all sources.

Figure 8. 100 pF in series with 3 nH



$$f = \frac{1}{2\Pi} \times \sqrt{\frac{1}{LC}}$$

Thus, 100 pF capacitors typically are adequate for RF bypassing on many current products. With a total inductance of 3 nH, these capacitors resonate at about 290 MHz. However, 500 pF capacitors with a total inductance of 3 nH will resonate at about 130 MHz and must be used with care in high-speed systems.

- Keep the trace lengths less than 0.2 inches. Bypass each active component beneath the component or adjacent to its V_{CC} pin.
- Adhere to the recommended bypass requirements specified by the component manufacturers.
- It is best to make provisions for bypass capacitor at each component. However, If it is not possible to bypass every active component, skip the slower devices in the interest of the high frequency devices.
- Once boards are assembled, based on EMI test results, board designers could decide to either populate or leave-out the bypass capacitors.
- Alternate two values of bypass capacitors. Always be sure the values are different by at least 2 orders of magnitude. For example, 0.1 uF and 0.001 uF capacitors could be used.
- Distribute the bypass capacitors in a checkerboard pattern.
- Carefully match the type and value of capacitor to the range of frequencies it must bypass (i.e., tantalum capacitors are more effective at higher frequencies than aluminum electrolytic capacitors, and capacitors of different values are effective at different frequencies).
- Use surface mount bypass capacitors. They are more effective than through-hole capacitors because they eliminate inductive leads.
- Each bypass capacitor should have its own via to ground and power. The lead inductance cannot be totally eliminated as there are leads inside the IC, but it can be minimized.

- Bypass all power leads with large capacitors (for example 22 uF) where the power first enters the circuit board. Distribute the large capacitors in a 6 inch grid.
- Do not use feed through holes between the bypass capacitor and the circuitry it is intended to decouple. This is especially applicable to high-speed digital circuitry such as Schottky or ECL, or low level analog circuitry.

3.5 Minimizing Board Conducted Emissions

High frequency noise conducted through an I/O cable can cause the receiving device to radiate. The following may lead to reduction in Conducted Emissions.

- I/O cables are a common source of radiation and proper filtering can greatly reduce the emission levels. Provide each signal on an I/O connector with its own return line. This is the optimum arrangement, but might not always be possible for predefined I/O connectors such as printers and serial ports.
- Bypass every signal conductor in an I/O cable leaving the enclosure to chassis ground.
- If cost effective and functionally possible, use filtered connectors. They have feed through bypass capacitors with high self-resonant frequencies, making them useful in filtering I/O cables. The extra cost of the filtered connectors may be traded against the cost of alternate filtering which requires board real estate.
- A solid bond is essential at the I/O connector to chassis and ground plane.
- Ferrite beads may be used to add high frequency loss to a circuit without introducing power loss at DC and low frequencies. They are effective when used to damp out high frequency oscillations from switching transients or parasitic resonances within a circuit. They may also be used to prevent high frequency noise from being conducted into a circuit on power supply or other leads. Ferrite beads are modeled as a series inductance and resistance. The magnitude of their impedance is given by:

$$|Z| = \sqrt{R^2 + (2\Pi fL)^2}$$

Where:
R = equivalent resistance of the bead in ohms
L = equivalent inductance of the bead in henries
f = frequency in hertz
π = 3.1415926...

The impedance of a single bead is generally limited to about 100 ohms. They are, therefore, most effective in low-impedance circuits such as power supplies, class C power amplifiers, resonant circuits and SCR switching circuits. If a single bead does not provide enough attenuation, multiple beads may be used. If two or three beads do not solve the problem, additional beads are not normally effective and other techniques should be employed. Ferrite beads are available either as loose beads which may be slipped over existing wires or installed on wire leads and in rolls suitable for automatic insertion equipment.

- Common mode chokes are an effective alternative when case shielding is not available.
- As a last resort, pass cables one or more times through common mode ferrite toroids to raise shield impedances and reduce shield currents.
- Position the processor connector on the motherboard so that it is at least two inches away from the I/O connector pins. This should reduce coupling to manageable levels.

4.0 System EMI Design Recommendations

4.1 Chassis Construction

The system case reduces EMI by containing EMI radiation. The two main factors that impact the effectiveness of the case in reducing EMI are the case material and discontinuities in the case. The following points help mitigate case discrepancies.

- Keep chassis seams as far away from the processor as practical. The example below shows that seams become leaky at $^{1}/_{20}$ wavelength. Therefore, even seams 2 inches long leak 300 MHz frequency EMI.

$$f = {}^{c}/_{\lambda}$$

Where:
f = frequency passed through the seam
c = speed of light = 3 × 108 m/s
$^{\lambda}/_{20}$ = length of the seam = 2” = 0.05m
λ = 40” = 1m
f = 3 × 108/1m = 300 MHz

- Where possible, use round holes instead of slotted holes. Round holes provide the greatest airflow volume for the least amount of EMI leakage.
- Thin material works fine for most high frequency I/O shielding. However, I/O shielding should be grounded at as many points as possible. I/O shielding may need to be stiffened to prevent system to system EMI variation.

4.2 Cabling

Cables make excellent antennas. The following suggestions reduce the impact of cables on EMI radiation.

- Provide adequate grounding for all cables.
- Ground both ends of cables to chassis ground.
- To prevent coupling, keep all cables away from chassis seams.
- Use ferrite beads to attenuate common mode noise on I/O cables.